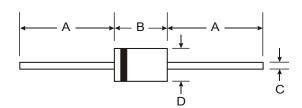


SF30AG - SF30JG

3.0A SUPER-FAST GLASS PASSIVATED RECTIFIER

Features

- Glass Passivated Die Construction
- **Diffused Junction**
- Super-Fast Switching for High Efficiency
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 125A Peak Low Reverse Leakage Current
- Plastic Material: UL Flammability Classification Rating 94V-0



Mechanical Data

Case: Molded Plastic

Terminals: Plated Leads Solderable per MIL-STD-202, Method 208

Polarity: Cathode Band Marking: Type Number

Weight: 1.12 grams (approx.)

Mounting Position: Any

DO-201AD								
Dim	Min	Max						
Α	25.40	_						
В	7.20	9.50						
С	1.20	1.30						
D	4.80	5.30						
All Dimensions in mm								

Maximum Ratings and Electrical Characteristics @ $T_A = 25^{\circ}C$ unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristic	Sym		SF30 AG	SF30 BG	SF30 CG	SF30 DG	SF30 FG	SF30 GG	SF30 HG	SF30 JG	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V _{RI} V _{RV}	VM	50	100	150	200	300	400	500	600	٧
RMS Reverse Voltage	V _{R(R}	MS)	35	70	100	140	210	280	350	420	V
Average Rectified Output Current (Note 1) @ T _A =	55°C)	3.0						Α		
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave Superimposed on Rated (JEDEC Method)	d Load I _{FS}	М	125							А	
Forward Voltage @ I _F =	: 3.0A V _F	М	0.95 1.3 1.5				.5	V			
Peak Reverse Current @ T _A = at Rated DC Blocking Voltage @ T _A =		5.0 100							μА		
Reverse Recovery Time (Note 3)			35 40				5	0	ns		
Typical Junction Capacitance (Note 2)		j	75 50							pF	
Typical Thermal Resistance Junction to Ambient		JA	32							K/W	
Operating and Storage Temperature Range		STG	-65 to +150							°C	

1. Valid provided that leads are maintained at ambient temperature at a distance of 9.5mm from the case. Notes:

- 2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.
- 3. Measured with $I_F = 0.5A$, $I_R = 1.0A$, $I_{rr} = 0.25A$. See Figure 5.



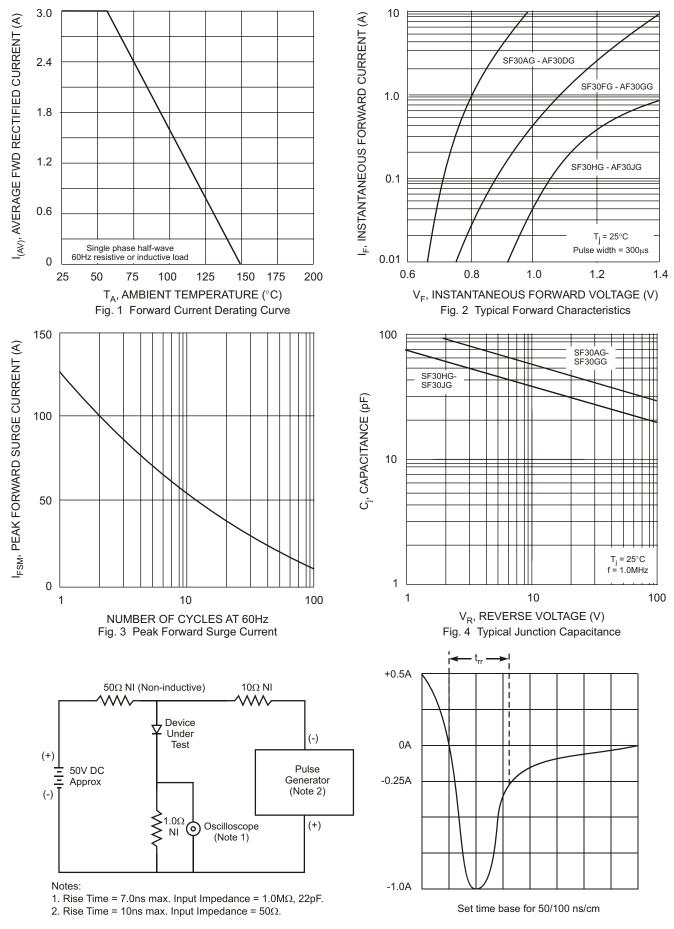


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit