19-6043; Rev 1; 3/12

EVALUATION KIT AVAILABLE

MAX17498A/MAX17498B/MAX17498C

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications

General Description

The MAX17498A/MAX17498B/MAX17498C devices are current-mode fixed-frequency flyback/boost converters with a minimum number of external components. They contain all the control circuitry required to design wide input voltage isolated and nonisolated power supplies. The MAX17498A has its rising/falling undervoltage lockout (UVLO) thresholds optimized for universal offline (85V AC to 265V AC) applications, while the MAX17498B/MAX17498C support UVLO thresholds suitable to low-voltage DC-DC applications.

The switching frequency of the MAX17498A/MAX17498C flyback converters is 250kHz, while that of the MAX17498B flyback/boost converter is 500kHz. These frequencies allow the use of tiny magnetic and filter components, resulting in compact, cost-effective power supplies. An EN/UVLO input allows the user to start the power supply precisely at the desired input voltage, while also functioning as an on/off pin. The OVI pin enables implementation of an input overvoltage-protection scheme that ensures that the converter shuts down when the DC input voltage exceeds the desired maximum value.

The devices incorporate a flexible error amplifier and an accurate reference voltage (REF) to enable the end user to regulate both positive and negative outputs. Programmable current limit allows proper sizing and protection of the primary switching FET. The MAX17498B supports a maximum duty cycle of 92% and provides programmable slope compensation to allow optimization of control-loop performance. The MAX17498A/MAX17498C support a maximum duty cycle of 49%, and have fixed internal slope compensation for optimum control-loop performance. The devices provide an open-drain PGOOD pin that serves as a power-good indicator and enters the high-impedance state to indicate that the flyback/boost converter is in regulation. An SS pin allows programmable soft-start time for the flyback/boost converter. Hiccup-mode overcurrent protection and thermal shutdown are provided to minimize dissipation under overcurrent and overtemperature fault conditions. The devices are available in a space-saving, 16-pin (3mm x 3mm) TQFN package with 0.5mm lead spacing.

***Ordering Information* appears at end of data sheet.**

***Typical Application Circuits* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX17498A.related**.*

Benefits and Features

- **Peak Current-Mode Flyback/Boost Converter**
- **Current-Mode Control Provides Excellent Transient Response**
- **Fixed Switching Frequency**
  - ✧ **250kHz (MAX17498A/MAX17498C)**
  - ✧ **500kHz (MAX17498B)**
- **Flexible Error Amplifier to Regulate Both Positive and Negative Outputs**
- **Programmable Soft-Start to Reduce Input Inrush Current**
- **Programmable Voltage or Current Soft-Start**
- **Power-Good Signal (PGOOD)**
- **Reduced Power Dissipation Under Fault**
  - ✧ **Hiccup-Mode Overcurrent Protection**
  - ✧ **Thermal Shutdown with Hysteresis**
- **Robust Protection Features**
  - ✧ **Flyback/Boost Programmable Current Limit**
  - ✧ **Input Overvoltage Protection**
- **Optimized Loop Performance**
  - ✧ **Programmable Slope Compensation for Flyback/Boost Maximizes Obtainable Phase Margin**
- **High Efficiency**
  - ✧ **175mΩ, 65V Rated n-Channel MOSFET Offers Typical Efficiency Greater Than 80%**
  - ✧ **No Current-Sense Resistor**
- **Optional Spread Spectrum**
- **Space-Saving, 16-Pin (3mm x 3mm) TQFN Package**

Applications

Front-End AC-DC Power Supplies for Industrial Applications (Isolated and Nonisolated)

Telecom Power Supplies

Wide Input Range DC Input Flyback/Boost Industrial Power Supplies

ABSOLUTE MAXIMUM RATINGS

IN to SGND ..... -0.3V to +40V
EN/UVLO to SGND ..... -0.3V to IN + 0.3V
OVI to SGND ..... -0.3V to V_{CC} + 0.3V
V_{CC} to SGND ..... -0.3V to +6V
SS, LIM, EA-, EA+, COMP, SLOPE, REF to SGND ..... -0.3V to (V_{CC} + 0.3V)
LX to SGND ..... -0.3V to +70V
PGOOD to SGND ..... -0.3V to +6V
PGND to SGND ..... -0.3V to +0.3V
Continuous Power Dissipation (Single-Layer Board)
TQFN (derate 20.8mW/°C above +70°C) 1700mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature (continuous) ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})					
IN Voltage Range (V_{IN})	MAX17498A	4.5		29	V
	MAX17498B/MAX17498C	4.5		36	
IN Supply Startup Current Under UVLO	$I_{INSTARTUP}$, V_{IN} < UVLO or EN/UVLO = SGND		22	36	µA
IN Supply Current (I_{IN})	Switching, f_{SW} = 250kHz (MAX17498A/MAX17498C)		1.8	3	mA
	Switching, f_{SW} = 500kHz (MAX17498B)		2	3.25	
IN Boostrap UVLO Rising Threshold	MAX17498A	19	20.5	22	V
	MAX17498B/MAX17498C	3.85	4.15	4.4	
IN Bootstrap UVLO Falling Threshold		3.65	3.95	4.25	V
IN Clamp Voltage	EN/UVLO = SGND, I_{IN} = 1mA (MAX17498A) (Note 2)	31	33.5	36	V
LINEAR REGULATOR (V_{CC})					
V_{CC} Output Voltage Range	6V < V_{IN} < 29V, 0mA < I_{VCC} < 50mA	4.8	5	5.2	V
V_{CC} Dropout Voltage	V_{IN} = 4.5V, I_{VCC} = 20mA		160	300	mV
V_{CC} Current Limit	V_{CC} = 0V, V_{IN} = 6V	50	100		mA
ENABLE (EN/UVLO)					
EN/UVLO Threshold	Rising	1.18	1.23	1.28	V
	Falling	1.11	1.17	1.21	
EN/UVLO Input Leakage Current	0V < $V_{EN/UVLO}$ < 1.5V, T_A = +25°C	-100	0	+100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION (OVI)					
OVI Threshold	Rising	1.18	1.23	1.28	V
	Falling	1.11	1.17	1.21	
OVI Masking Delay			2		µs
OVI Input Leakage Current	0V < V_{OVI} < 1.5V, T_A = +25°C	-100	0	+100	nA
SWITCHING FREQUENCY AND MAXIMUM DUTY CYCLE (f_{SW} and D_{MAX})					
Switching Frequency	MAX17498A/MAX17498C	235	250	265	kHz
	MAX17498B	470	500	530	
Maximum Duty Cycle	MAX17498A/MAX17498C	47.5	48.75	50	%
	MAX17498B	90	92	94	
Minimum Controllable On Time	t_{ONMIN}		110		ns
SOFT-START (SS)					
SS Set-Point Voltage		1.2	1.22	1.24	V
SS Pullup Current	V_{SS} = 400mV	9	10	11	µA
SS Peak Current-Limit-Enable Threshold		1.11	1.17	1.21	V
ERROR AMPLIFIER (EA+, EA-, and COMP)					
EA+ Input Bias Current	V_{EA+} = 1.5V, T_A = +25°C	-100		+100	nA
EA- Input Bias Current	V_{EA-} = 1.5V, T_A = +25°C	-100		+100	nA
Error-Amplifier Open-Loop Voltage Gain			90		dB
Error-Amplifier Transconductance	V_{COMP} = 2V, V_{LIM} = 1V	1.5	1.8	2.1	mS
Error-Amplifier Source Current	V_{COMP} = 2V, EA- < EA+	80	120	210	µA
Error-Amplifier Sink Current	V_{COMP} = 2V, EA- > EA+	80	120	210	µA
Current-Sense Transresistance		0.45	0.5	0.55	Ω
INTERNAL SWITCH					
DMOS Switch On-Resistance (R_{DSON})	I_{LX} = 200mA		175	380	mΩ
DMOS Peak Current Limit	LIM = 100K	1.62	1.9	2.23	A
DMOS Runaway Current Limit	LIM = 100K	1.9	2.3	2.6	A
LX Leakage Current	V_{LX} = 65V, T_A = +25°C		0.1	1	µA
CURRENT LIMIT (LIM)					
LIM Reference Current		9	10	11	µA
Peak Switch Current Limit with LIM Open		0.39	0.45	0.54	A
Runaway Switch Current Limit with LIM Open		0.39	0.5	0.6	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Number of Peak Current-Limit Hits Before Hiccup Timeout			8		#
Number of Runaway Current-Limit Hits Before Hiccup Timeout			1		#
Overcurrent Hiccup Timeout			32		ms
SLOPE COMPENSATION (SLOPE)					
SLOPE Pullup Current		9	10	11	µA
SLOPE-Compensation Resistor Range	MAX17498B	30		150	kΩ
Default SLOPE-Compensation Ramp	SLOPE = open		60		mV/µs
POWER-GOOD SIGNAL (PGOOD)					
PGOOD Output-Leakage Current (Off State)	V_{PGOOD} = 5V, T_A = +25°C	-1		+1	µA
PGOOD Output Voltage (On State)	I_{PGOOD} = 10mA	0		0.4	V
PGOOD Higher Threshold	EA- rising	93.5	95	96.5	%
PGOOD Lower Threshold	EA- falling	90.5	92	93.5	%
PGOOD Delay After EA- Reaches 95% Regulation			4		ms
THERMAL SHUTDOWN					
Thermal-Shutdown Threshold	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis			20		°C

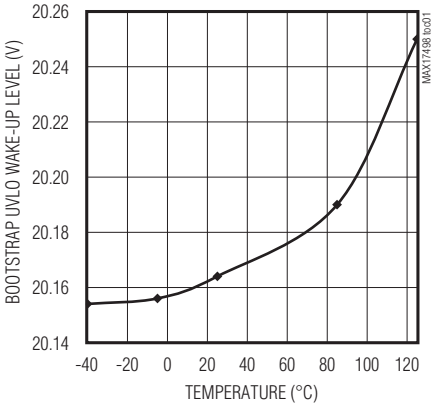
Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: The MAX17498A is intended for use in universal input power supplies. The internal clamp circuit at IN is used to prevent the bootstrap capacitor from changing to a voltage beyond the absolute maximum rating of the device when EN/UVLO is low (shutdown mode). Externally limit the maximum current to IN (hence to clamp) to 2mA (max) when EN/UVLO is low.

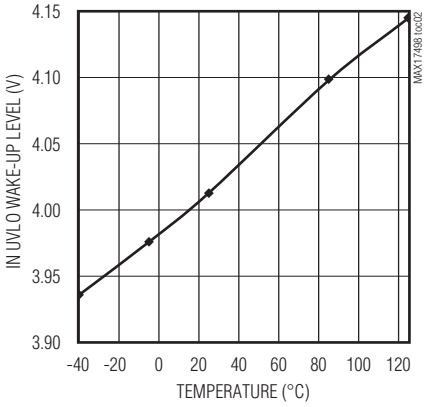
Typical Operating Characteristics

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

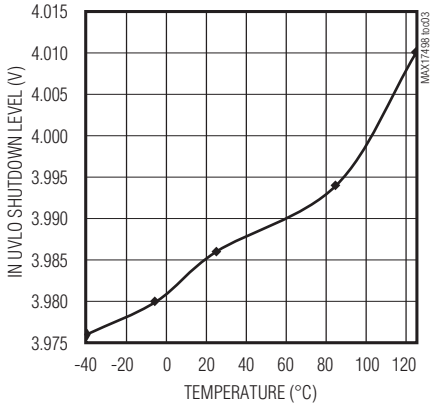
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17498A)



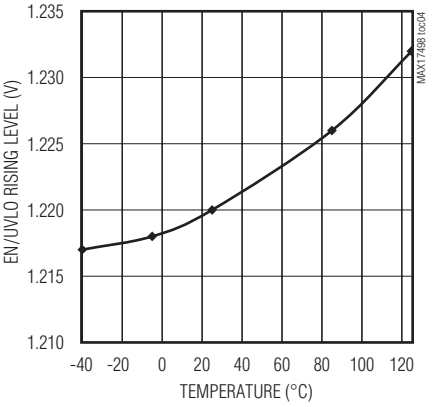
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17498B/MAX17498C)



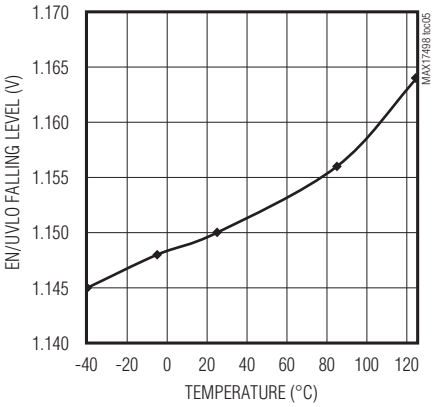
IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE



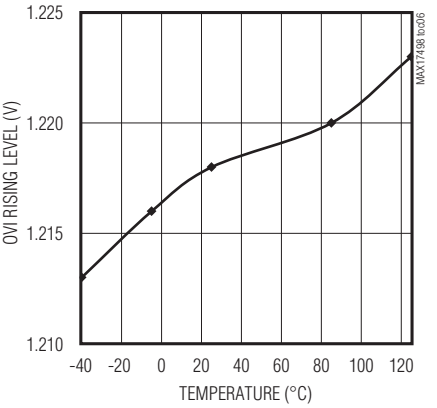
EN/UVLO RISING LEVEL vs. TEMPERATURE



EN/UVLO FALLING LEVEL vs. TEMPERATURE



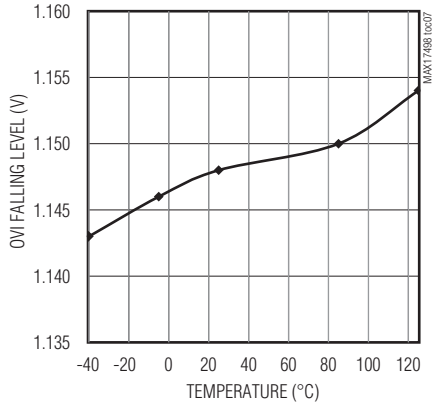
OVI RISING LEVEL vs. TEMPERATURE



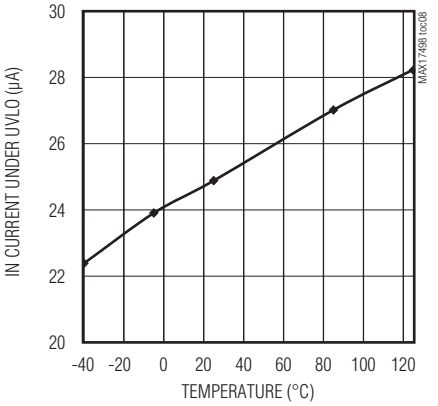
Typical Operating Characteristics (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

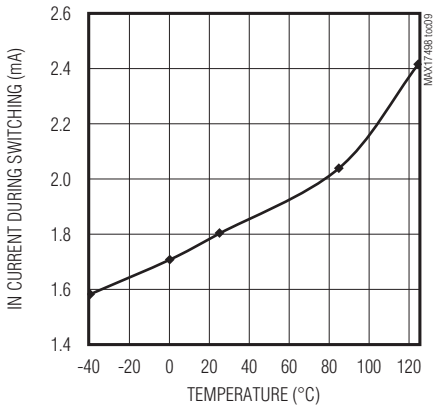
OVI FALLING LEVEL vs. TEMPERATURE



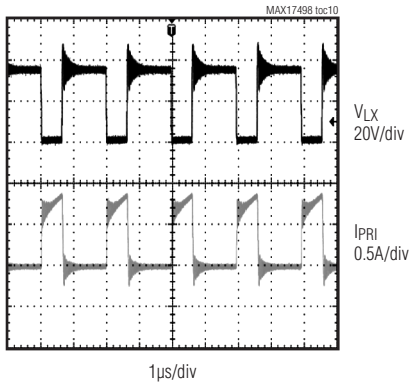
IN CURRENT UNDER UVLO vs. TEMPERATURE



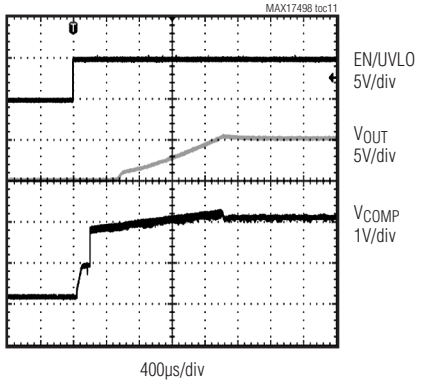
IN CURRENT DURING SWITCHING vs. TEMPERATURE



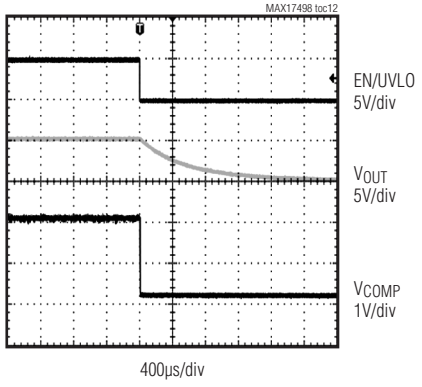
LX AND PRIMARY CURRENT WAVEFORM



EN STARTUP WAVEFORM



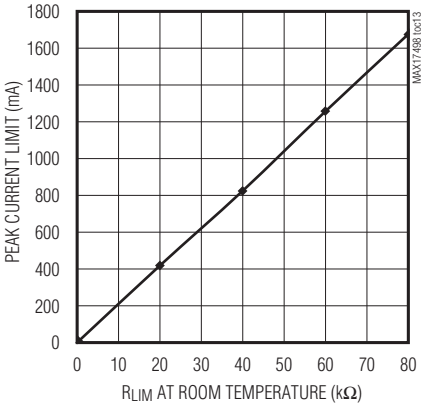
EN SHUTDOWN WAVEFORM



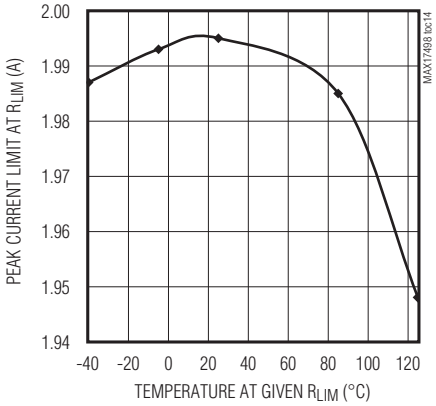
Typical Operating Characteristics (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

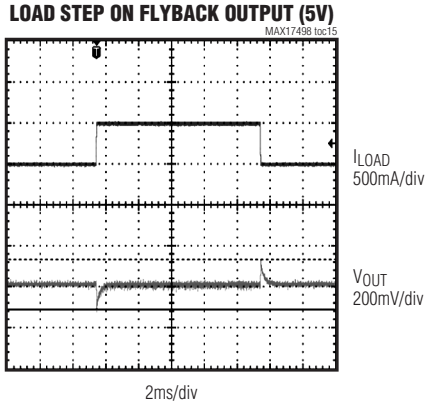
PEAK CURRENT LIMIT (I_{LIM}) vs. R_{LIM} AT ROOM TEMPERATURE



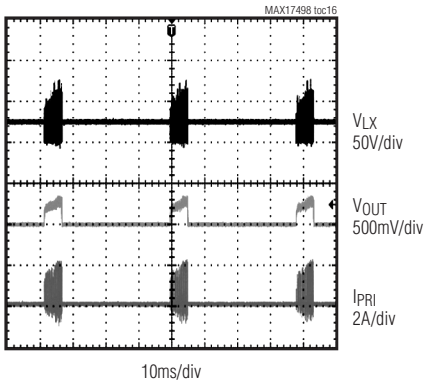
PEAK CURRENT LIMIT AT R_{LIM} = 100kΩ vs. TEMPERATURE



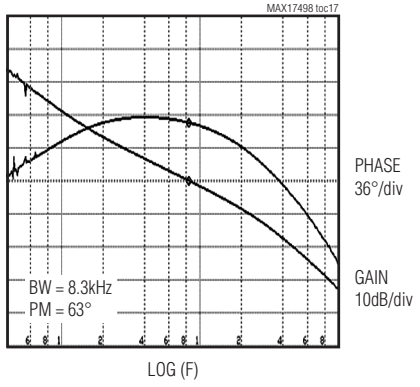
TRANSIENT RESPONSE FOR 50% LOAD STEP ON FLYBACK OUTPUT (5V)



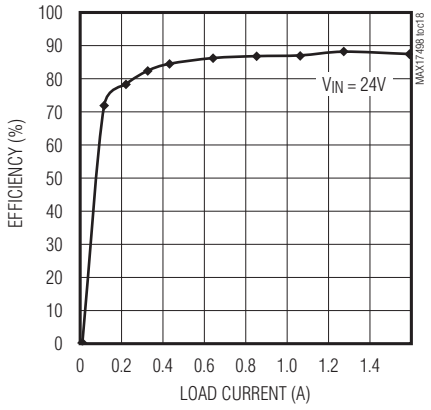
SHORT-CIRCUIT PROTECTION



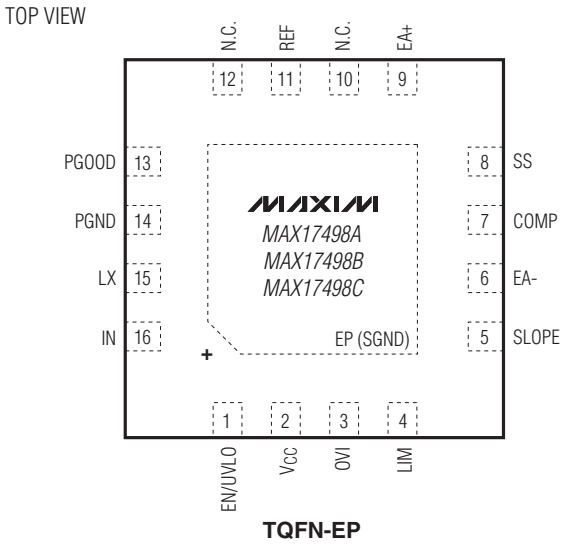
BODE PLOT - (5V OUTPUT AT 24V INPUT)



EFFICIENCY GRAPH AT 24V INPUT (FLYBACK REGULATOR)



Pin Configuration



TQFN-EP

Pin Description

PIN	NAME	FUNCTION
1	EN/UVLO	Enable/Undervoltage-Lockout Pin. Drive to > 1.23V to start the devices. To externally program the UVLO threshold of the input supply, connect a resistor-divider between input supply EN/UVLO and SGND.
2	V_{CC}	Linear Regulator Output. Connect input bypass capacitor of at least 1µF from V_{CC} to SGND as close as possible to the IC.
3	OVI	Overvoltage Comparator Input. Connect a resistor-divider between the input supply (OVI) and SGND to set the input overvoltage threshold.
4	LIM	Current-Limit Setting Pin. Connect a resistor between LIM and SGND to set the peak-current limit for nonisolated flyback converter. Peak-current limit defaults to 500mA if unconnected.
5	SLOPE	Slope Compensation Input Pin. Connect a resistor between SLOPE and SGND to set slope-compensation ramp. Connect to V_{CC} for minimum slope compensation. See the *Programming Slope Compensation (SLOPE)* section.
6	EA-	Inverting Input of the Flexible Error Amplifier. Connect to mid-point of resistor-divider from the positive terminal output to SGND.
7	COMP	Flexible Error-Amplifier Output. Connect the frequency-compensation network between COMP and SGND.
8	SS	Soft-Start Pin. Connect a capacitor from SS to SGND to set the soft-start time interval.
9	EA+	Noninverting Input of the Flexible Error Amplifier. Connect to SS to use 1.22V as the reference.
10, 12	N.C.	No Connection
11	REF	Internal 1.22V Reference Output Pin. Connect a 100pF capacitor from REF to SGND.

Pin Description (continued)

PIN	NAME	FUNCTION
13	PGOOD	Open-Drain Output. PGOOD goes high when EA- is within 5% of the set point. PGOOD pulls low when EA- falls below 92% of its set-point value.
14	PGND	Power Ground for Converter
15	LX	External Transformer/Inductor Connection for the Converter
16	IN	Internal Linear Regulator Input. Connect IN to the input-voltage source. Bypass IN to PGND with a 1µF (min) ceramic capacitor.
—	EP (SGND)	Exposed Pad. Internally connected to SGND. Connect EP to a large copper plane at SGND potential to provide adequate thermal dissipation. Connect EP (SGND) to PGND at a single point.

Detailed Description

The MAX17498A offers a bootstrap UVLO wakeup level of 20V with a wide hysteresis of 15V (min) optimized for implementing an isolated and nonisolated universal (85V AC to 265V AC) offline single-switch flyback converter or telecom (36V to 72V) power supplies. The MAX17498B/MAX17498C offer a UVLO wakeup level of 4.4V and are well suited for low-voltage DC-DC flyback/boost power supplies. An internal reference (1.22V) can be used to regulate the output down to 1.23V in nonisolated flyback and boost applications. Additional semi-regulated outputs, if needed, can be generated by using additional secondary windings on the flyback converter transformer. A flexible error amplifier and REF allow the end-user selection between regulating positive and negative outputs.

The devices utilize peak current-mode control and external compensation for optimizing the loop performance for various inductors and capacitors. The devices include a cycle-by-cycle peak current limit and eight consecutive occurrences of current-limit event trigger hiccup mode, that protect external components by halting switching for a period of time (32ms). The devices also include voltage soft-start for nonisolated designs and current soft-start for isolated designs to allow monotonic rise of the output voltage. The voltage or current soft-start can be selected using the SLOPE pin. See the *Block Diagram* for more information.

Input Voltage Range

The MAX17498A has different rising and falling UVLO thresholds on the IN pin than those of the MAX17498B/MAX17498C. The thresholds for the MAX17498A are optimized for implementing power-supply startup schemes typically used for offline AC-DC power supplies. The MAX17498A is therefore well suited for operation from the rectified DC bus in AC-DC power-supply applications typically encountered in front-end industrial power-supply applications. As such, the MAX17498A has no limitation on the maximum input voltage as long as the external components are rated suitably and the maximum operating voltages of the MAX17498A are respected. The MAX17498A can successfully be used in universal input-rectified (85V to 265V AC) bus applications, rectified 3-phase DC bus applications, and telecom (36V to 72V DC) applications.

The MAX17498B/MAX17498C are intended for implementing a flyback (isolated and nonisolated) and boost converter with an on-board 65V rated n-channel MOSFET. The IN pin of the MAX17498B/MAX17498C has a maximum operating voltage of 36V. The MAX17498B/MAX17498C implement rising and falling thresholds on the IN pin that assume power-supply startup schemes, typical of lower voltage DC-DC applications, down to an input voltage of 4.5V DC. Therefore, flyback converters with a 4.5V to 36V supply voltage range can be implemented with the MAX17498B/MAX17498C.

Internal Linear Regulator (Vcc)

The internal functions and driver circuits are designed to operate from a 5V ±5% power-supply voltage. The devices have an internal linear regulator that is powered from the IN pin and generates a 5V power rail. The output of the linear regulator is connected to the V_{CC} pin and should be decoupled with a 2.2µF capacitor to ground for stable operation. The V_{CC} converter output supplies the operating current for the devices. The maximum operating voltage of the IN pin is 29V for the MAX17498A and 36V for the MAX17498B/MAX17498C.

Configuring the Power Stage (LX)

The devices use an internal n-channel MOSFET to implement internal current sensing for current-mode control and overcurrent protection of the flyback/boost converter. To facilitate this, the drain of the internal nMOSFET is connected to the source of the external MOSFET in the MAX17498A high-input-voltage applications. The gate of the external MOSFET is connected to the IN pin. Ensure by design that the IN pin voltage does not exceed the maximum operating gate-voltage rating of the external MOSFET. The external MOSFET gate-source voltage is controlled by the switching action of the internal nMOSFET, while also sensing the source current of the external MOSFET. In the MAX17498B/MAX17498C-based applications, the LX pin is directly connected to either the flyback transformer primary winding or to the boost-converter inductor.

Maximum Duty Cycle

The MAX17498A/MAX17498C operate at a maximum duty cycle of 49%. The MAX17498B offers a maximum duty cycle of 92% to implement both flyback and boost converters involving large input-to-output voltage ratios in DC-DC applications.

Power-Good Signal (PGOOD)

The devices include a PGOOD signal that serves as a power-good signal to the system. PGOOD is an open-drain signal and requires a pullup resistor to the preferred supply voltage. The PGOOD signal monitors EA- and pulls high when EA- is 95% (typ) of its regulation value (1.22V). For isolated power supplies, PGOOD cannot serve as a power-good signal.

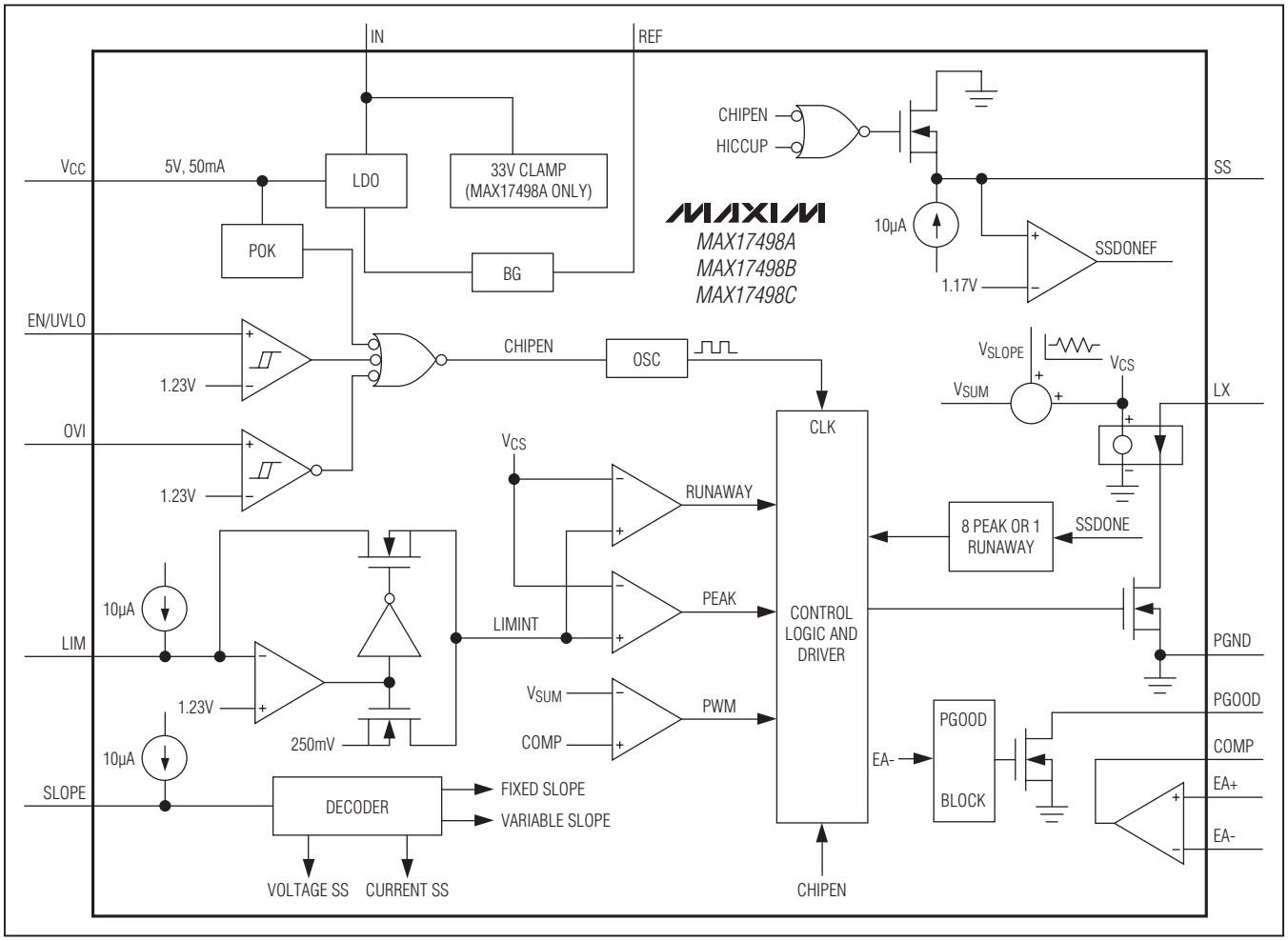


Figure 1. MAX17498A/MAX17498B/MAX17498C Block Diagram

Soft-Start

The devices implement soft-start operation for the flyback/boost converter. A capacitor connected to the SS pin programs the soft-start period for the flyback/boost converter. The soft-start feature reduces the input inrush current. These devices allow the end user to select between voltage soft-start usually preferred in nonisolated applications and current soft-start, which is useful in isolated applications to get a monotonic rise in the output voltage. See the *Programming Soft-Start of the Flyback/Boost Converter (SS)* section.

Spread-Spectrum Factory Option

For EMI-sensitive applications, a spread-spectrum-enabled version of the device can be requested from the factory. The frequency-dithering feature modulates the switching frequency by ±10% at a rate of 4kHz. This spread-spectrum-modulation technique spreads the energy of switching-frequency harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

Applications Information

Startup Voltage and Input Overvoltage-Protection Setting (EN/UVLO, OVI)

The devices' EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The devices do not commence startup operation unless the EN/UVLO pin voltage exceeds 1.23V (typ). The devices turn off if the EN/UVLO pin voltage falls below 1.17V (typ). A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.23V (typ) turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 2. When voltage at the OVI pin exceeds 1.23V (typ), the devices stop switching and resume switching operations only if voltage at the OVI pin falls below 1.17V (typ). For given values of startup DC input voltage (V_{START}), and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 24.9kΩ resistor for R_{OVI}:

$$R_{EN} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1\right] k\Omega$$

where R_{OVI} is in kΩ while V_{START} and V_{OVI} are in volts.

$$R_{SUM} = \left[R_{OVI} + R_{EN}\right] \times \left[\frac{V_{START}}{1.23} - 1\right] k\Omega$$

where R_{EN} and R_{OVI} are in kΩ. In universal AC input applications, R_{SUM} might need to be implemented as equal resistors in series (R_{DC1}, R_{DC2}, R_{DC3}) so that voltage across each resistor is limited to its maximum operation voltage.

$$R_{DC1} = R_{DC1} = R_{DC1} = \frac{R_{SUM}}{3} k\Omega$$

For low-voltage DC-DC applications based on the MAX17498B/MAX17498C, a single resistor can be used in the place of R_{SUM}, as the voltage across it is approximately 40V.

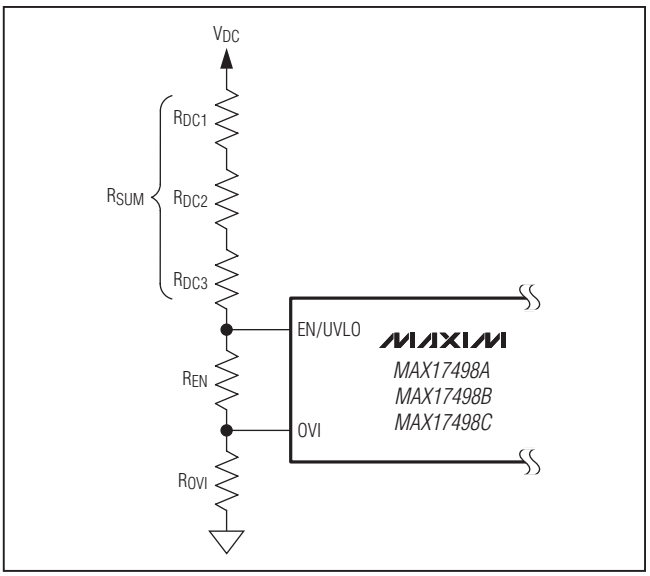


Figure 2. Programming EN/UVLO and OVI

Startup Operation

The MAX17498A is optimized for implementing an offline single-switch flyback converter and has a 20V IN UVLO wake-up level with hysteresis of 15V (min). In offline applications, a simple cost-effective RC startup circuit is used. When the input DC voltage is applied, the startup resistor (R_{START}) charges the startup capacitor (C_{START}), causing the voltage at the IN pin to increase towards the wake-up IN UVLO threshold (20V typ). During this time, the MAX17498A draws a low startup current of 20µA (typ) through R_{START}. When the voltage at IN reaches the wake-up IN UVLO threshold, the MAX17498A commences switching operations and drives the internal n-channel MOSFET whose drain is connected to the LX pin. In this condition, the MAX17998A draws 1.8mA current from C_{START}, in addition to the current required to switch the gate of the external nMOSFET. Since this current cannot be supported by the current through R_{START}, the voltage on C_{START} starts to drop. When suitably configured, as shown in Figure 10, the external nMOSFET is switched by the LX pin and the flyback/forward converter generates an output voltage (V_{OUT}) bootstrapped to the IN pin through the diode (D2). If V_{OUT} exceeds the sum of 5V and the drop across D2 before the voltage on C_{START} falls below 5V, then the IN voltage is sustained by V_{OUT}, allowing the MAX17498A to continue operating with energy from V_{OUT}. The large hysteresis (15V typ) of the MAX17498A allows for a small startup capacitor (C_{START}). The low startup curent (20µA typ) allows the use of a large start resistor (R_{START}), thus reducing power dissipation at higher DC bus voltages. Figure 3 shows the typical RC startup scheme for the MAX17498A. R_{START} might need to be implemented as equal, multiple resistors in series (R_{IN1}, R_{IN2}, and R_{IN3}) to share the applied high DC voltage in offline applications so that the voltage across each resistor is limited to the maximum continuous operating-voltage rating. R_{START} and C_{START} can be calculated as:

$$C_{START} = \left[I_{IN} + \left(\frac{Q_{GATE} \times f_{SW}}{10^6} \right) \right] \times \frac{t_{SS}}{10} \mu F$$

where I_{IN} is the supply current drawn at the IN pin in mA, Q_{GATE} is the gate charge of the external nMOSFET used in nC, f_{SW} is the switching frequency of the converter in Hz, and t_{SS} is the soft-start time programmed for the flyback/forward converter in ms. See the *Programming Soft-Start of the Flyback/Boost Converter (SS)* section.

$$R_{START} = \frac{(V_{START} - 10) \times 50}{[1 + C_{START}]} k\Omega$$

where C_{START} is the startup capacitor in µF.

For designs that cannot accept power dissipation in the startup resistors at high DC input voltages in offline applications, the startup circuit can be set up with a current source instead of a startup resistor as shown in Figure 4.

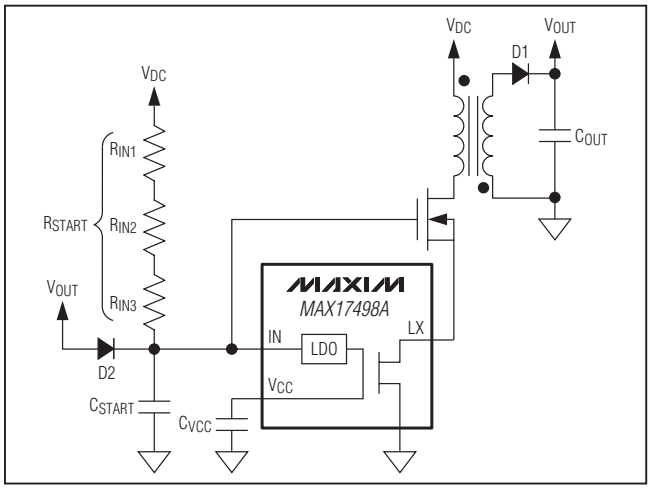


Figure 3. MAX17498A RC-Based Startup Circuit

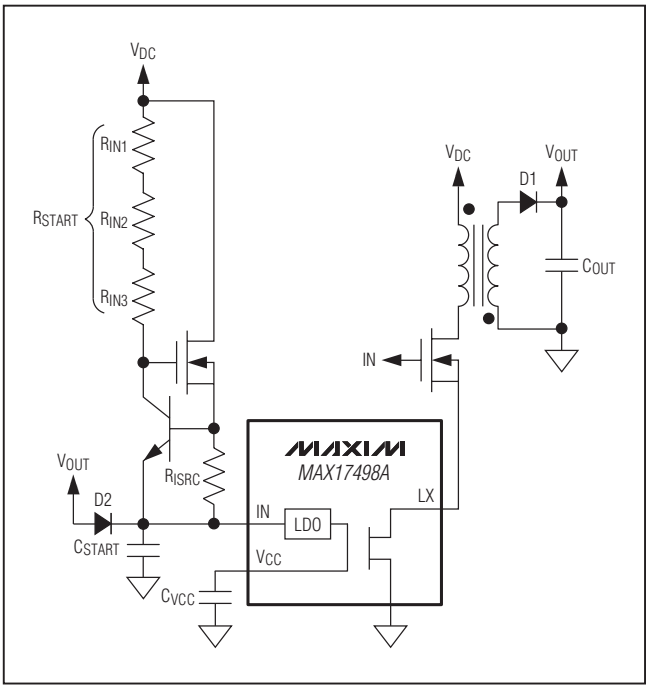


Figure 4. MAX17498A Current Source-Based Startup Circuit

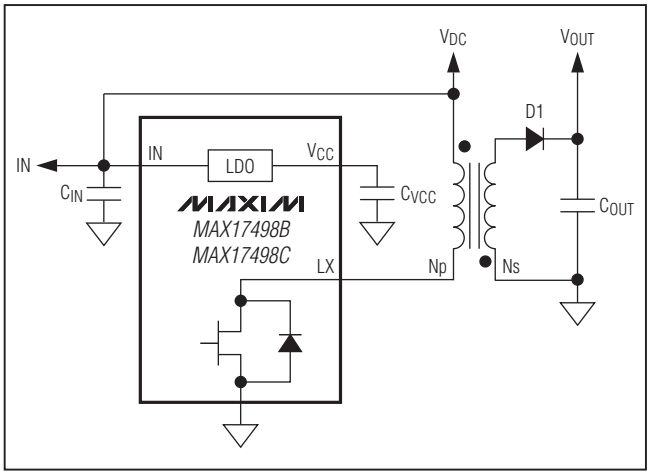


Figure 5. MAX17498B/MAX17498C Typical Startup Circuit with IN Connected Directly to DC Input

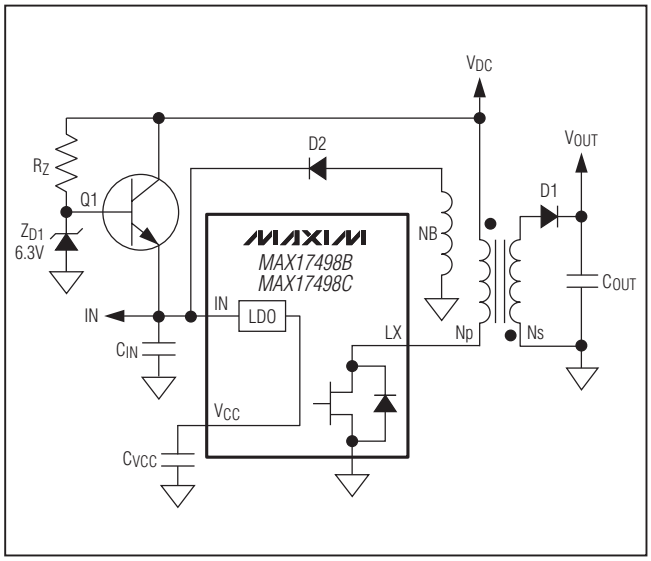


Figure 6. MAX17498B/MAX17498C Typical Startup Circuit with Bias Winding to Turn Off Q1 and Reduce Power Dissipation

The startup capacitor (C_{START}) can be calculated as:

$$C_{START} = \left[I_{IN} + \left(\frac{Q_{GATE} \times f_{SW}}{10^6} \right) \right] \times \frac{t_{SS}}{10} \mu F$$

where I_{IN} is the supply current drawn at the IN pin in mA, Q_{GATE} is the gate charge of the external MOSFET used in nC, f_{SW} is the switching frequency of the converter in kHz, and t_{SS} is the soft-start time programmed for the flyback converter in ms.

Resistors R_{SUM} and R_{ISRC} can be calculated as:

$$R_{SUM} = \frac{V_{START}}{10} M\Omega$$

$$R_{ISRC} = \frac{V_{BEQ1}}{70} M\Omega$$

The IN UVLO wakeup threshold of the MAX17498B/MAX17498C is set to 3.9V (typ) with a 200mV hysteresis, optimized for low-voltage DC-DC applications down to 4.5V. For applications where the input DC voltage is low enough (e.g., 4.5V to 5.5V DC) that the power loss incurred to supply the operating current of the MAX17498B/MAX17498C can be tolerated, the IN pin is directly connected to the DC input, as shown in Figure 5. In the case of higher DC input voltages (e.g., 16V to 32V DC), a startup circuit, such as that shown in Figure 6, can be used to minimize power dissipation in the startup circuit. In this startup scheme, the transistor (Q1) supplies the switching current until a bias winding NB comes up. The resistor (R_Z) can be calculated as:

$$R_Z = 9 \times (V_{INMIN} - 6.3) k\Omega$$

where V_{INMIN} is the minimum input DC voltage.

Programming Soft-Start of the Flyback/Boost Converter (SS)

The soft-start period in the voltage soft-start scheme of the devices can be programmed by selecting the value of the capacitor connected from the SS pin to GND. The capacitor C_{SS} can be calculated as:

$$C_{SS} = 8.13 \times t_{SS} nF$$

where t_{SS} is expressed in ms.

The soft-start period in the current soft-start scheme depends on the load at the output and the soft-start capacitor.

Programming Output Voltage

The devices incorporate a flexible error amplifier that allows regulating to both the positive and negative outputs. The positive output voltage of the converter can be programmed by selecting the correct values for the resistor-divider connected from V_{OUT}, the flyback/boost output to ground, with the midpoint of the divider connected to the EA- pin (Figure 7). With R_B selected in the range of 20kΩ to 50kΩ, R_U can be calculated as:

$$R_U = R_B \times \left[\frac{V_{OUT}}{1.22} - 1 \right] k\Omega$$

where R_B is in kΩ.

The negative output voltage of the converter can be programmed by selecting the correct values for the resistor-divider connected from V_{OUT}, the flyback/boost output to REF with the midpoint of the divider connected to the EA+ pin (Figure 8). With R1 selected in the range of 20kΩ to 50kΩ, R2 can be calculated as:

$$R2 = R1 \times \left[\frac{V_{OUT}}{1.22}\right] k\Omega$$

where R1 is in kΩ.

Current-Limit Programming (LIM)

The devices include a robust overcurrent-protection scheme that protects the device under overload and short-circuit conditions. For the flyback/boost converter, the devices include a cycle-by-cycle peak current limit that turns off the driver whenever the current into the LX pin exceeds an internal limit that is programmed by the resistor connected from the LIM pin to GND. The devices include a runaway current limit that protects the device under high-input-voltage short-circuit conditions when there is insufficient output voltage available to restore the inductor current built up during the on period of the flyback/boost converter. Either eight consecutive occurrences of the peak current-limit event or one occurrence of the runaway current limit trigger a hiccup mode that protects the converter by immediately suspending switching for a period of time (t_{RSTART}). This allows the overload current to decay due to power loss in the converter resistances, load, and the output diode of the flyback/boost converter before soft-start is attempted again. The resistor at the LIM pin for a desired current limit (I_{PK}) can be calculated as:

$$R_{LIM} = 50 \times I_{PK}\ k\Omega$$

where I_{PK} is expressed in amperes.

For a given peak current-limit setting, the runaway current limit is typically 20% higher. The peak current-limit-triggered hiccup operation is disabled until the end of soft-start, while the runaway current-limit-triggered hiccup operation is always enabled.

Programming Slope Compensation (SLOPE)

Since the MAX17498A/MAX17498C operate at a maximum duty cycle of 49%, in theory they do not require slope compensation for preventing subharmonic instability that occurs naturally in continuous-mode peak current-mode-controlled converters operating at duty cycles greater than 50%. In practice, the MAX17498A/MAX17498C require a minimum amount of slope compensation to provide stable, jitter-free operation. The MAX17498A/MAX17498C allow the user to program this default value of slope compensation simply by connecting the SLOPE pin to V_{CC}. It is recommended that discontinuous-mode designs also use this minimum amount of slope compensation to provide noise immunity and jitter-free operation.

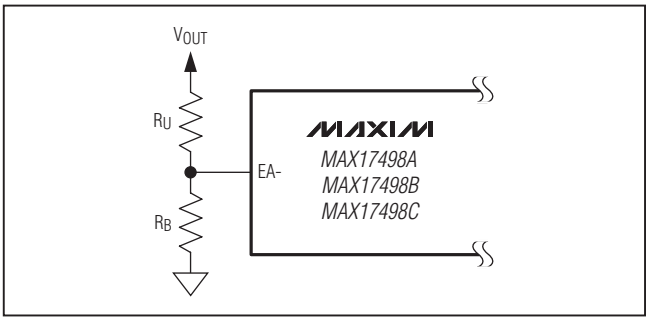


Figure 7. Programming the Positive Output Voltage

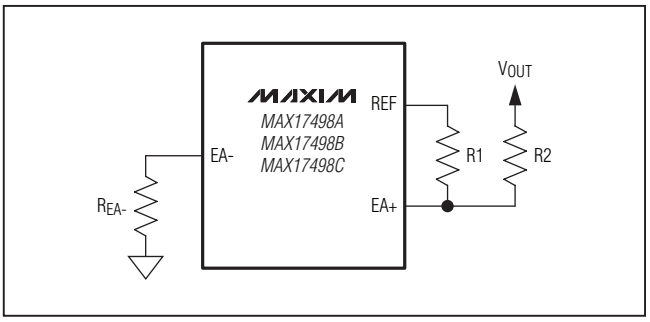


Figure 8. Programming the Negative Output Voltage

The MAX17498B flyback/boost converter can be designed to operate in either discontinuous mode or to enter into the continuous-conduction mode at a specific heavy-load condition for a given DC input voltage. In the continuous-conduction mode, the flyback/boost converter needs slope compensation to avoid subharmonic instability that occurs naturally over all specified load and line conditions in peak current-mode-controlled converters operating at duty cycles greater than 50%. A minimum amount of slope signal is added to the sensed current signal even for converters operating below 50% duty to provide stable, jitter-free operation. The SLOPE pin allows the user to program the necessary slope compensation by setting the value of the resistor (R_{SLOPE}) connected from SLOPE pin to ground.

$$R_{SLOPE} = 0.5 \times S_E\ k\Omega$$

where the slope (S_E) is expressed in millivolts per microsecond.

Error Amplifier, Loop Compensation, and Power-Stage Design of the Flyback/Boost Converter

The flyback/boost converter requires proper loop compensation to be applied to the error-amplifier output to achieve stable operation. The goal of the compensator design is to achieve the desired closed-loop bandwidth and sufficient phase margin at the crossover frequency of the open-loop gain-transfer function of the converter. The error amplifier provided in the devices is a transconductance amplifier. The compensation network used to apply the necessary loop compensation is shown in Figure 9.

The flyback/boost converter can be used to implement the following converters and operating modes:

- Nonisolated flyback converter in discontinuous-conduction mode (DCM flyback)
- Nonisolated flyback converter in continuous-conduction mode (CCM flyback)
- Boost converter in discontinuous-conduction mode (DCM boost)
- Boost converter in continuous-conduction mode (CCM boost)

Calculations for loop-compensation values (R_Z, C_Z, and C_P) for these converter types and design procedures for power-stage components are detailed in the following sections.

DCM Flyback

Primary-Inductance Selection

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is ideally delivered entirely to the output. The maximum primary-inductance value for which the converter remains in discontinuous mode at all operating conditions can be calculated as:

$$L_{PRIMAX} \le \frac{(V_{INMIN} \times D_{MAX})^2 \times 0.4}{(V_{OUT} + V_D) \times I_{OUT} \times f_{SW}}$$

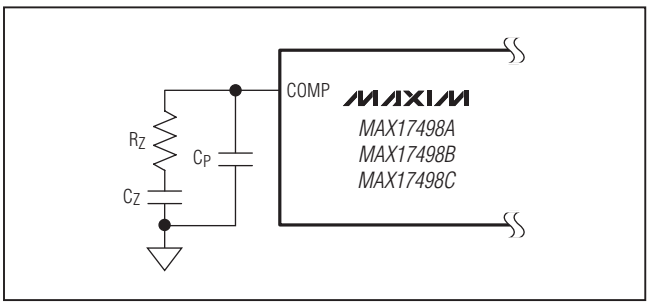


Figure 9. Error-Amplifier Compensation Network

where D_{MAX} is 0.35 for the MAX17498A/MAX17498C and 0.7 for the MAX17498B, V_D is the voltage drop of the output rectifier diode on the secondary winding, and f_{SW} is the switching frequency of the power converter. Choose the primary inductance value to be less than L_{PRIMAX}.

Duty-Cycle Calculation

The accurate value of the duty cycle (D_{NEW}) for the selected primary inductance (L_{PRI}) can be calculated using the following equation:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times (V_{OUT} + V_D) \times I_{OUT} \times f_{SW}}}{V_{INMIN}}$$

Turns-Ratio Calculation (Ns/Np)

Transformer turns ratio (K = Ns/Np) can be calculated as:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{V_{INMIN} \times D_{MAX}}$$

Peak/RMS-Current Calculation

The transformer manufacturer needs RMS current values in the primary and secondary to design the wire diameter for the different windings. Peak current calculations are useful in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current:

$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times f_{SW}}$$

Maximum primary RMS current:

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}}$$

Maximum secondary peak current:

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{K}$$

Maximum secondary RMS current:

$$I_{SECRMS} = I_{PRIPEAK} \times \sqrt{\frac{I_{SECPEAK} \times L_{PRI} \times f_{SW}}{3(V_{OUTF} + V_D)}}$$

For current-limit setting, the peak current can be calculated as:

$$I_{LIM} = I_{PRIPEAK} \times 1.2$$

Primary RCD Snubber Selection

Ideally, the external n-channel MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary

winding during the off period of the nMOSFET. In practice, parasitic inductances and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external nMOSFET. The snubber capacitor can be calculated using the following equation:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^2 \times K^2}{V_{OUT}^2}$$

where L_{LK} is the leakage inductance that can be obtained from the transformer specifications (usually 1% to 2% of the primary inductance).

The power to be dissipated in the snubber resistor is calculated using the following formula:

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{PRIPEAK}^2 \times f_{SW}$$

The snubber resistor can be calculated based on the following equation:

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times K^2}$$

The voltage rating of the snubber diode is:

$$V_{DSNUB} = V_{INMAX} + \left(2.5 \times \frac{V_{OUT}}{K}\right)$$

Output-Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application so that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be 1/10 the switching frequency (f_{SW}). For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore, output-voltage ripple is a function of load current and duty cycle. Use the following equation to calculate the output-capacitor ripple:

$$\Delta V_{COUT} = \frac{D_{NEW} \times \left[I_{PRIPEAK} - \left[K \times I_{OUT}\right]\right]^2}{2 \times I_{PRIPEAK} \times f_{SW} \times C_{OUT}}$$

where I_{OUT} is load current and D_{NEW} is the duty cycle at minimum input voltage.

Input-Capacitor Selection

The MAX17498A is optimized to implement offline AC-DC converters. In such applications, the input capacitor must be selected based on either the ripple due to the rectified line voltage, or based on holdup-time requirements. Holdup time can be defined as the time period over which the power supply should regulate its output voltage from the instant the AC power fails. The MAX17498B/MAX17498C are useful in implementing low-voltage DC-DC applications where the switching-frequency ripple must be used to calculate the input capacitor. In both cases, the capacitor must be sized to meet RMS current requirements for reliable operation.

Capacitor Selection Based on Switching Ripple (MAX17498B/MAX17498C): For DC-DC applications, X7R ceramic capacitors are recommended due to their stability over the operating temperature range. The ESR and ESL of a ceramic capacitor are relatively low, so the ripple voltage is dominated by the capacitive component. For the flyback converter, the input capacitor supplies the current when the main switch is on. Use the following equation to calculate the input capacitor for a specified peak-to-peak input switching ripple (V_{IN_RIP}):

$$C_{IN} = \frac{D_{NEW} \times I_{PRIPEAK}\left[1 - \left(0.5 \times D_{NEW}\right)\right]^2}{2 \times f_{SW} \times V_{IN\_RIP}}$$

Capacitor Selection Based on Rectified Line-Voltage Ripple (MAX17498A): For the flyback converter, the input capacitor supplies the input current when the diode rectifier is off. The voltage discharge (V_{IN_RIP}), due to the input average current, should be within the limits specified:

$$C_{IN} = \frac{0.5 \times I_{PRIPEAK} \times D_{NEW}}{f_{RIPPLE} \times V_{IN\_RIP}}$$

where f_{RIPPLE}, the input AC ripple frequency equal to the supply frequency for half-wave rectification, is two times the AC supply frequency for full-wave rectification.

Capacitor Selection Based on Hold-Up Time Requirements (MAX17498A): For a given output power (P_{HOLDUP}) that needs to be delivered during hold-up time (t_{HOLDUP}), DC bus voltage at which the AC supply fails (V_{INFAIL}), and the minimum DC bus voltage at which the converter can regulate the output voltages (V_{INMIN}), the input capacitor (C_{IN}) is estimated as:

$$C_{IN} = \frac{3 \times P_{HOLDUP} \times t_{HOLDUP}}{(V_{INFAIL}^2 - V_{INMIN}^2)}$$

The input capacitor RMS current can be calculated as:

$$I_{INCRMS} = \frac{0.6 \times V_{INMIN} \times (D_{MAX})^2}{f_{SW} \times L_{PRI}}$$

External MOSFET Selection

MOSFET selection criteria includes the maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage:

$$V_{DSMAX} = V_{INMAX} + \left[\left(\frac{V_{OUT} + V_D}{K}\right) \times 2.5\right]$$

The drain current rating of the external MOSFET is selected to be greater than the worst-case peak current-limit setting.

Secondary-Diode Selection

Secondary-diode-selection criteria includes the maximum reverse voltage, average current in the secondary, reverse recovery time, junction capacitance, and the maximum allowable power dissipation of the package. The voltage stress on the diode is the sum of the output voltage and the reflected primary voltage.

The maximum operating reverse-voltage rating must be higher than the worst-case reverse voltage:

$$V_{SECDIODE} = 1.25 \times (K \times V_{INMAX} + V_{OUT})$$

The current rating of the secondary diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) should be low enough to ensure that the junction temperature is within limits. This necessitates that the diode current rating be in the order of 2 x I_{OUT} to 3 x I_{OUT}. Select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance.

Error-Amplifier Compensation Design

The loop compensation values are calculated as:

$$R_Z = 450 \times \sqrt{\frac{\left[1 + \left[\frac{0.1 \times f_{SW}}{f_P}\right]^2\right] \times V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{SW}}}$$

where:

$$f_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}}$$

$$C_Z = \frac{1}{\pi \times R_Z \times f_P}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

f_{SW} is the switching frequency of the devices and can be obtained from the *Electrical Characteristics* section.

CCM Flyback

Transformer Turns-Ratio Calculation (K = Ns/Np)

The transformer turns ratio can be calculated using the following formula:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{V_{INMIN} \times D_{MAX}}$$

where D_{MAX} is the duty cycle assumed at minimum input (0.35 for MAX17498A/MAX17498C and 0.7 for MAX17498B).

Primary-Inductance Calculation

Calculate the primary inductance based on the ripple:

$$L_{PRI} = \frac{(V_{OUT} + V_D) \times (1 - D_{NOM}) \times K}{2 \times I_{OUT} \times \beta \times f_{SW}}$$

where D_{NOM}, the nominal duty cycle at nominal operating DC input voltage (V_{INNOM}), is given as:

$$D_{NOM} = \frac{(V_{OUT} + V_D) \times K}{[V_{INNOM} + (V_{OUT} + V_D) \times K]}$$

The output current, down to which the flyback converter should operate in CCM, is determined by selection of the fraction ß in the above primary inductance formula. For example, ß should be selected as 0.15 so that the converter operates in CCM down to 15% of the maximum

output load current. Since the ripple in the primary current waveform is a function of duty cycle and is maximum-at-maximum DC input voltage, the maximum (worst-case) load current, down to which the converter operates in CCM, occurs at maximum operating DC input voltage. V_D is the forward drop of the selected output diode at maximum output current.

Peak/RMS-Current Calculation

RMS current values in the primary and secondary are needed by the transformer manufacturer to design the wire diameter for the different windings. Peak current calculations are useful in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current:

$$I_{PRIPEAK} = \left(\frac{I_{OUT} \times K}{1 - D_{MAX}}\right) + \left(\frac{V_{INMIN} \times D_{MAX}}{2 \times L_{PRI} \times f_{SW}}\right)$$

Maximum primary RMS current:

$$I_{PRIRMS} = \sqrt{I_{PRIPEAK}^2 + \frac{\Delta I_{PRI}^2}{3} - (I_{PRIPEAK} \times \Delta I_{PRI})} \times \sqrt{D_{MAX}}$$

where ΔI_{PRI} is the ripple current in the primary current waveform, and is given by:

$$\Delta I_{PRI} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times f_{SW}}\right)$$

Maximum secondary peak current:

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{K}$$

Maximum secondary RMS current:

$$I_{SECRMS} = \sqrt{I_{SECPEAK}^2 + \frac{\Delta I_{SEC}^2}{3} - (I_{SECPEAK} \times \Delta I_{SEC})} \times \sqrt{1 - D_{MAX}}$$

where ΔI_{SEC} is the ripple current in the secondary current waveform, and is given by:

$$\Delta I_{SEC} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times f_{SW} \times K}\right)$$

Current-limit setting the peak current can be calculated as:

$$I_{LIM} = I_{PRIPEAK} \times 1.2$$

Primary RCD Snubber Selection

The design procedure for primary RCD snubber selection is identical to that outlined in the *DCM Flyback* section.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application so that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be less than 1/5 the worst-case (lowest) RHP zero frequency (f_{RHP}). The right half-plane zero frequency is calculated as:

$$f_{ZRHP} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$

For the CCM flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore, the output-voltage ripple is a function of load current and duty cycle. Use the following equation to estimate the output-voltage ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}}$$

Input-Capacitor Selection

The design procedure for input-capacitor selection is identical to that outlined in the *DCM Flyback* section.

External MOSFET Selection

The design procedure for external MOSFET selection is identical to that outlined in the *DCM Flyback* section.

Secondary-Diode Selection

The design procedure for secondary-diode selection is identical to that outlined in the *DCM Flyback* section.

Error-Amplifier Compensation Design

In the CCM flyback converter, the primary inductance and the equivalent load resistance introduces a right half-plane zero at the following frequency:

$$f_{ZRHP} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$

The loop-compensation values are calculated as:

$$R_Z = \frac{200 \times I_{OUT}}{(1-D_{MAX})} \times \sqrt{1+\left[\frac{f_{RHP}}{5 \times f_P}\right]^2}$$

where f_P, the pole due to output capacitor and load, is given by:

$$f_P = \frac{(1+D_{MAX}) \times I_{OUT}}{2 \times \pi \times C_{OUT} \times V_{OUT}}$$

The above selection sets the loop-gain crossover frequency (f_C, where the loop gain equals 1) equal to 1/5 the right half-plane zero frequency:

$$f_C \le \frac{f_{ZRHP}}{5}$$

With the control-loop zero placed at the load pole frequency:

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P}$$

With the high-frequency pole placed at 1/2 the switching frequency:

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

DCM Boost

In a DCM boost converter, the inductor current returns to zero in every switching cycle. Energy stored during the on time of the main switch is delivered entirely to the load in each switching cycle.

Inductance Selection

The design procedure starts with calculating the boost converter's input inductor so that it operates in DCM at all operating line and load conditions. The critical inductance required to maintain DCM operation is calculated as:

$$L_{IN} \le \frac{\left[(V_{OUT} - V_{INMIN}) \times V_{INMIN}^2\right] \times 0.4}{I_{OUT} \times V_{OUT}^2 \times f_{SW}}$$

where V_{INMIN} is the minimum input voltage.

Peak/RMS-Current Calculation

To set the current limit, the peak current in the inductor can be calculated as:

$$I_{LIM} = I_{PK} \times 1.2$$

where I_{PK} is given by:

$$I_{PK} = \sqrt{\left[\frac{2 \times (V_{OUT} - V_{INMIN}) \times I_{OUT}}{L_{INMIN} \times f_{SWMIN}}\right]}$$

L_{INMIN} is the minimum value of the input inductor, taking into account tolerance and saturation effects. f_{SWMIN} is the minimum switching frequency for the MAX17498B from the *Electrical Characteristics* section.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application so that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be 1/10 the switching frequency (f_{SW}). For the boost converter, the output capacitor supplies the load current when the main switch is on, and therefore, the output-voltage ripple is a function of duty cycle and load current. Use the following equation to calculate the output-capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times L_{IN} \times I_{PK}}{V_{INMIN} \times C_{OUT}}$$

Input-Capacitor Selection

The value of the required input ceramic capacitor can be calculated based on the ripple allowed on the input DC bus. The input capacitor should be sized based on the RMS value of the AC current handled by it. The calculations are:

$$C_{IN} = \left[\frac{3.75 \times I_{OUT}}{V_{INMIN} \times f_{SWMIN} \times (1 - D_{MAX})}\right]$$

The capacitor RMS can be calculated as:

$$I_{CIN\_RMS} = \frac{I_{PK}}{2 \times \sqrt{3}}$$

Error-Amplifier Compensation Design

The loop-compensation values for the error amplifier can now be calculated as:

$$C_Z = \frac{G_{DC} \times G_M \times 10}{2 \times \pi \times f_{SW}} = (G_{DC} \times 10)\ nF$$

where G_{DC}, the DC gain of the power stage, is given as:

$$G_{DC} = \sqrt{\frac{8 \times (V_{OUT} - V_{INMIN}) \times f_{SW} \times V_{OUT}^2 \times L_{IN}}{(2V_{OUT} - V_{INMIN})^2 \times I_{OUT}}}$$

$$R_Z = \frac{V_{OUT} \times C_{OUT} \times (V_{OUT} - V_{INMIN})}{I_{OUT} \times C_Z \times (2V_{OUT} - V_{INMIN})}$$

where V_{INMIN} is the minimum operating input voltage and I_{OUT} is the maximum load current:

$$C_P = \frac{C_{OUT} \times ESR}{R_Z}$$

Slope Compensation

In theory, the DCM boost converter does not require slope compensation for stable operation. In practice, the converter needs a minimum amount of slope for good noise immunity at very light loads. The minimum slope is set for the devices by connecting the SLOPE pin to the V_{CC} pin.

Output-Diode Selection

The voltage rating of the output diode for the boost converter ideally equals the output voltage of the boost converter. In practice, parasitic inductances and capacitances in the circuit interact to produce voltage overshoot during the turn-off transition of the diode that occurs when the main switch turns on. The diode rating should therefore be selected with the necessary margin to accommodate this extra voltage stress. A voltage rating of 1.3 x V_{OUT} provides the necessary design margin in most cases.

The current rating of the output diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) is low enough to ensure that the junction temperature is within limits. This necessitates that the diode current rating be in the order of 2 x I_{OUT} to 3 x I_{OUT}. Select fast-recovery diodes with a recovery time less than 50ns or Schottky diodes with low junction capacitance.

Internal MOSFET RMS Current Calculation

The voltage stress on the internal MOSFET, whose drain is connected to LX, ideally equals the sum of the output voltage and the forward drop of the output diode. In practice, voltage overshoot and ringing occur due to the action of circuit parasitic elements during the turn-off transition. The maximum rating of the devices' internal n-channel MOSFET is 65V, making it possible to design boost converters with output voltages up to 48V and sufficient margin for voltage overshoot and ringing. The RMS current into LX is useful in estimating the conduction loss in the internal nMOSFET, and is given as:

$$I_{LX\_RMS} = \sqrt{\frac{I_{PK}^3 \times L_{INS} \times f_{SW}}{3 \times V_{INMIN}}}$$

where I_{PK} is the peak current calculated at the lowest operating input voltage (V_{INMIN}).

CCM Boost

In a CCM boost converter, the inductor current does not return to zero during a switching cycle. Since the MAX17498B implements a nonsynchronous boost converter, the inductor current enters DCM operation at load currents below a critical value equal to 1/2 the peak-to-peak ripple in the inductor current.

Inductor Selection

The design procedure starts with calculating the boost converter's input inductor at nominal input voltage for a ripple in the inductor current equal to 30% of the maximum input current:

$$L_{IN} = \frac{V_{IN} \times D \times (1 - D)}{0.3 \times I_{OUT} \times f_{SW}}$$

where D is the duty cycle calculated as:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D}$$

V_D is the voltage drop across the output diode of the boost converter at maximum output current.

Peak/RMS-Current Calculation

To set the current limit, the peak current in the inductor and internal nMOSFET can be calculated as:

$$I_{PK} = \left[\frac{V_{OUT} \times D_{MAX} \times (1 - D_{MAX})}{L_{INMIN} \times f_{SWMIN}} + \frac{I_{OUT}}{(1 - D)}\right] \times 1.2 \text{ for } D_{MAX} \geq 0.5$$

$$I_{PK} = \left[\frac{0.25 \times V_{OUT}}{L_{INMIN} \times f_{SWMIN}} + \frac{I_{OUT}}{(1 - D)}\right] \times 1.2 \text{ for } D_{MAX} \geq 0.5$$

D_{MAX}, the maximum duty cycle, is obtained by substituting the minimum input operating voltage (V_{INMIN}) in the equation above for duty cycle. L_{INMIN} is the minimum value of the input inductor taking into account tolerance and saturation effects. f_{SWMIN} is the minimum switching frequency for the MAX17498B from the *Electrical Characteristics* section.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as:

$$C_{OUTF} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be 1/10 the switching frequency (f_{SW}). For the boost converter, the output capacitor supplies the load current when the main switch is on, and therefore, the output-voltage ripple is a function of duty cycle and load current. Use the following equation to calculate the output-capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times D_{MAX}}{C_{OUT} \times f_{SW}}$$

Input-Capacitor Selection

The input ceramic capacitor value required can be calculated based on the ripple allowed on the input DC bus. The input capacitor should be sized based on the RMS value of the AC current handled by it. The calculations are:

$$C_{IN} = \left[\frac{3.75 \times I_{OUT}}{V_{INMIN} \times f_{SW} \times (1 - D_{MAX})}\right]$$

The input-capacitor RMS current can be calculated as:

$$I_{CIN\_RMS} = \frac{\Delta I_{LIN}}{2 \times \sqrt{3}}$$

where:

$$\Delta I_{LIN} = \left[\frac{V_{OUT} \times D_{MAX} \times (1 - D_{MAX})}{L_{INMIN} \times f_{SWMIN}}\right] \text{ for } D_{MAX} < 0.5$$

$$\Delta I_{LIN} = \left[\frac{0.25 \times V_{OUT}}{L_{INMIN} \times f_{SWMIN}}\right] \text{ for } D_{MAX} \geq 0.5$$

Error-Amplifier Compensation Design

The loop-compensation values for the error amplifier can now be calculated as:

$$R_Z = \frac{203 \times {V_{OUT}}^2 \times C_{OUT} \times (1 - D_{MAX})}{I_{OUTMAX} \times L_{IN}}$$

where I_{OUTMAX} is the maximum load current:

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{2 \times I_{OUTMAX} \times R_Z}$$

$$C_P = \frac{1}{\pi \times f_{SW} \times R_Z}$$

Slope-Compensation Ramp

The slope required to stabilize the converter at duty cycles greater than 50% can be calculated as:

$$S_E = \frac{0.41 (V_{OUT} - V_{INMIN})}{L_{IN}} \text{ V per } \mu s$$

where L_{IN} is in µH.

Output-Diode Selection

The design procedure for output-diode selection is identical to that outlined in the *DCM Boost* section.

Internal MOSFET RMS Current Calculation

The voltage stress on the internal MOSFET, whose drain is connected to LX, ideally equals the sum of the output voltage and the forward drop of the output diode. In practice, voltage overshoot and ringing occur due to the action of circuit parasitic elements during the turn-off transition. The maximum rating of the internal n-channel MOSFET of the devices is 65V, making it possible to design boost converters with output voltages up to 48V and sufficient margin for voltage overshoot and ringing. The RMS current into LX is useful in estimating the conduction loss in the internal nMOSFET, and is given as:

$$I_{LXRMS} = \frac{I_{OUT} \times \sqrt{D_{MAX}}}{(1 - D_{MAX})}$$

where D_{MAX} is the duty cycle at the lowest operating input voltage and I_{OUT} is the maximum load current.

Thermal Considerations

It should be ensured that the junction temperature of the devices does not exceed +125°C under the operating conditions specified for the power supply. The power dissipated in the devices to operate can be calculated using the following equation:

$$P_{IN} = V_{IN} \times I_{IN}$$

where V_{IN} is the voltage applied at the IN pin and I_{IN} is operating supply current.

The internal n-channel MOSFET experiences conduction loss and transition loss when switching between on and off states. These losses are calculated as:

$$P_{CONDUCTION} = I_{LXRMS}^2 \times R_{DSONLX}$$

$$P_{TRANSITION} = 0.5 \times V_{INMAX} \times I_{PK} \times (t_R + t_F) \times f_{SW}$$

where t_R and t_F are the rise and fall times of the internal nMOSFET in CCM operation. In DCM operation, since the switch current starts from zero, only t_F exists and the transition-loss equation changes to:

$$P_{TRANSITION} = 0.5 \times V_{INMAX} \times I_{PK} \times t_F \times f_{SW}$$

Additional loss occurs in the system in every switching cycle due to energy stored in the drain-source capacitance of the internal MOSFET being lost when the MOSFET turns on and discharges the drain-source capacitance voltage to zero. This loss is estimated as:

$$P_{CAP} = 0.5 \times C_{DS} \times V_{DSMAX}^2 \times f_{SW}$$

The total power loss in the devices can be calculated from the following equation:

$$P_{LOSS} = P_{IN} + P_{CONDUCTION} + P_{TRANSITION} + P_{CAP}$$

The maximum power that can be dissipated in the devices is 1666mW at +70°C temperature. The power-dissipation capability should be derated as the temperature rises above +70°C at 21mW/°C. For a multilayer board, the thermal-performance metrics for the package are given below:

$$\theta_{JA} = 48°C / W$$

$$\theta_{JC} = 10°C / W$$

The junction-temperature rise of the devices can be estimated at any given maximum ambient temperature (T_{AMAX}) from the following equation:

$$T_{JMAX} = T_{AMAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the devices is maintained at a given temperature (T_{EPMAX}) by using proper heatsinks, then the junction-temperature rise of the devices can be estimated at any given maximum ambient temperature from the following equation:

$$T_{JMAX} = T_{EPMAX} + (\theta_{JC} \times P_{LOSS})$$

Layout, Grounding and Bypassing

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency switching power converters. This implies that the loop areas for forward and return pulsed currents in various parts of the circuit should be minimized. Additionally, small-current loop areas reduce radiated EMI. Similarly, the heatsink of the main MOSFET presents a dV/dt source, and therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least noisy section of the power ground plane, typically the return of the input filter capacitor. The negative terminal of the filter capacitor, ground return of the power switch, and current-sensing resistor must be close together. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation. For a sample layout that ensures first-pass success, refer to the MAX17498B evaluation kit layout available at **www.maxim-ic.com**.

For universal AC input designs, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Typical Application Circuits

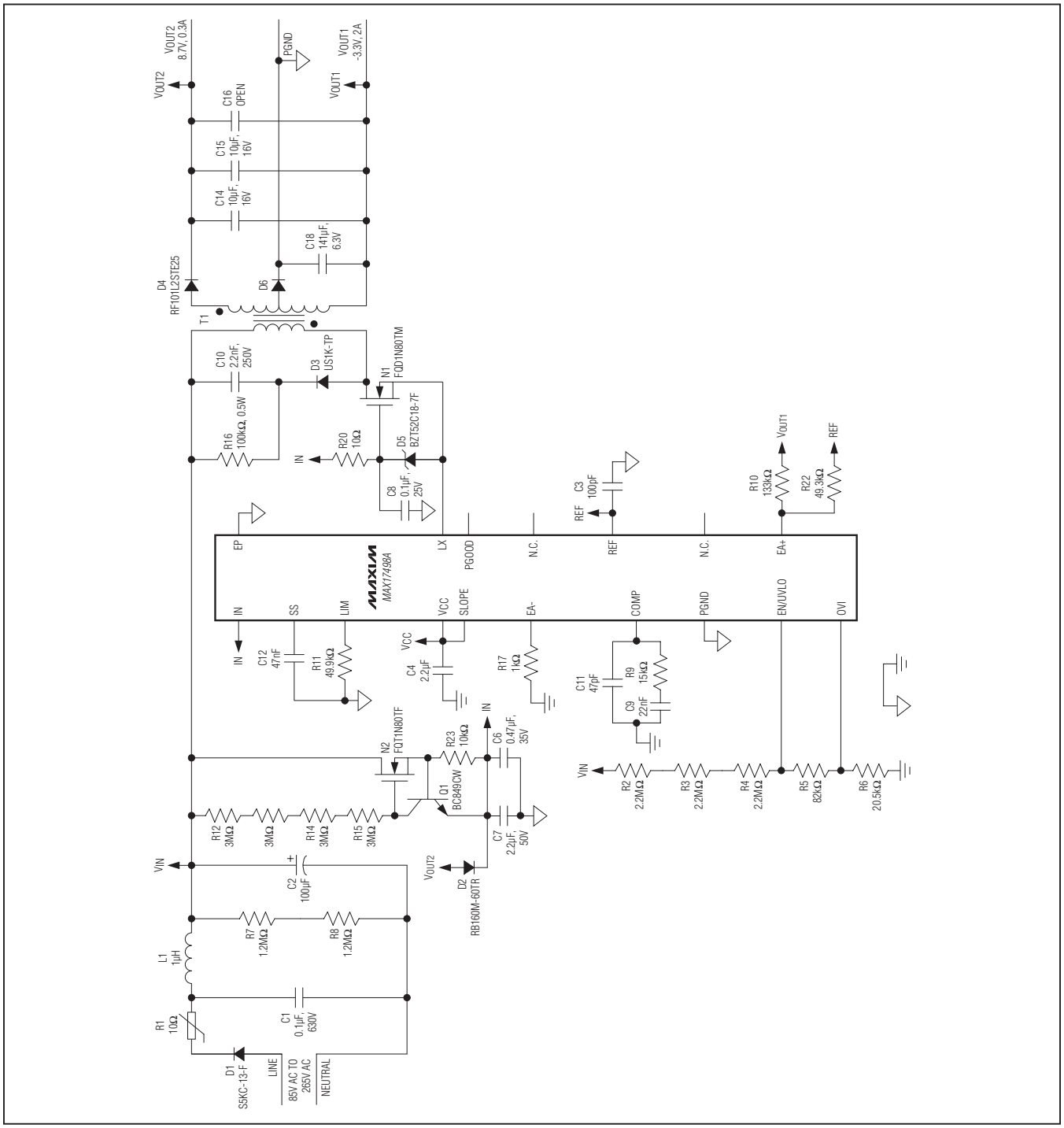


Figure 10. MAX17498A Nonisolated Multiple-Output AC-DC Power Supply

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications

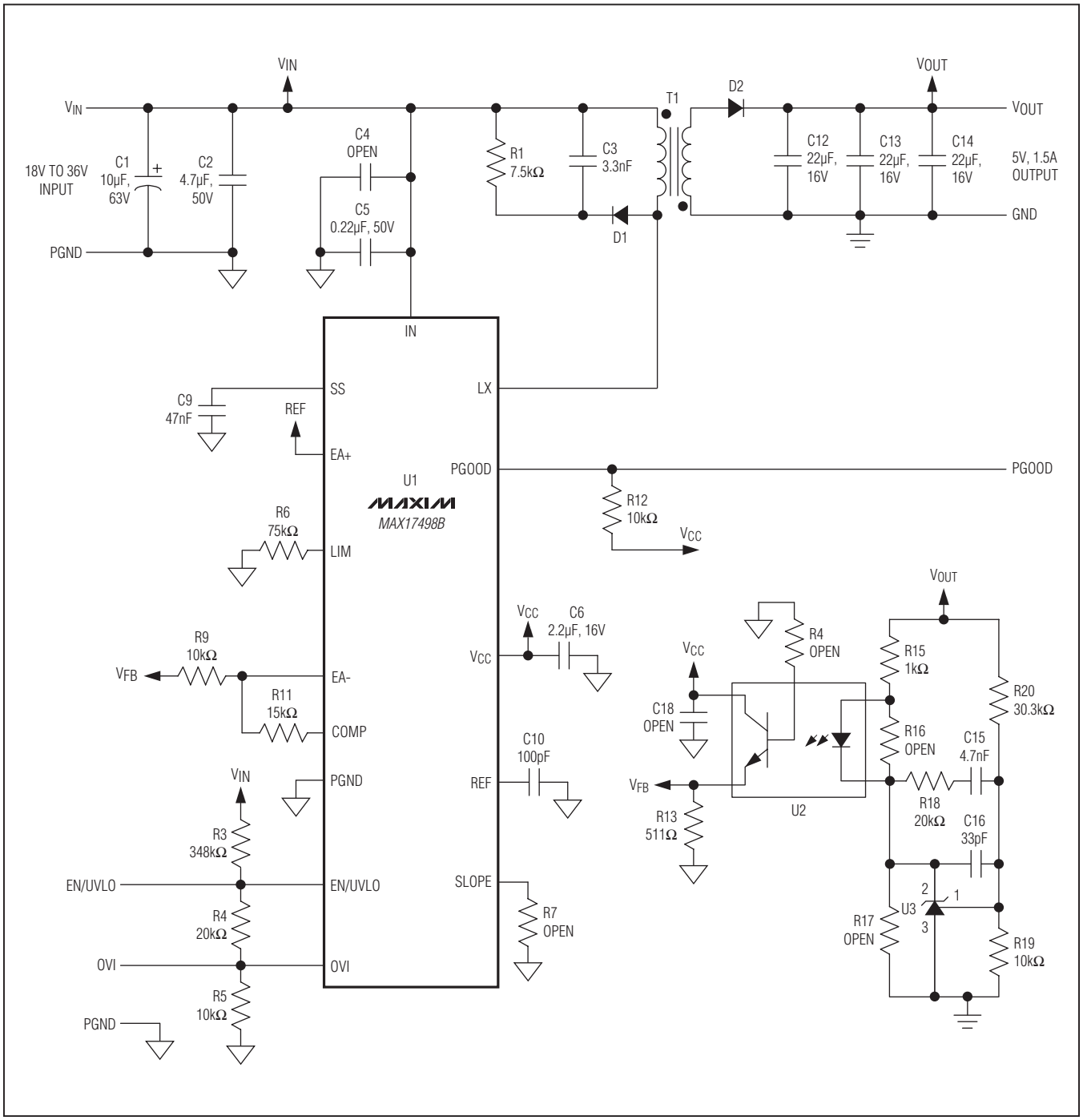


Figure 11. MAX17498B Isolated DC-DC Power Supply

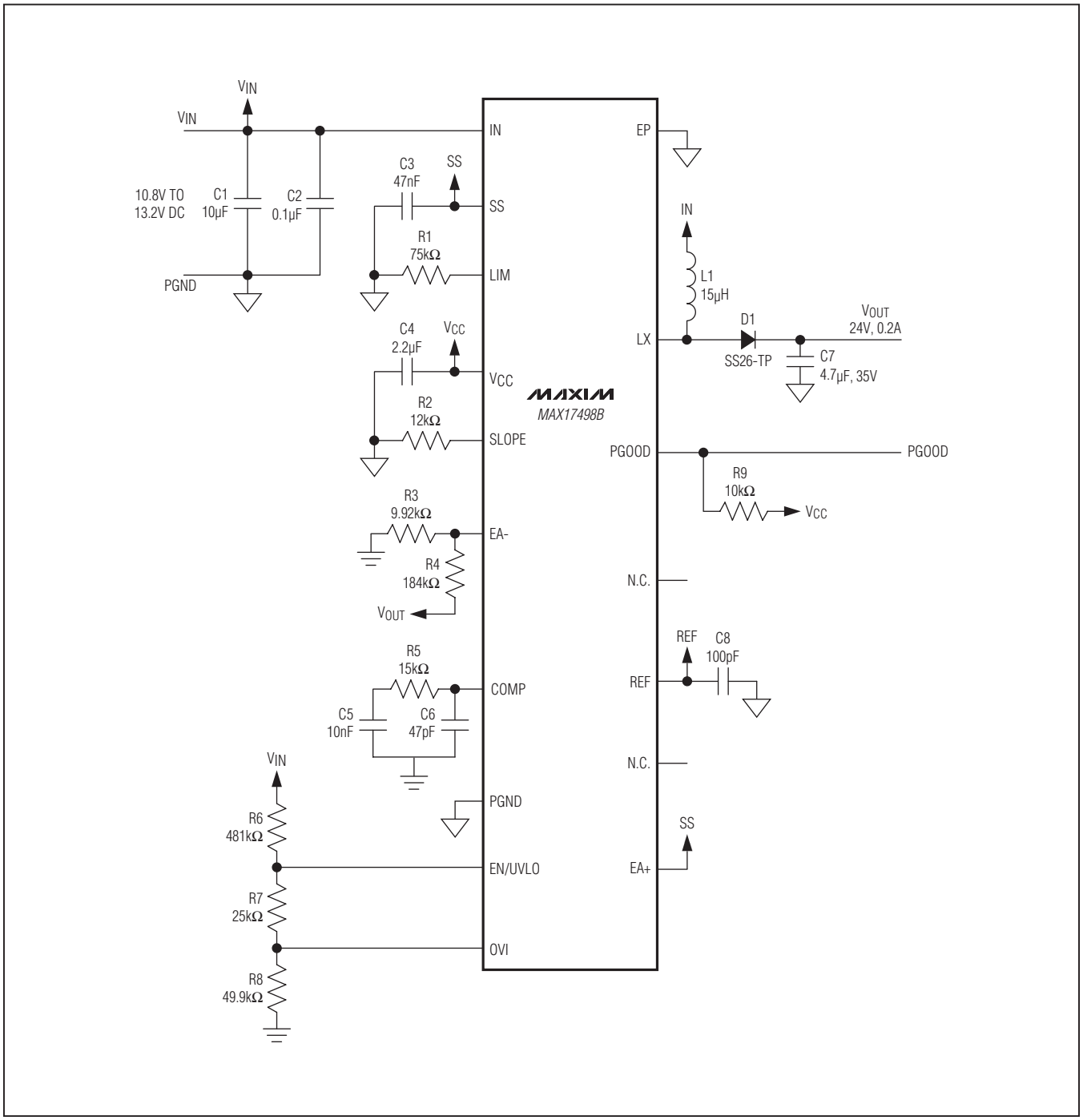


Figure 12. MAX17498B Boost Power Supply

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX17498AATE+	-40°C to +125°C	16 TQFN-EP*	250kHz, Offline Flyback Converter
MAX17498BATE+	-40°C to +125°C	16 TQFN-EP*	500kHz, Low-Voltage DC-DC Flyback/Boost Converter
MAX17498CATE+	-40°C to +125°C	16 TQFN-EP*	250kHz, Low-Voltage DC-DC Flyback Converter

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+5	**21-0136**	**90-0032**

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	3/12	Removed future product references for MAX17498B and MAX17498C	27

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications