

## Characteristics

Parameter	Rating	Units
Blocking Voltage	400	V <sub>P</sub>
Load Current, T <sub>A</sub> =25°C:		
With 5°C/W Heat Sink	3.35	A <sub>rms</sub>
No Heat Sink	1.35	
On-Resistance	0.85	Ω
R <sub>θJC</sub>	0.35	°C/W

## Features

- 3.35A<sub>rms</sub> Load Current with 5°C/W Heat Sink
- Low 0.85Ω On-Resistance
- 400V<sub>P</sub> Blocking Voltage
- 2500V<sub>rms</sub> Input/Output Isolation
- Low Thermal Resistance (0.35 °C/W)
- Electrically Non-conductive Thermal Pad for Heat Sink Applications
- Low Drive Power Requirements
- Arc-Free With No Snubbing Circuits
- No EMI/RFI Generation
- Machine Insertable, Wave Solderable

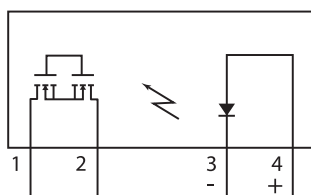
## Applications

- Industrial Controls / Motor Control
- Robotics
- Medical Equipment—Patient/Equipment Isolation
- Instrumentation
  - Multiplexers
  - Data Acquisition
  - Electronic Switching
  - I/O Subsystems
  - Meters (Watt-Hour, Water, Gas)
- Transportation Equipment
- Aerospace/Defense

## Approvals

- UL 508 Recognized Component: File E69938

## Pin Configuration



## Description

Clare and IXYS have combined to bring OptoMOS® technology, reliability and compact size to a new family of high power Solid State Relays.

As part of this family, the CPC1967 single-pole normally open (1-Form-A) Solid State Power Relay is rated for up to 3.35A<sub>rms</sub> continuous load current with a 5°C/W heat sink.

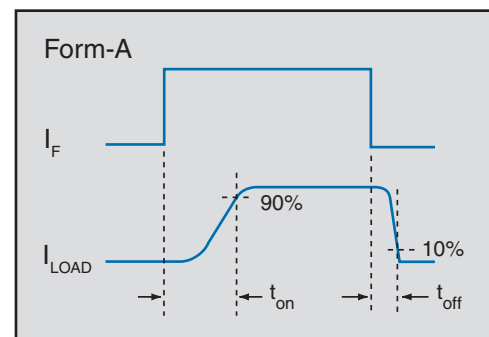
The CPC1967 employs optically coupled MOSFET technology to provide 2500V<sub>rms</sub> of input to output isolation. The output, constructed with efficient MOSFET switches and photovoltaic die, uses Clare's patented OptoMOS architecture while the input, a highly efficient GaAlAs infrared LED, provides the optically coupled control. The combination of low on-resistance and high load current handling capability makes this relay suitable for a variety of high performance switching applications.

The unique i4-PAC package pioneered by IXYS enables Solid State Relays to achieve the highest load current and power ratings. This package features a unique IXYS process where the silicon chips are soft soldered onto the Direct Copper Bond (DCB) substrate instead of the traditional copper leadframe. The DCB ceramic, the same substrate used in high power modules, not only provides 2500V<sub>rms</sub> isolation, but also very low thermal resistance (0.35 °C/W).

## Ordering Information

Part	Description
CPC1967J	i4-PAC Package (25 per tube)

## Switching Characteristics



## 1 Specifications

### 1.1 Absolute Maximum Ratings @ 25°C

Symbol	Ratings	Units
Blocking Voltage	400	V <sub>P</sub>
Reverse Input Voltage	5	V
Input Control Current	100	mA
Peak (10ms)	1	A
Input Power Dissipation	150	mW
Isolation Voltage, Input to Output	2500	V <sub>rms</sub>
Operational Temperature	-40 to +85	°C
Storage Temperature	-40 to +125	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

### 1.2 Electrical Characteristics @ 25°C

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
<b>Output Characteristics</b>						
Load Current <sup>1</sup>						
Peak	t <sub>≤</sub> 10ms	I <sub>L</sub>	-	-	15	A <sub>P</sub>
Continuous	No Heat Sink				1.35	A <sub>rms</sub>
Continuous	T <sub>C</sub> =25°C				13.15	
Continuous	T <sub>C</sub> =99°C				1.5	
On-Resistance <sup>2</sup>	I <sub>F</sub> =10mA, I <sub>L</sub> =1A	R <sub>ON</sub>	-	0.7	0.85	Ω
Off-State Leakage Current	V <sub>L</sub> =400V <sub>P</sub>	I <sub>LEAK</sub>	-	-	1	μA
Switching Speeds						
Turn-On	I <sub>F</sub> =10mA, V <sub>L</sub> =10V	t <sub>on</sub>	-	5	20	ms
Turn-Off		t <sub>off</sub>	-	0.13	5	
Output Capacitance	V <sub>L</sub> =25V, f=1MHz	C <sub>out</sub>	-	470	-	pF
<b>Input Characteristics</b>						
Input Control Current <sup>3</sup>	I <sub>L</sub> =1A	I <sub>F</sub>	-	-	10	mA
Input Dropout Current	-	I <sub>F</sub>	0.6	-	-	mA
Input Voltage Drop	I <sub>F</sub> =5mA	V <sub>F</sub>	0.9	1.2	1.4	V
Reverse Input Current	V <sub>R</sub> =5V	I <sub>R</sub>	-	-	10	μA
<b>Input/Output Characteristics</b>						
Capacitance, Input-to-Output	-	C <sub>I/O</sub>	-	1	-	pF

<sup>1</sup> Higher load currents possible with proper heat sinking.

<sup>2</sup> Measurement taken within 1 second of on-time.

<sup>3</sup> For applications requiring high temperature operation (T<sub>C</sub> > 60°C) a LED drive current of 20mA is recommended.

## 2 Thermal Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Thermal Resistance (Junction to Case)	-	$R_{\theta JC}$	-	-	0.35	°C/W
Thermal Resistance (Junction to Ambient)	Free Air	$R_{\theta JA}$	-	33	-	°C/W
Junction Temperature (Operating)	-	$T_J$	-40	-	100	°C

### 2.1 Thermal Management

Device high current characterization was performed using Kunze heat sink KU 1-159, phase change thermal interface material KU-ALC 5, and transistor clip KU 4-499/1. This combination provided an approximate junction-to-ambient thermal resistance of 12.5°C/W.

### 2.2 Heat Sink Calculation

Higher load currents are possible by using lower thermal resistance heat sink combinations.

#### Heat Sink Rating

$$R_{\theta CA} = \frac{(T_J - T_A) I_{L(99)}^2}{I_L^2 \cdot P_{D(99)}} - R_{\theta JC}$$

$T_J$  = Junction Temperature (°C),  $T_J \leq 100^\circ\text{C}$  \*

$T_A$  = Ambient Temperature (°C)

$I_{L(99)}$  = Load Current with Case Temperature @ 99°C ( $A_{DC}$ )

$I_L$  = Desired Operating Load Current ( $A_{DC}$ ),  $I_L \leq I_{L(MAX)}$

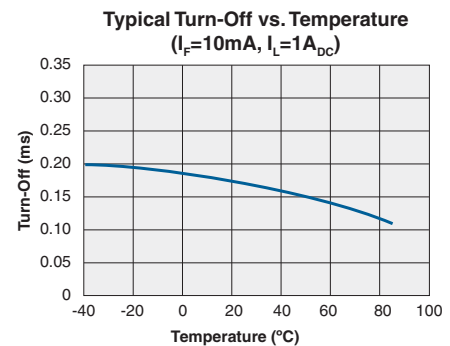
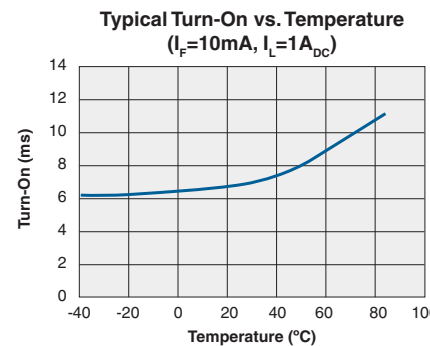
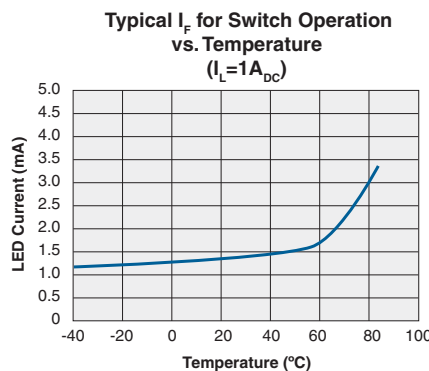
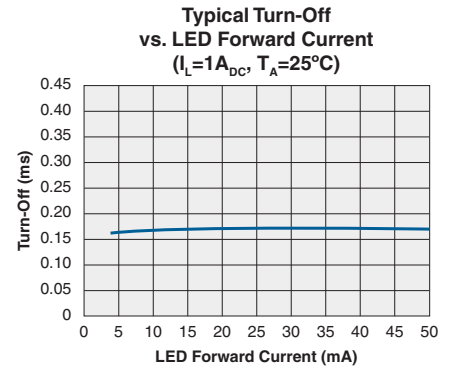
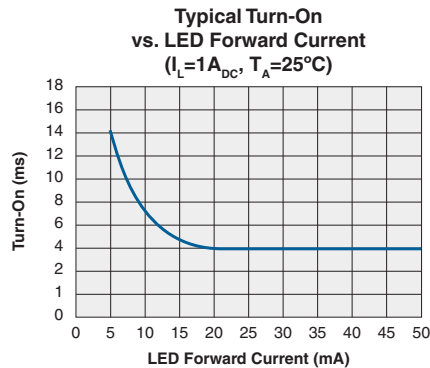
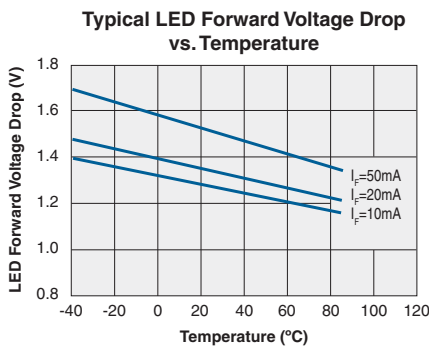
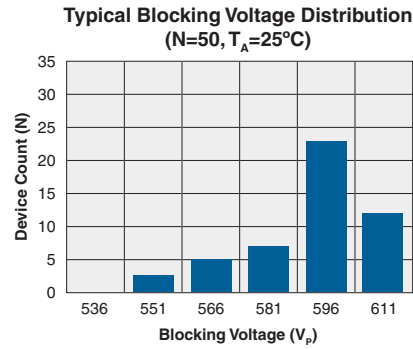
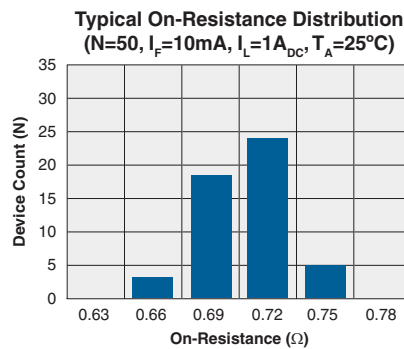
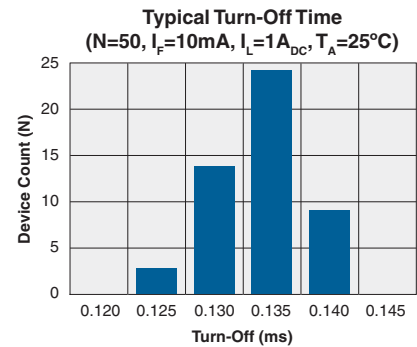
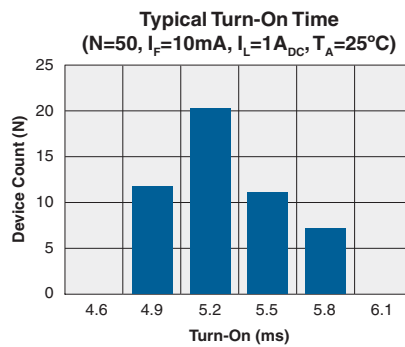
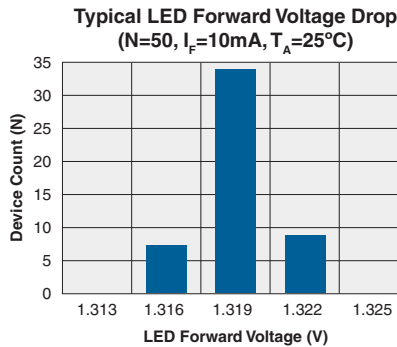
$R_{\theta JC}$  = Thermal Resistance, Junction to Case (°C/W) = 0.35°C/W

$R_{\theta CA}$  = Thermal Resistance of Heat Sink & Thermal Interface Material, Case to Ambient (°C/W)

$P_{D(99)}$  = Maximum power dissipation with case temperature held at 99°C = 2.86W

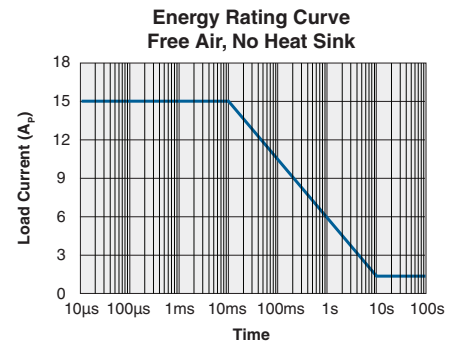
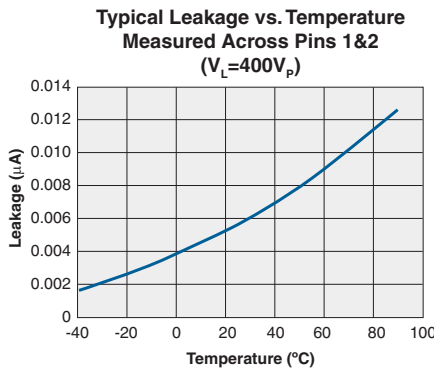
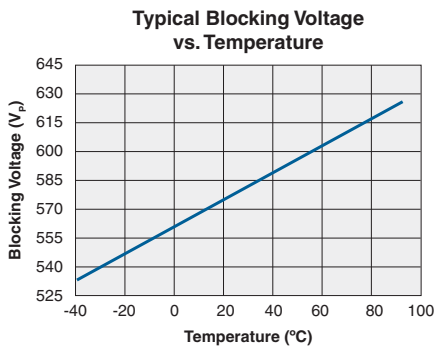
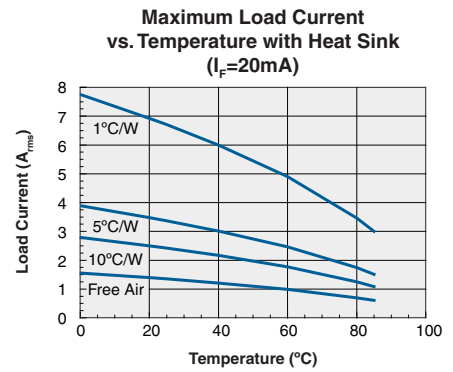
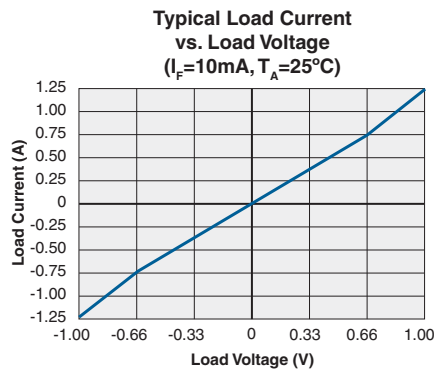
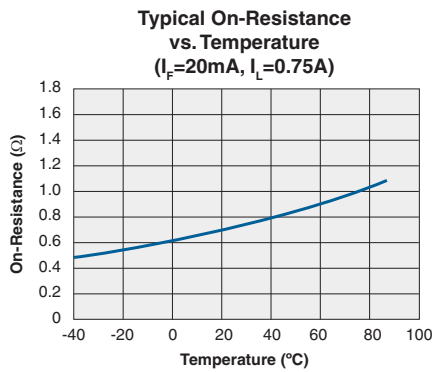
\* Elevated junction temperature reduces semiconductor lifetime.

### 3 Performance Data



Unless otherwise specified, all performance data was acquired without the use of a heat sink.

The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.



Unless otherwise specified, all performance data was acquired without the use of a heat sink.

The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

## 4 Manufacturing Information

### 4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC1967J	MSL 1

### 4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

### 4.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

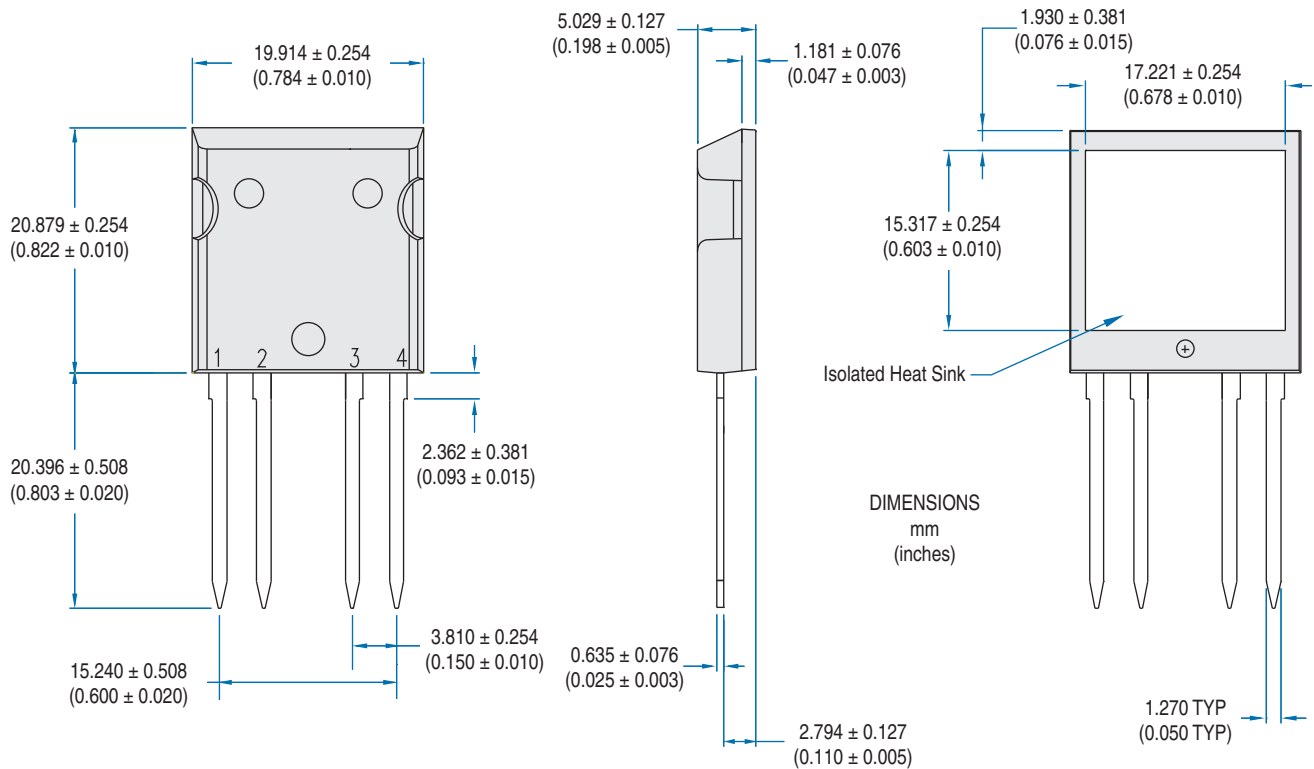
Device	Maximum Temperature x Time
CPC1967J	245°C for 30 seconds

### 4.4 Board Wash

Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since Clare employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake may be necessary if a wash is used after solder reflow processes. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.



**4.5 Mechanical Dimensions**



NOTE: Back-side heat sink meets  $2500V_{rms}$  isolation to the pins.

**For additional information please visit our website at: [www.clare.com](http://www.clare.com)**

Clare, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses nor indemnity are expressed or implied. Except as set forth in Clare's Standard Terms and Conditions of Sale, Clare, Inc. assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

The products described in this document are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of Clare's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. Clare, Inc. reserves the right to discontinue or make changes to its products at any time without notice.

Specification: DS-CPC1967-R05  
©Copyright 2011, Clare, Inc.  
All rights reserved. Printed in USA.  
1/7/2011