Full Bridge MOSFET/IGBT Driver up to 600V

1. Functional Description of the AMG-DF102

The AMG-DF102 is a high voltage MOSFET and IGBT driver with two dependent high and low side output channels for Full-Bridge applications. The IC AMG-DF102 has an additional driver in high side configuration to drive a buck converter.

CMOS and TTL compatible input levels. Logic inputs are CMOS Schmitt-triggered with pull-down resistors.

The floating high side outputs are designed for bootstrap operation so to drive an N-channel power MOSFET or IGBT in high side configuration.

During start up the input ENQ need to be tied to VCC to pull the driver outputs low. With ENQ being pulled low, the device is enabled. This protects against unwanted behaviour of the power stage during the start up process, when the supply voltage is rising.

2. Features

- ❑ Logic supply range from 12 to 15V
- ❑ CMOS Schmitt-triggered input logic with pull-down
- ❑ Internally inserted dead time
- ❑ High side output follows corresponding input
- ❑ Floating high side outputs designed for bootstrap operation
- ❑ Enable input turns off all outputs
- ❑ Under-voltage detection for all outputs
- ❑ Temperature range –25°C to 85°C
- ❑ Package SOP24

3. Application

The AMG-DF102 is suitable for High Voltage Power Supplies, Motor Controls, Inverters, Battery Chargers and Lamp Ballasts.

3.1. Example Application Drawing

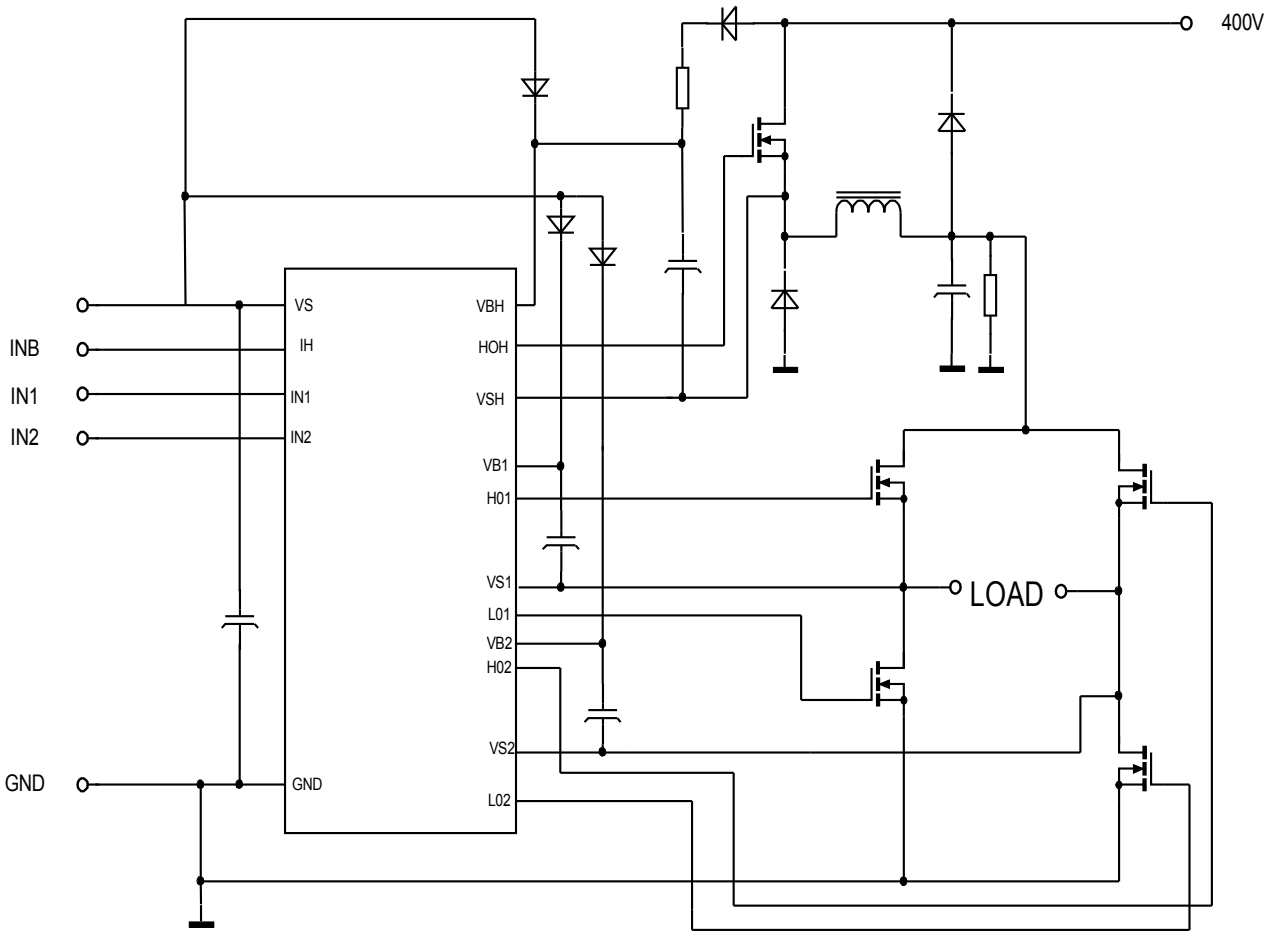


Figure 1: Please insert a clear example application drawing here.

3.2. Application Notes

Transistors, bootstrap diodes and caps physically need to be placed as close as possible to the IC. Via's and 90º trace curves should be avoided. For best performance the distance between the transistors, bootstrap diodes and caps - and the IC should be kept under 1cm, traces to the transistors should be straight and min. 1mm wide, if needed only 45º trace curves. Bootstrap diodes need to be fast switching diodes. Bootstrap capacitors need to have low ESR. Traces to/from the bootstrap diodes and caps should be min. 1mm wide, as short as possible and only 45º curves used.

Additional information may be found in Application Note: AMG-AN-DF102

Table of Contents

4. Block Diagram

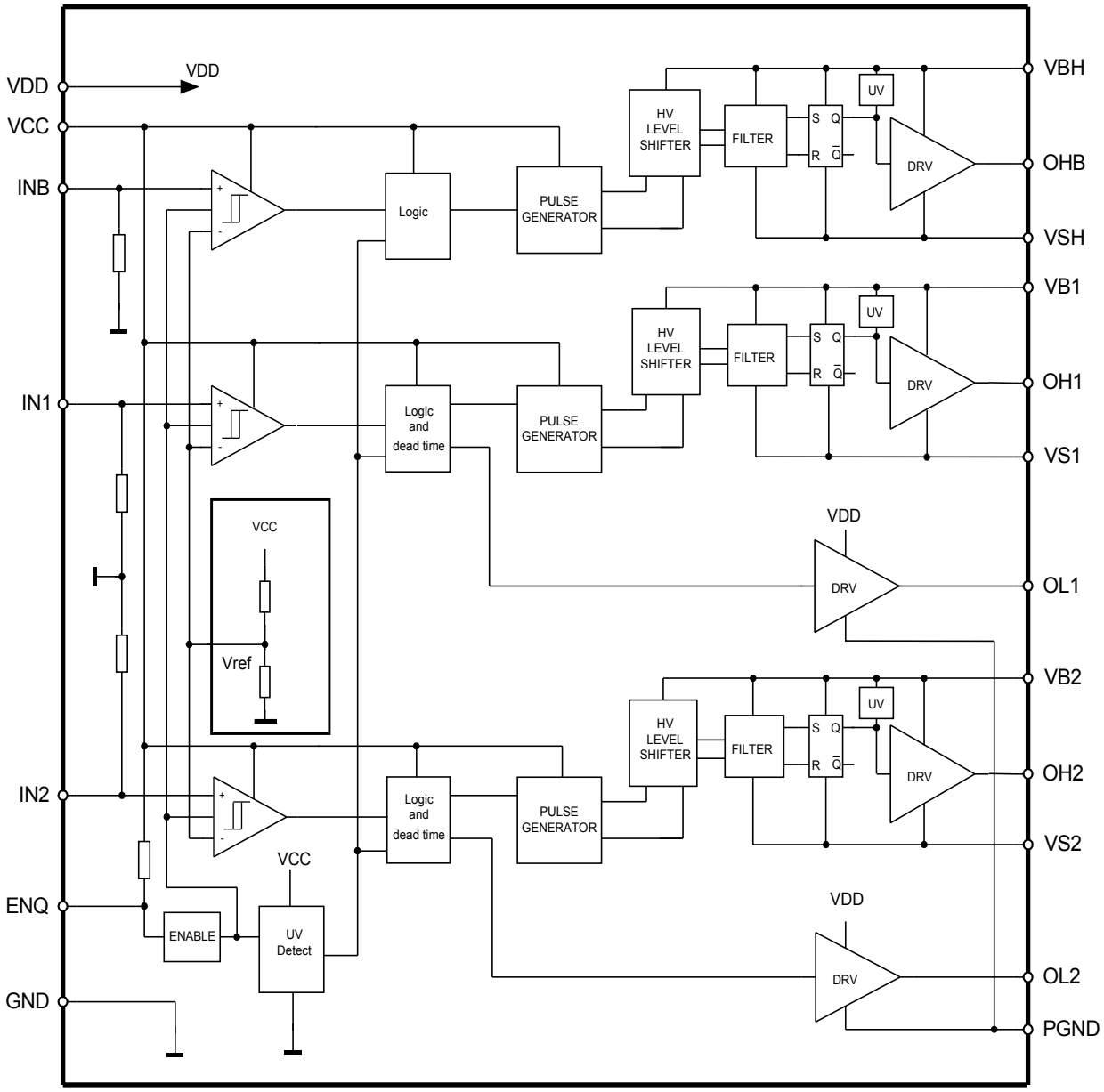


Figure 2: Block Diagram

5. Block Descriptions

5.1. Voltage Divider VCC

- Internal reference voltage for logic inputs (connection to INB, IN1, IN2).

5.2. Input Enable

- Enables the digital inputs and the UV-Detection for VCC. The ENQ is a CMOS input equipped with a pull-up resistor. The enable input needs be pulled low to enable device operation. If the enable pin is left unconnected or pulled high, all outputs are pulled low.

5.3. Trigger input

- CMOS differential amplifier with hysteresis. The negative input is attached to the internal reference while the positive input is connected to the corresponding input pins. Inputs are equipped with a pull-down resistor.

5.4. UV Detection on VCC

- CMOS comparator with a hysteresis to detect under voltage supply conditions on VCC.

5.5. Logic and dead time

- Input logic and dead time insertion. The dead time is set internally by an RC-combination.

5.6. Pulse-Generator

- Pulse generation from falling and rising edges of the input signal. These pulses are transmitted to the floating high side gate driver stages. This leads to lower power consumption.

5.7. HV-Level-Shifter

- Level shifting the pulses of the pulse generators to the floating high side driver output stages.

5.8. Filter

- Filtering noise and transients.

5.9. R-S

- Latch for storing the current output state.

5.10. UV Detection for the High Side

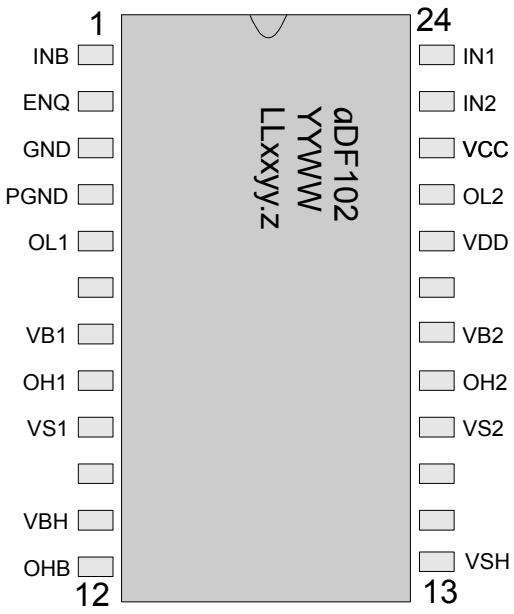
- Detecting under voltage conditions during power up and during operation. Pulling the high side drivers low in case of too low a supply.

5.11. DRV

- CMOS gate driver output stage for low and high side.

6. Pinning

PIN#	Symbol	Description
1	INB	Logic input for high side gate driver output OHB
2	ENQ	Input to enable device operation (active low)
3	GND	Ground
4	PGND	Power Ground
5	OL1	Low side gate driver output, inverted to IN1
6	n.c.	
7	VB1	High side gate driver supply
8	OH1	High side gate driver output, in phase with IN1
9	VS1	High side gate driver supply return
10	n.c.	
11	VBH	High side buck driver supply
12	OHB	High side gate driver output, in phase with INB
13	VSH	High side buck driver supply return
14	n.c.	
15	n.c.	
16	VS2	High side gate driver supply return
17	OH2	High side gate driver output, in phase with IN2
18	VB2	High side gate driver supply
19	n.c.	
20	VDD	Low side driver supply
21	OL2	Low side gate driver output, inverted to IN2
22	VCC	Logic supply
23	IN2	Input for high and low side gate drive outputs OH2 + OL2
24	IN1	Input for high and low side gate drive outputs OH1 + OL1



Top View

7. Pin description

VCC	**Logic supply**
VDD	**Low side driver supply**
GND	**Signal and logic GND**
PGND	**Power ground, supply return for low side gate drivers (bridge)**
IN1	**Signal input for the first half bridge**
IN2	**Signal input for the second half bridge**
INB	**Signal input for the buck converter high side driver**
ENQ	**Enable input, enables the inputs, low active**
VBH	**High side supply for the buck converter high side driver**
OHB	**High side buck converter gate driver output**
VSH	**High side supply return for the buck converter gate drive OHB**
VB1,2	**High side supply for high side gate drivers (bridge)**
OH1,2	**High side gate driver outputs (bridge)**
VS1,2	**High side supply return for gate drivers OH1,2 (bridge)**
OL1,2	**Low side driver outputs (bridge)**

8. Absolute Maximum Ratings

The maximum ratings may not under any circumstances be exceeded, TA = -25°C bis 85°C

#	Symbol	Parameter	Min	Max	Unit
1	V_{CC}	Logic supply voltage	-0.3	18	V
2	V_{DD}	Low side driver supply voltage	-0.3	18	V
3	V_{Bx}	High side floating supply voltage	-0.3	618	V
4	V_{Sx}	High side floating supply offset voltage	V_{BX} - 18[1]	V_{BX} + 0.3	V
5	V_{OH}	High side floating output voltage	V_{SX} –0.3	V_{BX} + 0.3	V
6	V_{INX}	Logic input voltage (IN1, IN2, INB)	-0.3	V_{CC}+0.3	V
7	V_{ENQ}	Input voltage Enable (ENQ)	-0.3	V_{CC}+0.3	V
8	T_J[2]	Junction Temperature	-25	150	°C
9	T_{stg}	Storage temperature range	-55	150	°C
10	Rthja	Thermal resistance junction to ambient		80	K/W
11	V_{ESD}[3]	ESD (acc. HMB), pins IN1, IN2, INB and ENQ	-500	500	V
12	V_{ESD}[4]	ESD (according to HMB), all other pins	-1000	1000	V

9. Electrical Characteristics

9.1. Operational Range

#	Symbol	Parameter	Min	Max	Unit
1	V_{Bx}	Absolute high side supply voltage	V_{SX} +12	V_{SX} +15	V
2	V_{Sx}	High side floating supply offset voltage		400	V
3	V_{DD}	Low side driver supply voltage	12	15	V
4	V_{CC}	Logic supply voltage	12	15	V
5	f_s	Switching frequency		120	KHz
6	V_{INX}	Logic input voltage (INB, IN1, IN2, pull-down)	V_{GND}	V_{GND} + V_{CC}	V
7	V_{ENQ}	Enable input voltage (ENQ, pull-up)	V_{GND}	V_{GND} + V_{CC}	V
8	t_{pw}	High side pulse width (PWM)	1		µs
9	T_A	Ambient temperature	-25	85	°C

1 The suffix x is a replacement for a respective 1, 2 or B

2 $T_J = R_{thja} * P_{tot} + T_A$

3 HBM for Inputs only

4 HBM for Inputs only

9.2. DC Characteristics

DC characteristics contain the spread of values guaranteed within the specified supply voltage and temperature range and the technology process parameter range unless otherwise specified.

Typical values are valid at V_{CC} = V_{DD} =15V, V_{BX}-V_{SX} =15V, ENQ=Low, T_J = 25°C unless stated.

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	I_{QCC}	Quiescent V_{CC} supply current	IN_X=open		0.8	1.4	mA
2	I_{QDD}	Quiescent V_{DD} supply current	IN_X=open		2	2.5	mA
3	I_{QBH}	Quiescent V_{BH} supply current	IN_X=open		0.4	0.6	mA
4	I_{QBX}	Quiescent V_{BX} supply current	IN_X=open		0.9	1.6	mA
5	V_{CCUV+}	Rising VCC supply undervoltage threshold	IN_X=open	tbd	11.6	tbd	V
6	V_{CCUV-}	Falling VCC supply undervoltage threshold	IN_X=open	tbd	10.8	tbd	V
7	I_{O-}	Output Low short circuit pulsed current	V_O=12V t_{PW}<1µs, T_J =25°C	200	tbd	-	mA
8	I_{O+}	Output High short circuit pulsed current	V_O=0V t_{PW}<1µs, T_J =25°C	150	tbd	-	mA

9.3. Logic Characteristics

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{INL}	Low input voltage (INB, IN1, IN2)		-	4.5	5.5	V
2	V_{INH}	High input voltage (INB, IN1, IN2,)		9.0	10.0	-	V
3	I_{INH}	High input bias current (pull-down)		-	20	60	µA
4	I_{INL}	Low input bias current (pull-down)	V_{IN}=0.1V	-	-	1	µA

9.4. AC Characteristics

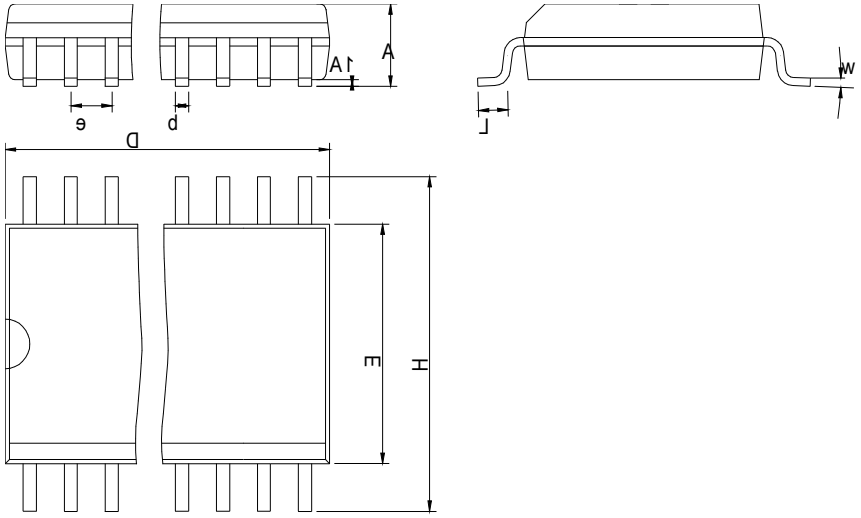
AC characteristics contain the spread of values guarantee within the specified supply voltage and temperature range and the technology process parameter range unless otherwise specified.

All values are valid at V_{CC} = V_{DD} =15V, V_{BX}-V_{SX} =15V, C_{Load}=1000pF, T_J= 25°C unless stated.

#	Symbol	Parameter	Typ	Max	Unit
1	t_{onINX}[5]	Turn-on propagation delay	1200		ns
2	t_{offINX}[4]	Turn-off propagation delay	50		ns
3	t_r	Turn on rise time	100		ns
4	t_f	Turn off fall time	50		ns

10. IC-Package

24-pin Plastic SOP



Small Outline Package (SOP) SOP24				JEDEC MS-012 300 mil					
Dimensions (mm)	D	E	H	A	A1	e	b	L	w
nom	15.3	7.5	10.31	2.54	0.20	1.27	0.41	0.76	4°

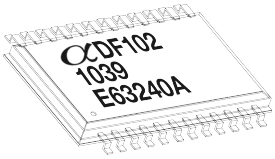
5 The suffix x is a replacement for a respective 1, 2

11. IC-Marking

*a*DF102

4 digits date code = 2 digits year + 2 digits work week

8 digits lot number = 2 digits fab process + 4 digits lot number + 1 digit sub lot



12. Ordering Information

AMG-DF102-ISP24U	shipment in tubes
AMG-DF102-ISP24R	shipment in Tape & Reel

13. Notes and Cautions

13.1. ESD Protection

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1MΩ resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

13.2. Storage conditions

The AMG-DF102 corresponds to moisture sensitivity classification ML2, according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

14. Disclaimer

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