

## RF Power Field Effect Transistor

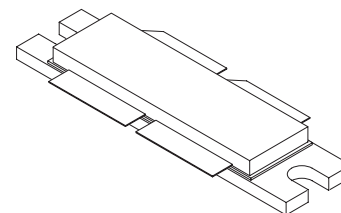
### N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts,  $I_{DQ} = 2 \times 700$  mA  
 IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13  
     Output Power — 40 Watts  
     Power Gain — 17 dB  
     Efficiency — 26%  
     Adjacent Channel Power –  
         750 kHz: -45.0 dBc @ 30 kHz BW  
         1.98 MHz: -60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

**MRF9180R6**

**880 MHz, 170 W, 26 V  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



**CASE 375D-05, STYLE 1  
 NI-1230**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	388 2.22	W W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

**Table 3. ESD Protection Characteristics**

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

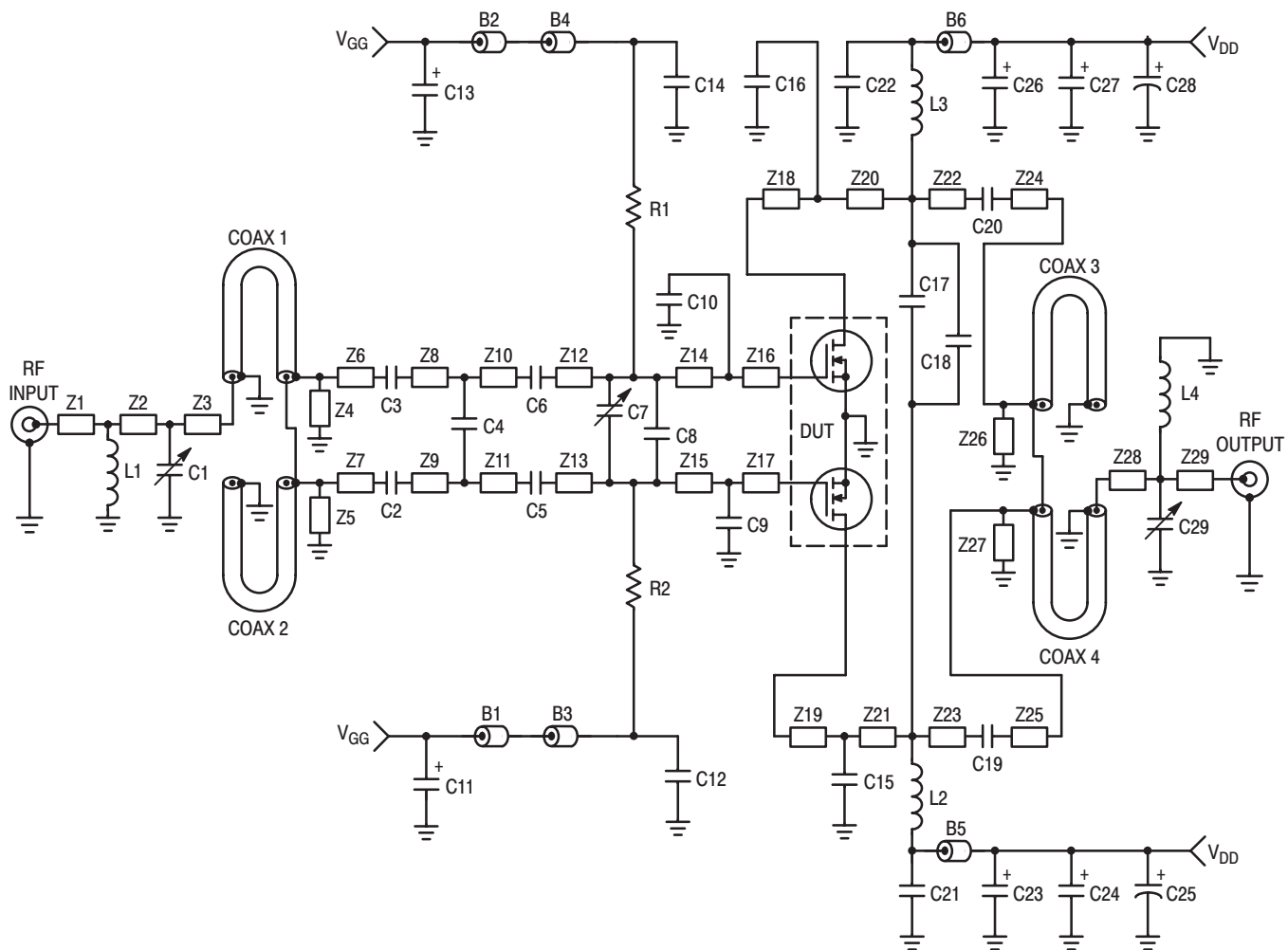
Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b> <sup>(1)</sup>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate–Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$
<b>On Characteristics</b> <sup>(1)</sup>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 300\ \mu\text{A}$ )	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 700\text{ mA}$ )	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2\text{ A}$ )	$V_{DS(on)}$	—	0.19	0.5	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 6\text{ A}$ )	$g_{fs}$	—	6	—	S
<b>Dynamic Characteristics</b> <sup>(1)</sup>					
Output Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	77	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	3.8	—	pF
<b>Functional Tests</b> (In Freescale Test Fixture, 50 ohm system) <sup>(2)</sup>					
Two–Tone Common–Source Amplifier Power Gain ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ , $f_2 = 880.1\text{ MHz}$ )	$G_{ps}$	16	17.5	—	dB
Two–Tone Drain Efficiency ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ , $f_2 = 880.1\text{ MHz}$ )	$\eta$	35	39	—	%
3rd Order Intermodulation Distortion ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ , $f_2 = 880.1\text{ MHz}$ )	IMD	—	–31	–28	dBc
Input Return Loss ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ , $f_2 = 880.1\text{ MHz}$ )	IRL	—	–15	–9	dB
Two–Tone Common–Source Amplifier Power Gain ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 865.0\text{ MHz}$ , $f_2 = 865.1\text{ MHz}$ )	$G_{ps}$	—	17.5	—	dB
Two–Tone Drain Efficiency ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 865.0\text{ MHz}$ , $f_2 = 865.1\text{ MHz}$ )	$\eta$	—	38.5	—	%
3rd Order Intermodulation Distortion ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 865.0\text{ MHz}$ , $f_2 = 865.1\text{ MHz}$ )	IMD	—	–31	—	dBc
Input Return Loss ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W PEP}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 865.0\text{ MHz}$ , $f_2 = 865.1\text{ MHz}$ )	IRL	—	–13	—	dB
Power Output, 1 dB Compression Point ( $V_{DD} = 26\text{ Vdc}$ , CW, $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ )	$P_{1dB}$	—	170	—	W

- Each side of device measured separately.
- Device measured in push–pull configuration.

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

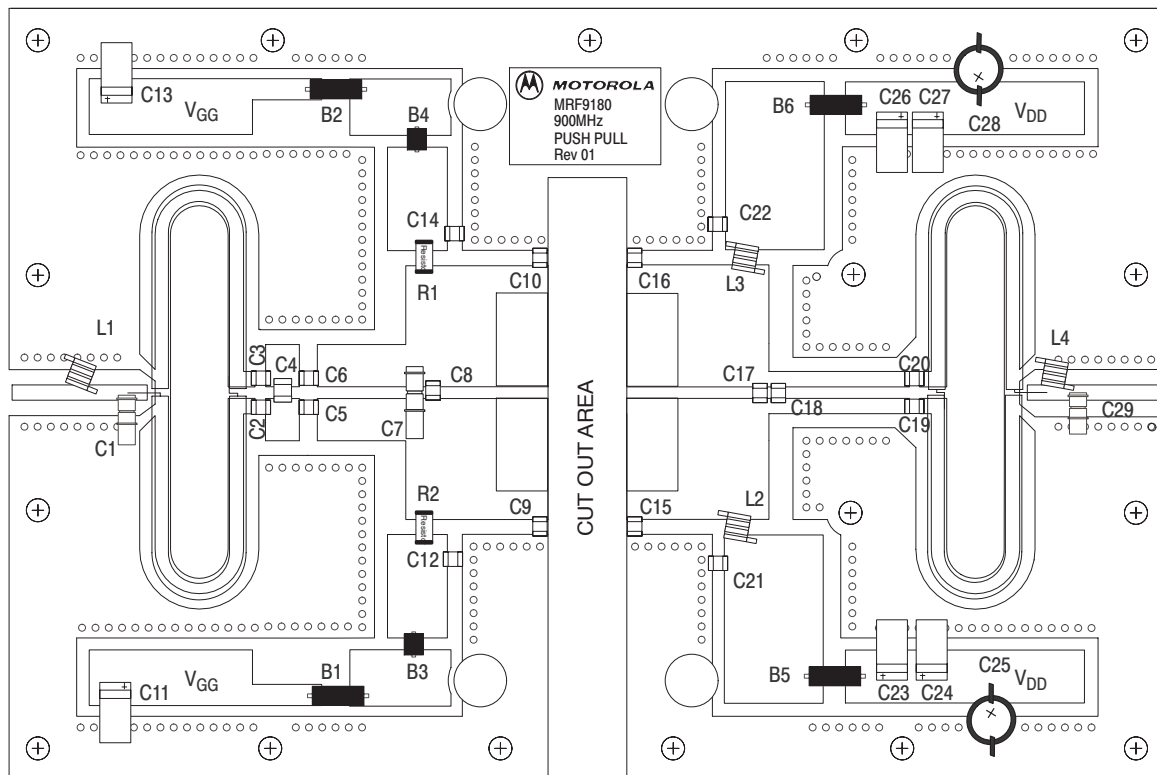
Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> (In Freescale Test Fixture, 50 ohm system) <sup>(2)</sup> <b>(continued)</b>					
Common-Source Amplifier Power Gain ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W CW}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ )	$G_{ps}$	—	16.5	—	dB
Drain Efficiency ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W CW}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f_1 = 880.0\text{ MHz}$ )	$\eta$	—	55	—	%
Output Mismatch Stress ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 170\text{ W CW}$ , $I_{DQ} = 2 \times 700\text{ mA}$ , $f = 880\text{ MHz}$ , $V_{SWR} = 10:1$ , All Phase Angles at Frequency of Tests)	$\Psi$	No Degradation In Output Power Before and After Test			

2. Device measured in push-pull configuration.



B1, B2, B5, B6	Long Ferrite Beads, Surface Mount	Z1	0.420" x 0.080" Microstrip
B3, B4	Short Ferrite Beads, Surface Mount	Z2	0.190" x 0.080" Microstrip
C1	0.6–4.5 pF Variable Capacitor	Z3	0.097" x 0.080" Microstrip
C2, C3, C5, C6, C12, C14, C19, C20, C21, C22	47 pF Chip Capacitors	Z4, Z5, Z26, Z27	2.170" x 0.080" Microstrip
C4, C9, C10, C15, C16	12 pF Chip Capacitors	Z6, Z7	0.075" x 0.080" Microstrip
C7	0.8–9.1 pF Variable Capacitor	Z8, Z9	0.088" x 0.220" Microstrip
C8	7.5 pF Chip Capacitor	Z10, Z11	0.088" x 0.220" Microstrip
C11, C13	10 $\mu$ F, 35 V Tantalum Surface Mount Chip Capacitors	Z12, Z13	0.460" x 0.220" Microstrip
C17	3.6 pF Chip Capacitor	Z14, Z15	0.685" x 0.625" Microstrip
C18	5.1 pF Chip Capacitor	Z16, Z17	0.055" x 0.625" Microstrip
C23, C24, C26, C27	22 $\mu$ F, 35 V Tantalum Surface Mount Chip Capacitors	Z18, Z19	0.055" x 0.632" Microstrip
C25, C28	220 $\mu$ F, 50 V Electrolytic Capacitors	Z20, Z21	0.685" x 0.632" Microstrip
C29	0.4–2.5 pF Variable Capacitor	Z22, Z23	0.732" x 0.080" Microstrip
Coax1, Coax2	25 $\Omega$ , Semi Rigid Coax, 70 mil OD, 1.05" Long	Z24, Z25	0.060" x 0.080" Microstrip
Coax3, Coax4	50 $\Omega$ , Semi Rigid Coax, 85 mil OD, 1.05" Long	Z28	0.230" x 0.080" Microstrip
L1, L2, L3	18.5 nH Mini Spring Inductors, Coilcraft	Z29	0.460" x 0.080" Microstrip
L4	12.5 nH Mini Spring Inductor, Coilcraft	Board	30 mil Teflon <sup>®</sup> , $\epsilon_r = 2.55$ ,
R1, R2	510 $\Omega$ , 1/10 W Chip Resistors	Material	Copper Clad, 2 oz Cu

Figure 1. 880 MHz Broadband Test Circuit Schematic



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**Figure 2. 880 MHz Broadband Test Circuit Component Layout**

### TYPICAL CHARACTERISTICS

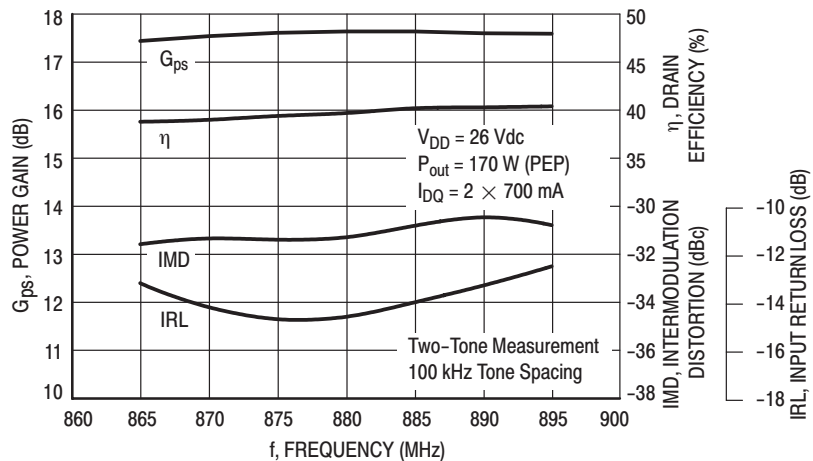


Figure 3. Class AB Broadband Circuit Performance

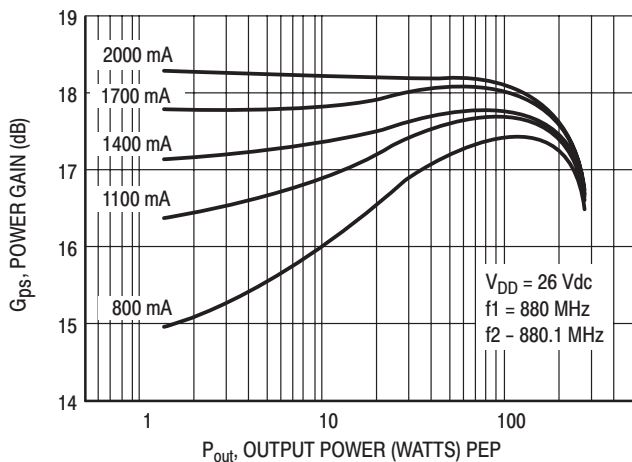


Figure 4. Power Gain versus Output Power

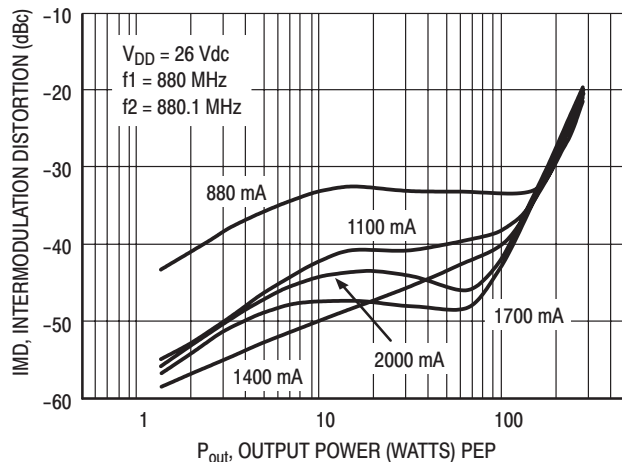


Figure 5. Intermodulation Distortion versus Output Power

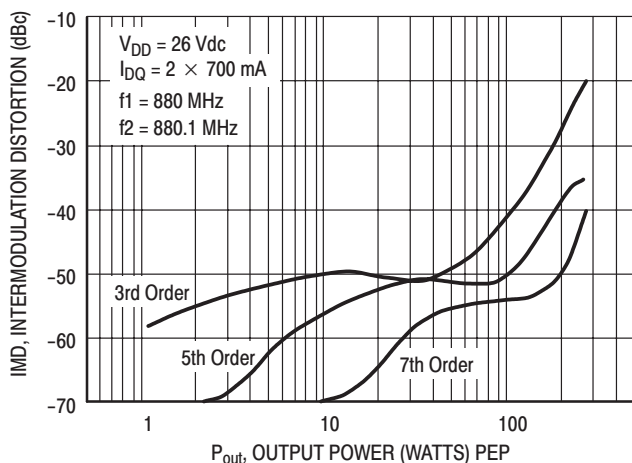


Figure 6. Intermodulation Distortion Products versus Output Power

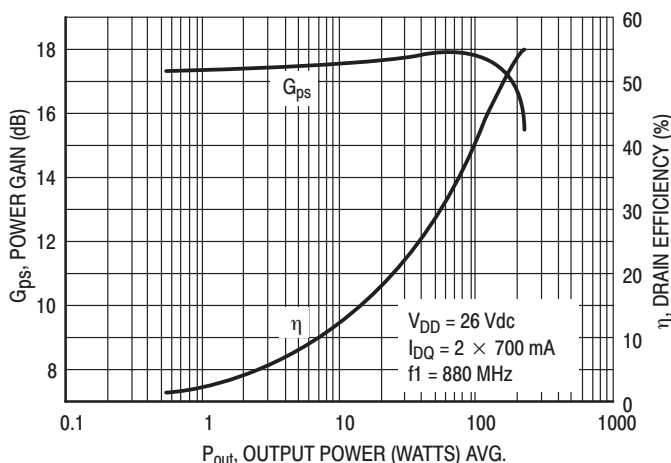
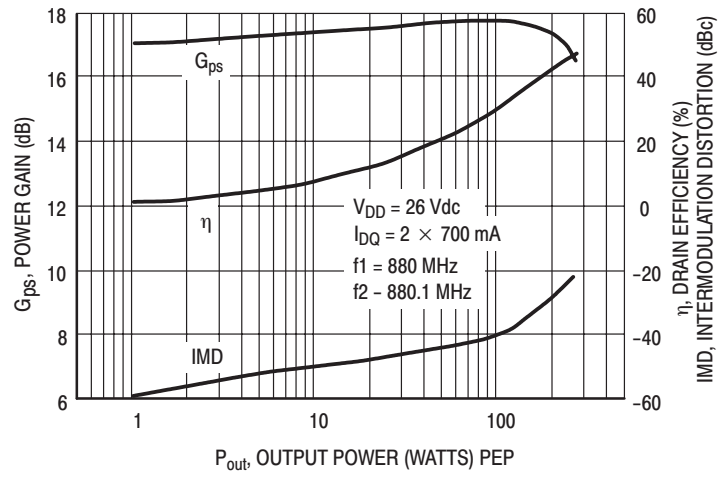
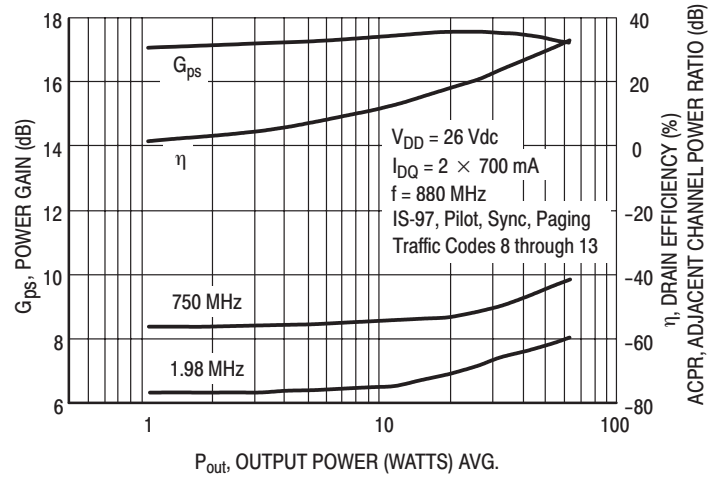


Figure 7. Power Gain and Efficiency versus Output Power

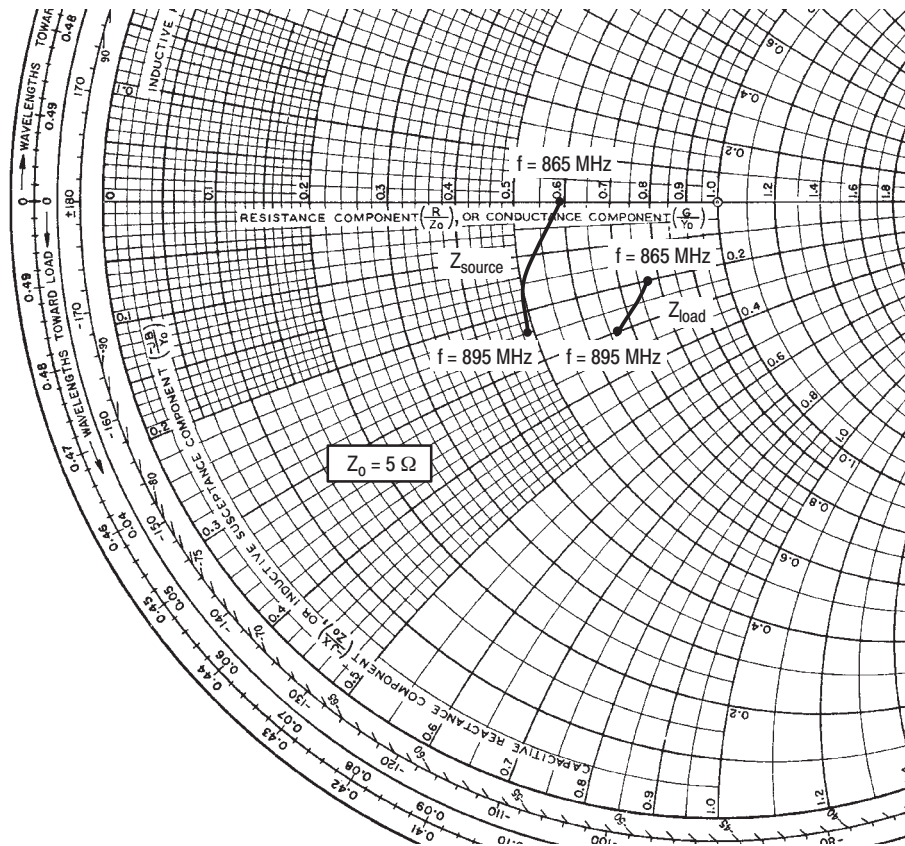
## TYPICAL CHARACTERISTICS



**Figure 8. Power Gain, Efficiency and IMD versus Output Power**



**Figure 9. Power Gain, Efficiency and ACPR versus Output Power**



$V_{DD} = 26 \text{ V}$ ,  $I_{DQ} = 2 \times 700 \text{ mA}$ ,  $P_{\text{out}} = 170 \text{ W PEP}$

f MHz	$Z_{\text{source}}$ $\Omega$	$Z_{\text{load}}$ $\Omega$
865	$2.95 - j0.00$	$3.83 - j1.02$
880	$2.48 - j0.67$	$3.55 - j1.38$
895	$2.44 - j1.18$	$3.34 - j1.51$

$Z_{\text{source}}$  = Test circuit impedance as measured from gate to gate, balanced configuration.

$Z_{\text{load}}$  = Test circuit impedance as measured from drain to drain, balanced configuration.

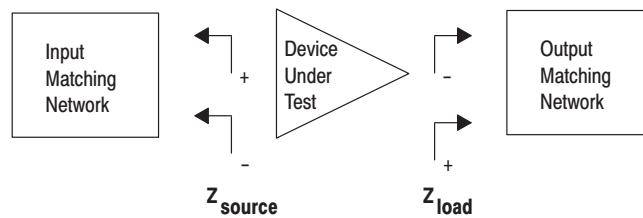


Figure 10. Series Equivalent Source and Load Impedance



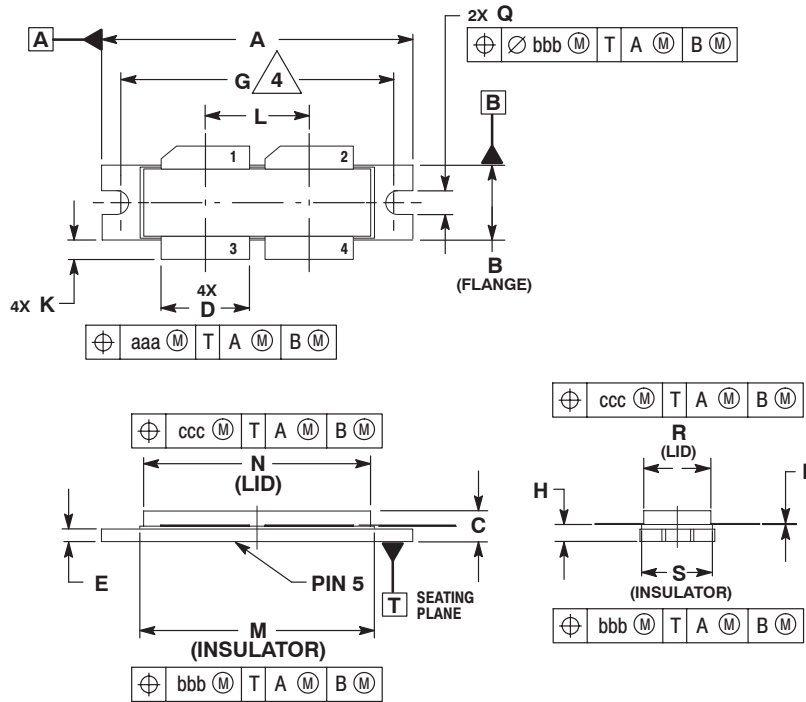


# NOTES



## NOTES

## PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400 BSC		35.56 BSC	
H	0.082	0.090	2.08	2.29
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

- STYLE 1:
1. DRAIN
  2. DRAIN
  3. GATE
  4. GATE
  5. SOURCE

CASE 375D-05  
ISSUE D  
NI-1230

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Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

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Technical Information Center  
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