Ordering number : ENA1980

SANYO Semiconductors
DATA SHEET

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LV5980MX — Bi-CMOS IC Low power consumption and high efficiency Step-down Switching Regulator

Overview

LV5980MX is 1ch DC-DC converter with built-in power Pch MOSFET. The recommended operating range is 4.5V to 23V. The maximum current is 3A. The operating current is about 60μA, and low power consumption is achieved.

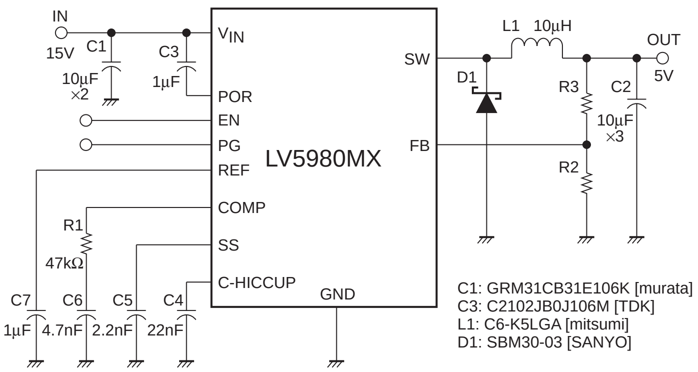
Features and Functions

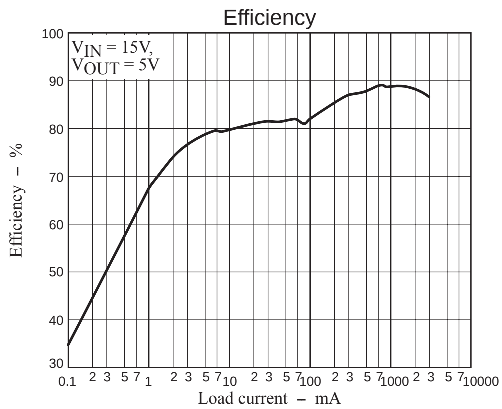
- 1ch SBD rectification DC-DC converter IC with built-in power Pch MOSFET
- Typical value of light load mode current is 60μA
- 4.5V to 23V Operating input voltage range
- 100mΩ High-side switch
- Output voltage adjustable to 1.235V
- The oscillatory frequency is 370kHz
- built-in OCP circuit with P-by-P method
- When P-by-P is generated continuously, it shifts to the HICCUP operation
- If connect C-HICCUP to GND pin, then latch-off when over current
- External capacitor Soft-start
- Under voltage lock-out, thermal shutdown and power good indication

Applications

- DVD/Blu-ray™ drivers and HDD
- LCD monitors and TVs
- Point of load DC/DC converters
- Office supplies

Application Circuit Example





SANYO Semiconductor Co., Ltd.
http://semicon.sanyo.com/en/network

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN} max		25	V
Allowable pin voltage	V_{IN}-SW		30	V
	EN		V_{IN}	V
	PG		V_{IN}	V
	V_{IN}-PDR		6	V
	REF		6	V
	SS		REF	V
	FB		REF	V
	COMP		REF	V
	C-HICCUP		REF	V
Allowable power dissipation	Pd max	Specified substrate *1	1.05	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*1 Specified substrate : 40.0mm × 30.0mm × 1.6mm, fiberglass epoxy printed circuit board, 2 layers

Note 1 : Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Note 2 : Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input Voltage Range	V_{IN}		4.5 to 23	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 15V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage						
Internal reference voltage	V_{REF}		1.210	1.235	1.260	V
Pch drive voltage	V_{PDR}	I_{OUT} = 0 to -5mA	V_{IN}-5.5	V_{IN}-5.0	V_{IN}-4.5	V
Saw wave oscillator						
Oscillatory frequency	F_{OSC}		310	370	430	kHz
ON/OFF circuit						
IC startup voltage (EN PIN)	V_{CNT}_ON		2.0		V_{IN}	V
Disable voltage (EN PIN)	V_{CNT}_OFF				0.3	V
Soft start circuit						
Soft start • source current	I_{SS}_SC	EN > 2V	1.2	1.8	2.4	μA
Soft start • sink current	I_{SS}_SK	EN < 0.3V, SS = 0.4V		220		μA
UVLO circuit						
UVLO release voltage	V_{UVLON}	FB = COMP	3.3	3.7	4.1	V
UVLO lock voltage	V_{UVLOF}	FB = COMP	3.02	3.42	3.82	V
Error amplifier						
Input bias current	I_{EA}_IN		-100	-10		nA
Error amplifier gain	G_{EA}		100	220	380	μA/V
Output sink current	I_{EA}_OSK	FB = 1.75V	-30	-17	-8	μA
Output source current	I_{EA}_OSC	FB = 0.75V	8	17	30	μA
Over current limit circuit						
Current limit peak	I_{CL}		3.5	4.7	6.2	A
HICCUP timer start-up cycle	N_{CYC}			15		cycle
HICCUP comparator threshold voltage	V_{tHIC}		1.19	1.25	1.31	V
HICCUP timer charge current	I_{HIC}			1.8		μA
PWM comparator						
Maximum on-duty	D_{MAX}		94			%

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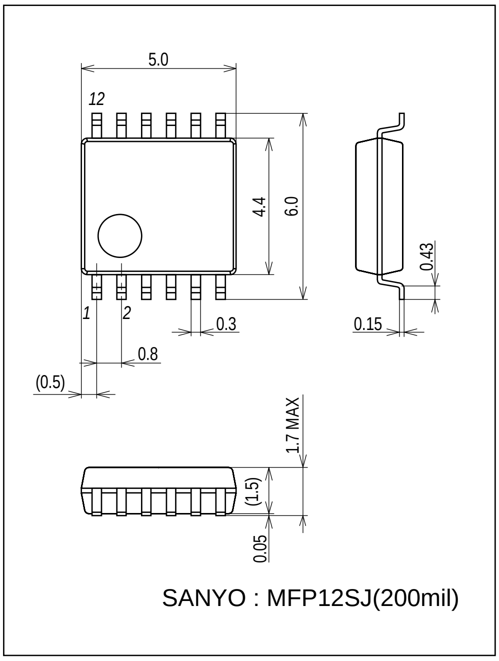
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic output						
Power good “L” sink current	I_{PWRGD_L}	PG = 0.5V		0.47		mA
Power good “H” leakage current	I_{PWRGD_H}	PG = 5V			1	μA
Power good threshold FB voltage	V_{tPG}		0.97	1.07	1.17	V
Power good hysteresis	V_{PG_H}		40	50	60	mV
Output						
Output on resistance	R_{ON}	I_O = 0.5A		100		mΩ
The entire device						
Standby current	I_{CCS}	EN < 0.3V			1	μA
Light load mode consumption current	I_{SLEEP}	EN > 2V, No oscillatory		60	80	μA
Thermal shutdown	TSD	Design guarantee *2		170		°C

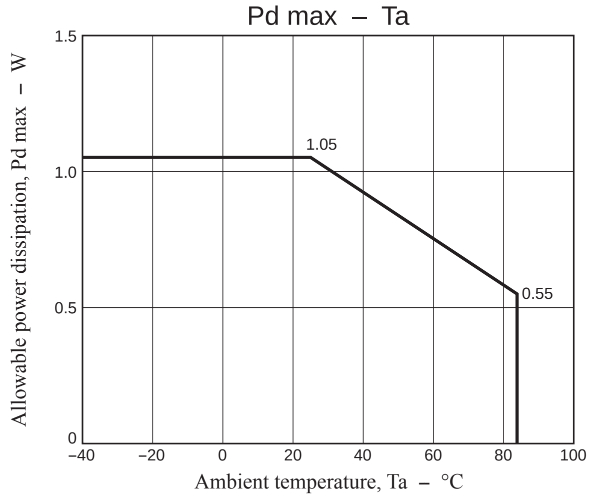
*2 : Design guarantee: Signifies target value in design. These parameters are not tested in an independent IC.

Package Dimensions

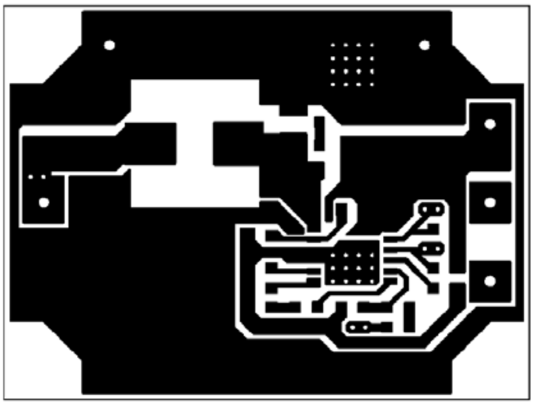
unit : mm (typ)

3414

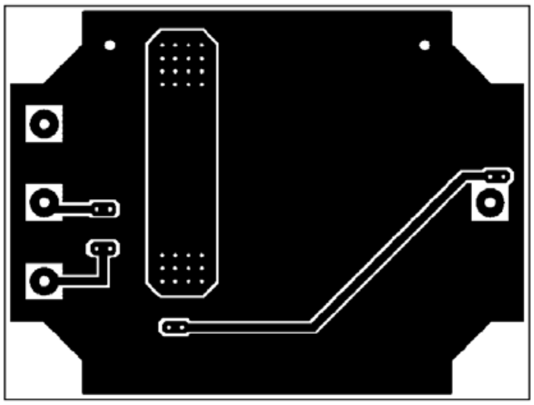




Specified substrate

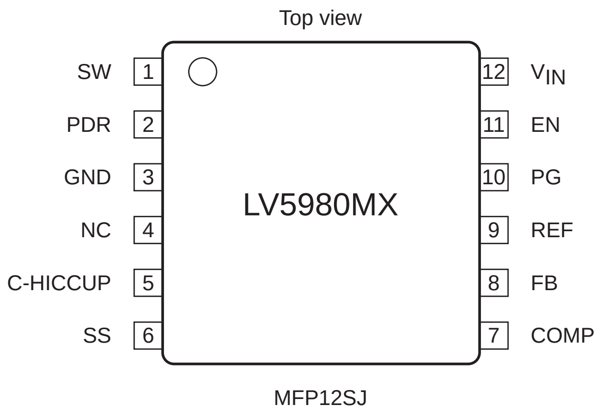


Top

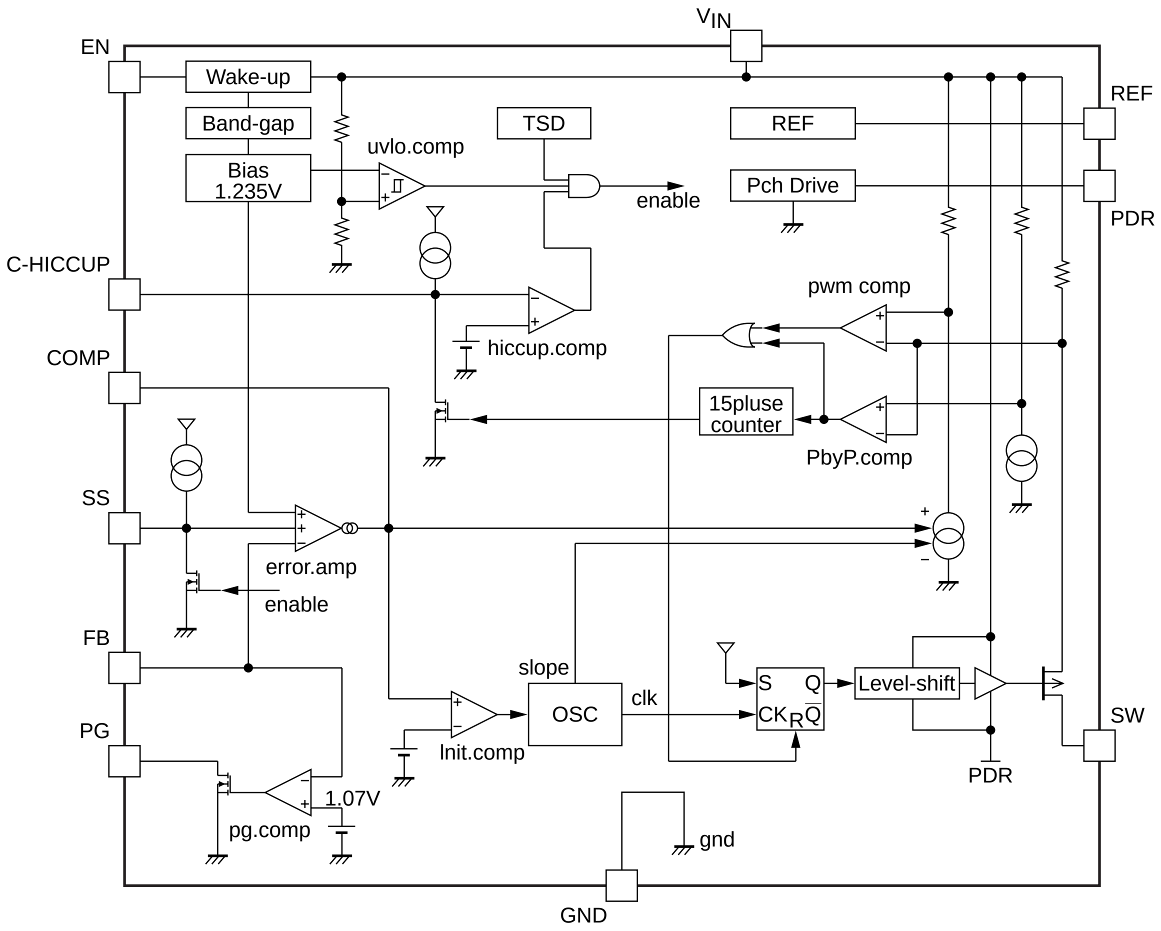


Bottom

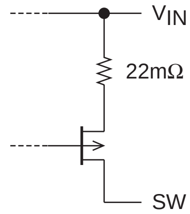
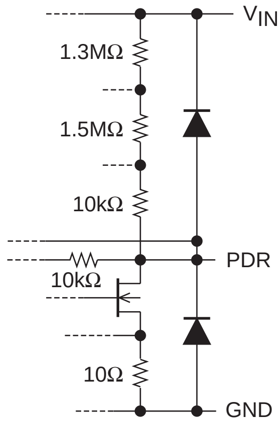
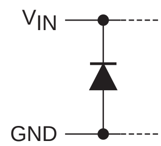
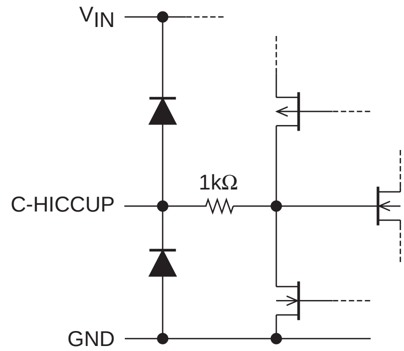
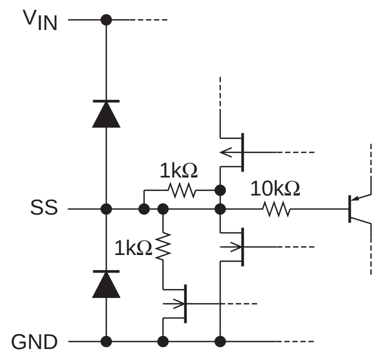
Pin Assignment



Block Diagram



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	SW	High-side Pch MOSFET drain Pin.	
2	PDR	Pch MOSFET gate drive voltage. The bypass capacitor is necessarily connected between this pin and V_{IN}.	
3	GND	Ground Pin. Ground pin voltage is reference voltage	
4	NC	NC Pin. The NC Pin becomes open in an IC. Therefore the NC Pin has any problem by neither the grand short nor the open.	
5	C-HICCUP	It is capacitor connection pin for setting re-startup cycle in HICCUP mode. If connect it to GND pin, then latch-off when over current.	
6	SS	Capacitor connection pin for soft start. About 1.8μA current charges the soft start capacitor.	

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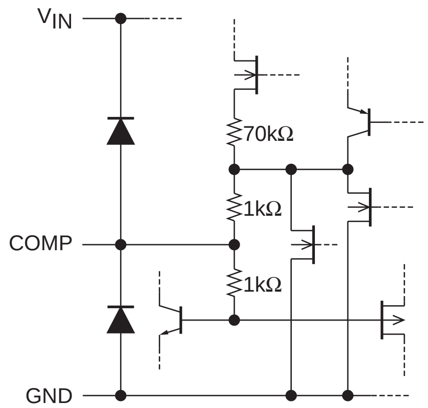
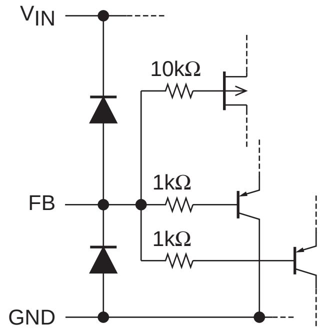
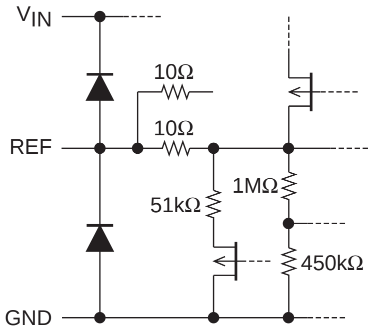
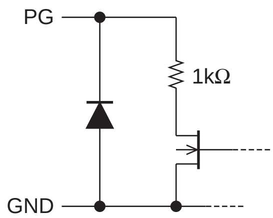
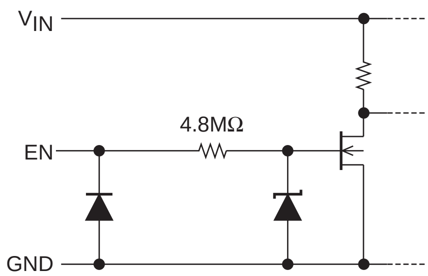
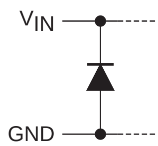
Pin No.	Pin name	Function	Equivalent circuit
7	COMP	Error amplifier output pin. The phase compensation network is connected between GND pin and COMP pin. Thanks to current-mode control, comp pin voltage would tell you the output current amplitude. Comp pin is connected internally to an Init.comparator which comparates with 0.9V reference. If comp pin voltage is larger than 0.9V, IC operates in “continuous mode”. If comp pin voltage is smaller than 0.9V, IC operates in “discontinuous mode (low consumption mode)”.	
8	FB	Error amplifier reverse input pin. ICs make its voltage keep 1.235V. Output voltage is divided by external resistances and it across FB.	
9	REF	Reference voltage.	
10	PG	Power good pin. Connect to open drain of MOS-FET in ICs inside. Setting output voltage to "L", when FB voltage is 1.02V or less.	
11	EN	ON/OFF Pin.	
12	V_{IN}	Supply voltage pin. It is observed by the UVLO function. When its voltage becomes 3.7V or more, ICs startup in soft start.	

Detailed Description

Power-save Feature

The LV5980MX has Power-saving feature to enhance efficiency when the load is light.
By shutting down unnecessary circuits, operating current of the IC is minimized and high efficiency is realized.

Output Voltage Setting

Output voltage (V_{OUT}) is configurable by the resistance R3 between V_{OUT} and FB and the R2 between FB and GND. V_{OUT} is given by the following equation (1).

$$V_{OUT} = (1 + \frac{R3}{R2}) \times V_{REF} = (1 + \frac{R3}{R2}) \times 1.235 \ \ [V] \qquad (1)$$

Soft Start

Soft start time (T_{SS}) is configurable by the capacitor (C5) between SS and GND. The setting value of T_{SS} is given by the equation (2).

$$T_{SS} = C5 \times \frac{V_{REF}}{I_{SS}} = C5 \times \frac{1.235}{1.8 \times 10^{-6}} \ \ [ms] \qquad (2)$$

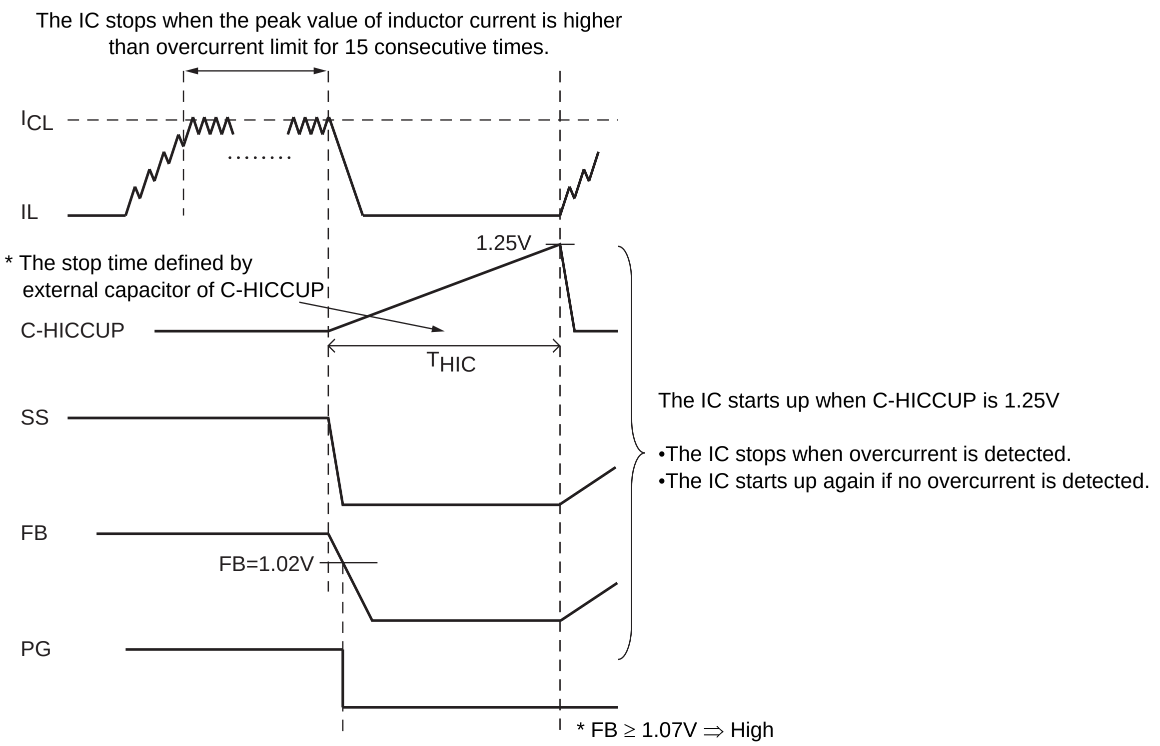
Power Good

FB constantly monitors V_{OUT}. When FB voltage is lower than 1.02V, PG is pulled down to Low. PG comparator has hysteresis of 50mV. Because PG is open-drain output, you can connect other ICs with PG to realize wired-or with other ICs.

Hiccup Over Current Protection

Over current limit (I_{CL}) is set to 4.7A in the IC. When the peak value of inductor current is higher than 4.7A for 15 consecutive times, the protection deems it as over current and stops the IC. Stop period (T_{HIC}) is defined by the external capacitor of the C-HICCUP. When C-HICCUP is about 1.25V, the IC starts up. Regardless of a status; whether it starts up or SS charge, once over current is detected, the IC stops again and when the protection does not detect over current status, the IC starts up again. The setting value of T_{HIC} is given by the equation (3).

$$T_{HIC} = \frac{C4 \times V_{tHIC}}{I_{HIC}} = \frac{C4 \times 1.25}{1.8 \times 10^{-6}} \ \ [s] \qquad (3)$$



Design Procedure

Inductor Selection

When conditions for input voltage, output voltage and ripple current are defined, the following equations (4) give inductance value.

$$\left\{\begin{array}{l} L = \dfrac{V_{IN} - V_{OUT}}{\Delta I_R} \times T_{ON} \\[2ex] T_{ON} = \dfrac{1}{\{((V_{IN} - V_{OUT}) \div (V_{OUT} + VF)) + 1\} \times F_{OSC}} \\[2ex] F_{OSC} \text{ : Oscillatory Frequency} \\ VF \text{ : Forward voltage of Schottky Barrier diode} \\ V_{IN} \text{ : Input voltage} \\ V_{OUT} \text{ : Output voltage} \end{array}\right\} \quad (4)$$

- Inductor current: Peak value (I_{RP})
  Current peak value (I_{RP}) of the inductor is given by the equation (5).

$$I_{RP} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (5)$$

Make sure that rating current value of the inductor is higher than a peak value of ripple current.

- Inductor current: ripple current (ΔI_R)
  Ripple current (ΔI_R) is given by the equation (6).

$$\Delta I_R = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \quad (6)$$

When load current (I_{OUT}) is less than 1/2 of the ripple current, inductor current flows discontinuously.

Output Capacitor Selection

Make sure to use a capacitor with low impedance for switching power supply because of large ripple current flows through output capacitor.
This IC is a switching regulator which adopts current mode control method. Therefore, you can use capacitor such as ceramic capacitor and OS capacitor in which equivalent series resistance (ESR) is exceedingly small.
Effective value is given by the equation (7) because the ripple current (AC) that flows through output capacitor is saw tooth wave.

$$I_{C\_OUT} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times F_{OSC} \times V_{IN}} \ \text{[Arms]} \quad (7)$$

Input Capacitor Selection

Ripple current flows through input capacitor which is higher than that of the output capacitors.
Therefore, caution is also required for allowable ripple current value.
The effective value of the ripple current flows through input capacitor is given by the equation (8).

$$I_{C\_IN} = \sqrt{D\,(1 - D)} \times I_{OUT} \ \text{[Arms]} \quad (8)$$

$$D = \frac{T_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

In (8), D signifies the ratio between ON/OFF period. When the value is 0.5, the ripple current is at a maximum. Make sure that the input capacitor does not exceed the allowable ripple current value given by (8). With (8), if V_{IN}=15V, V_{OUT}=5V, I_{OUT}=1.0A and F_{OSC}=370 kHz, then I_{C_IN} value is about 0.471Arms.
In the board wiring from input capacitor, $\overline{V_{IN}}$ to GND, make sure that wiring is wide enough to keep impedance low because of the current fluctuation. Make sure to connect input capacitor near output capacitor to lower voltage bound due to regeneration current.When change of load current is excessive (I_{OUT}: high ⇒ low), the power of output electric capacitor is regenerated to input capacitor. If input capacitor is small, input voltage increases. Therefore, you need to implement a large input capacitor. Regeneration power changes according to the change of output voltage, inductance of a coil and load current.

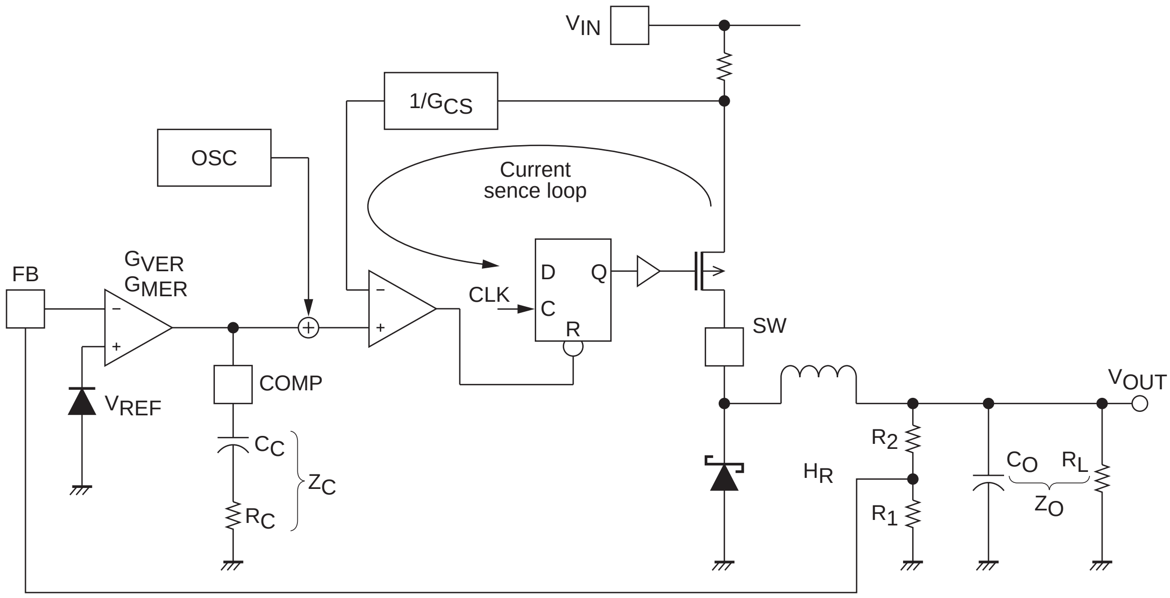
Selection of external phase compensation component

This IC adopts current mode control which allows use of ceramic capacitor with low ESR and solid polymer capacitor such as OS capacitor for output capacitor with simple phase compensation. Therefore, you can design long-life and high quality step-down power supply circuit easily.

Frequency Characteristics

The frequency characteristic of this IC is constituted with the following transfer functions.

(1) Output resistance breeder	: H_R
(2) Voltage gain of error amplifier	: G_{VEA}
Current gain	: G_{MEA}
(3) Impedance of phase compensation external element	: Z_C
(4) Current sense loop gain	: G_{CS}
(5) Output smoothing impedance	: Z_O



Closed loop gain is obtained with the following formula (9).

$$G = H_R \cdot G_{MER} \cdot Z_C \cdot G_{CS} \cdot Z_O$$

$$= \frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{SC_C}\right) \cdot G_{CS} \cdot \frac{R_L}{1 + SC_O \cdot R_L} \qquad (9)$$

Frequency characteristics of the closed loop gain is given by pole fp1 consists of output capacitor C_O and output load resistance R_L, zero point fz consists of external capacitor C_C of the phase compensation and resistance R_C, and pole fp2 consists of output impedance Z_{ER} of error amplifier and external capacitor of phase compensation C_C as shown in formula (9). fp1, fz, fp2 are obtained with the following equations (10) to (12).

$$fp1 = \frac{1}{2\pi \cdot C_O \cdot R_L} \qquad (10)$$

$$fz = \frac{1}{2\pi \cdot C_C \cdot R_C} \qquad (11)$$

$$fp2 = \frac{1}{2\pi \cdot Z_{ER} \cdot C_C} \qquad (12)$$

Calculation of external phase compensation constant

Generally, to stabilize switching regulator, the frequency where closed loop gain is 1 (zero-cross frequency f_{ZC}) should be 1/10 of the switching frequency (or 1/5). Since the switching frequency of this IC is 370kHz, the zero-cross frequency should be 37kHz. Based on the above condition, we obtain the following formula (13).

$$\frac{V_{REF}}{V_{OUT}} \bullet G_{MER} \bullet \left(R_C + \frac{1}{SC_C}\right) \bullet G_{CS} \bullet \frac{R_L}{1 + SC_O \bullet R_L} = 1 \qquad (13)$$

As for zero-cross frequency, since the impedance element of phase compensation is RC >>1/SC_C, the following equation (14) is obtained.

$$\frac{V_{REF}}{V_{OUT}} \bullet G_{MER} \bullet R_C \bullet G_{CS} \bullet \frac{R_L}{1 + 2\pi \bullet f_{ZC} \bullet C_O \bullet R_L} = 1 \qquad (14)$$

Phase compensation external resistance can be obtained with the following formula (15), the variation of the formula (14). Since $2\pi \bullet f_{ZC} \bullet C_O \bullet R_L >> 1$ in the equation (15), we know that the external resistance is independent of load resistance.

$$R_C = \frac{V_{OUT}}{V_{REF}} \bullet \frac{1}{G_{MER}} \bullet \frac{1}{G_{CS}} \bullet \frac{1 + 2\pi \bullet f_{ZC} \bullet C_O \bullet R_L}{R_L} \qquad (15)$$

When output is 5V and load resistance is 5Ω (1A load), the resistances of phase compensation are as follows.
G_{CS} = 2.7A/V, G_{MER} = 220μA/V, f_{ZC} = 37kHz

$$R_C = \frac{5}{1.235} \times \frac{1}{220 \times 10^{-6}} \times \frac{1}{2.7} \times \frac{1 + 2 \times 3.14 \times (37 \times 10^3) \times (30 \times 10^{-6}) \times 5}{5} = 48.898\ldots \times 10^3$$

$$= 48.90\ [k\Omega]$$

If frequency of zero point fz and pole fp1 are in the same position, they cancel out each other. Therefore, only the pole frequency remains for frequency characteristics of the closed loop gain.
In other words, gain decreases at -20dB/dec and phase only rotates by 90º and this allows characteristics where oscillation never occurs.

$$fp1 = fz$$

$$\frac{1}{2\pi \bullet C_O \bullet R_L} \bullet \frac{1}{2\pi \bullet C_O \bullet R_C}$$

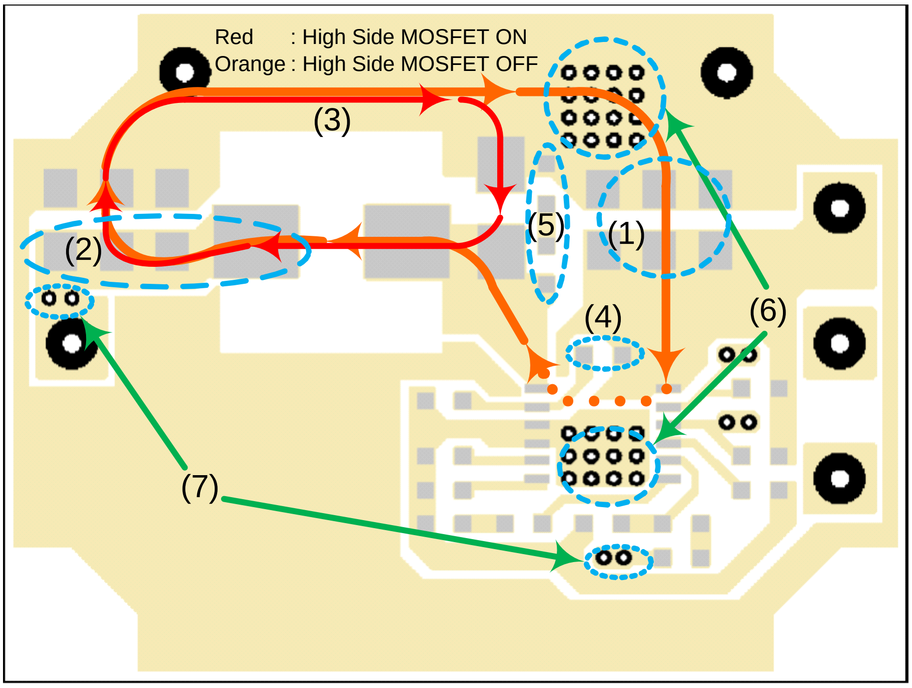
$$C_C = \frac{R_L \bullet C_O}{R_C} \bullet \frac{5 \times (30 \times 10^{-6})}{48.9 \times 10^3} = 3.067\ldots \times 10^{-9}$$

$$= 3.07\ [nF]$$

The above shows external compensation constant obtained through ideal equations. In reality, we need to define phase constant through testing to verify constant IC operation at all temperature range, load range and input voltage range. In the evaluation board for delivery, phase compensation constants are defined based on the above constants. The zero-cross frequency required in the actual system board, in other word, transient response is adjusted by external compensation resistance. Also, if the influence of noise is significant, use of external phase compensation capacitor with higher value is recommended.

Caution in pattern design

Pattern design of the board affects the characteristics of DC-DC converter. This IC switches high current at a high speed. Therefore, if inductance element in a pattern wiring is high, it could be the cause of noise. Make sure that the pattern of the main circuit is wide and short.



(1) Pattern design of the input capacitor

Connect a capacitor near the IC for noise reduction between V_{IN} and the GND. The change of current is at the largest in the pattern between an input capacitor and V_{IN} as well as between GND and an input capacitor among all the main circuits. Hence make sure that the pattern is as fat and short as possible.

(2) Pattern design of an inductor and the output capacitor

High electric current flows into the choke coil and the output capacitor. Therefore this pattern should also be as fat and short as possible.

(3) Pattern design with current channel into consideration

Make sure that when High side MOSFET is ON (red arrow) and OFF (orange arrow), the two current channels runs through the same channel and an area is minimized.

(4) Pattern design of the capacitor between V_{IN}-PDR

Make sure that the pattern of the capacitor between V_{IN} and PDR is as short as possible.

(5) Pattern design of the snubber circuit

Locate a snubber circuit in parallel with the Schottky barrier diode.

(6) Pattern design of the small signal GND

The GND of the small signal should be separated from the power GND.

(7) Pattern design of the FB-OUT line

Wire the line shown in red between FB and OUT to the output capacitor as near as possible.

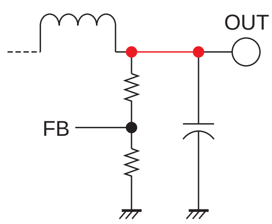
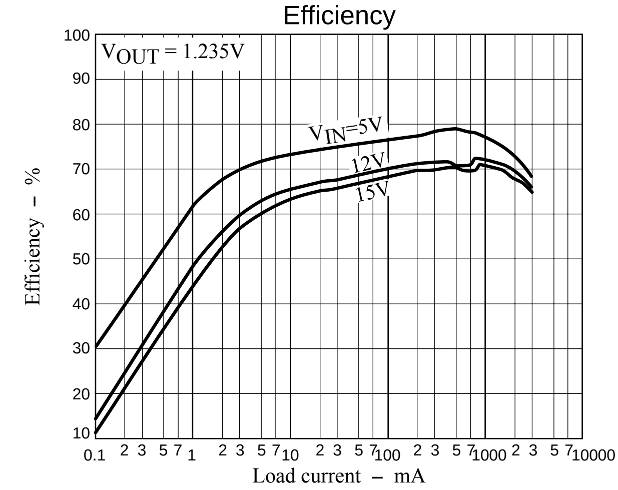
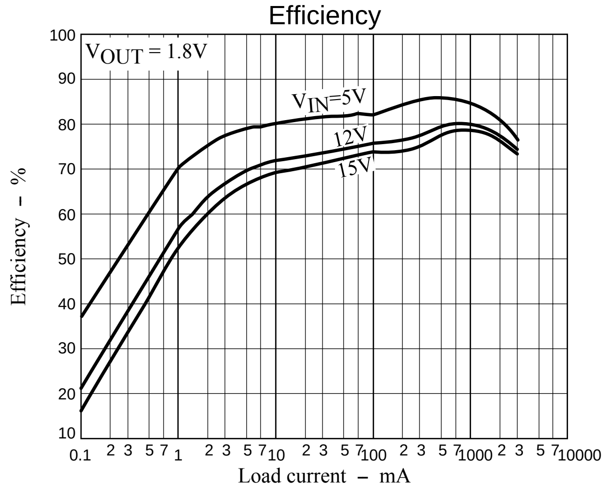
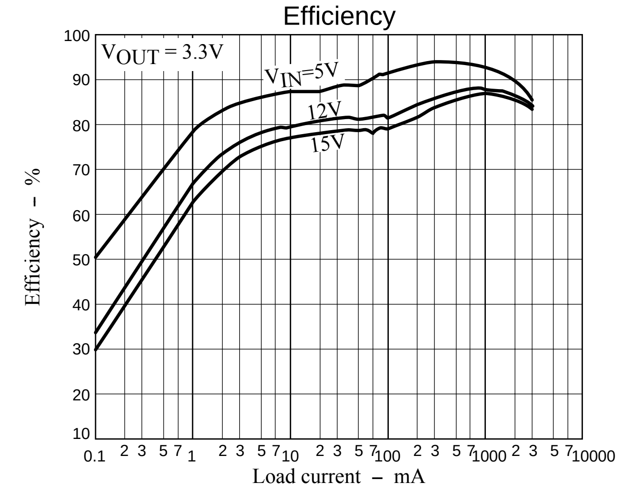


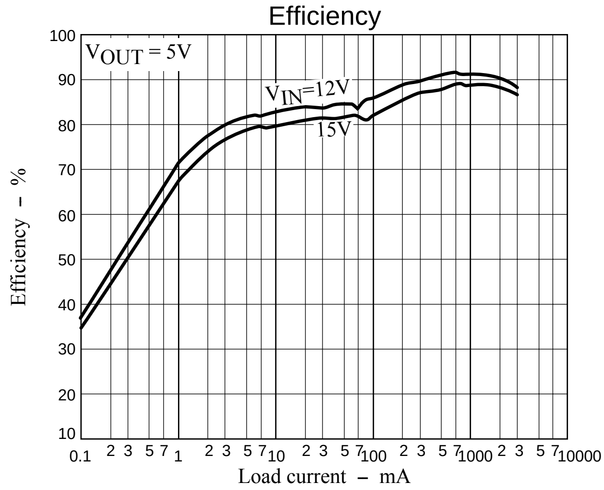
Fig: FB-OUT Line

Typical Performance Characteristics
Application Curves at Ta = 25°C

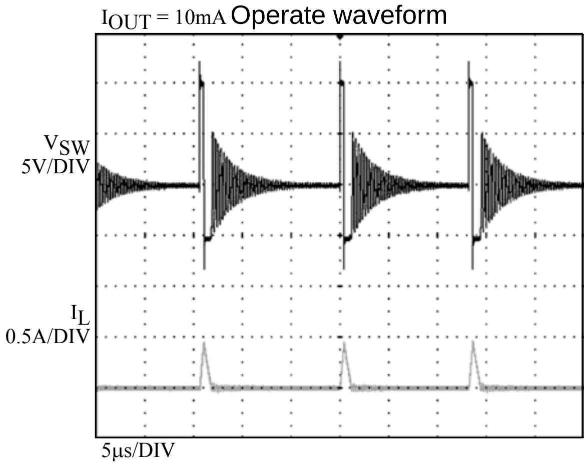


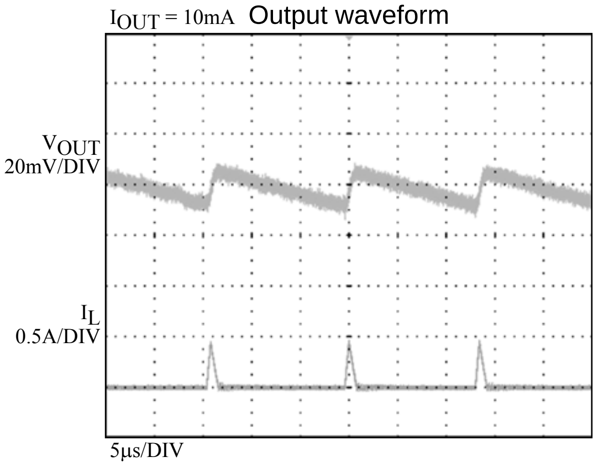




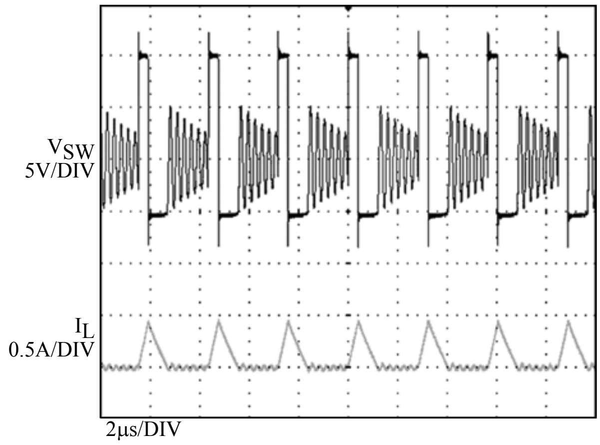


Wake up sequence (Circuit from Typical Application, Ta = 25°C, V_{IN} = 15V, V_{OUT} = 5V)

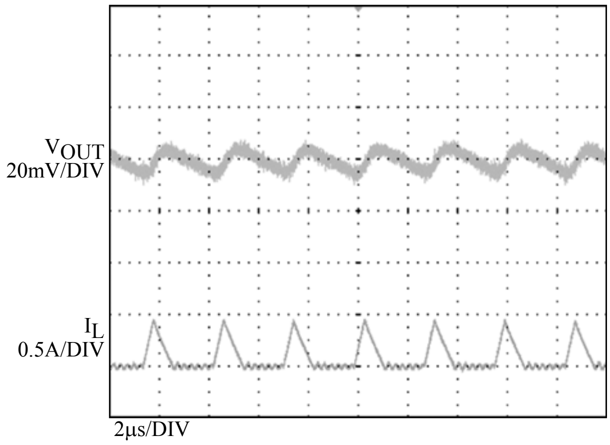




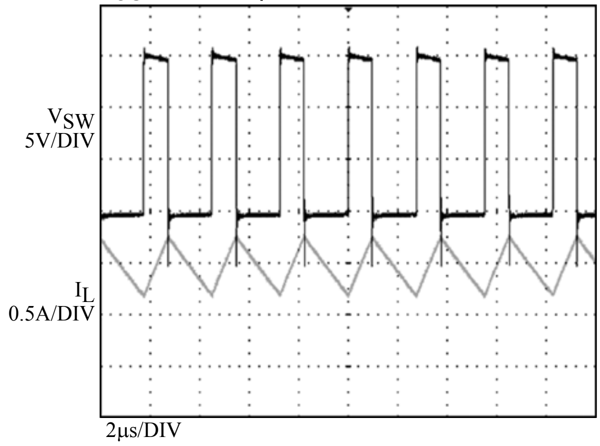
I_{OUT} = 200mA Operate waveform



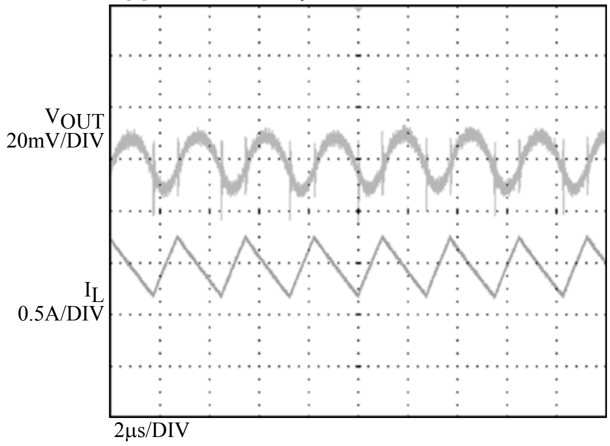
I_{OUT} = 200mA Output waveform



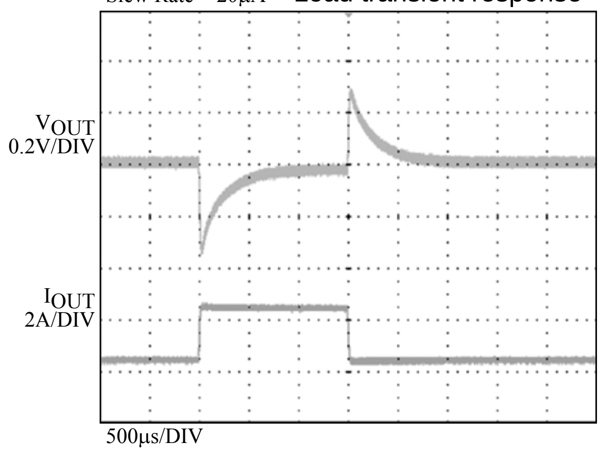
I_{OUT} = 2A Operate waveform



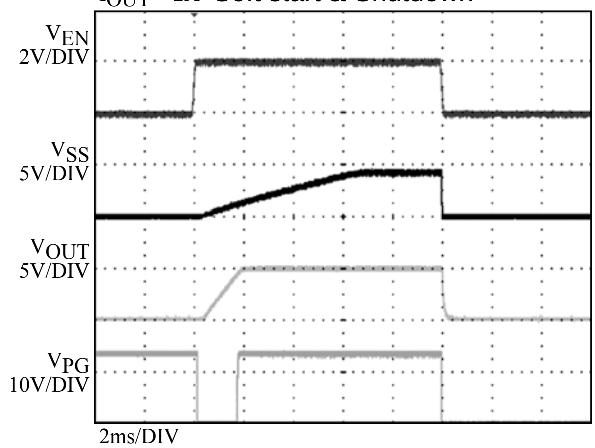
I_{OUT} = 2A Output waveform



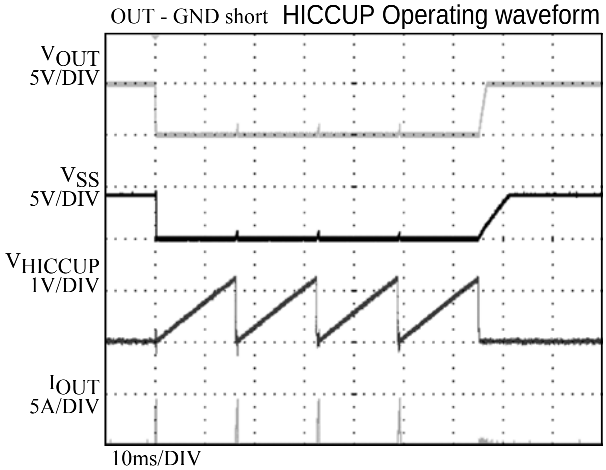
I_{OUT} = 0.5 ⇔ 2.5A,
Slew Rate = 20µA Load transient response



I_{OUT} = 2A Soft start & Shutdown

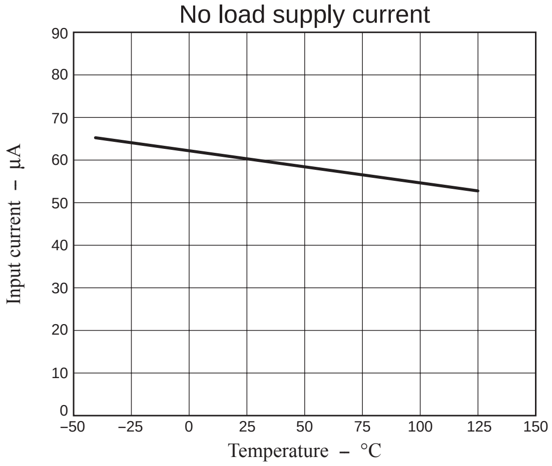


OUT - GND short HICCUP Operating waveform

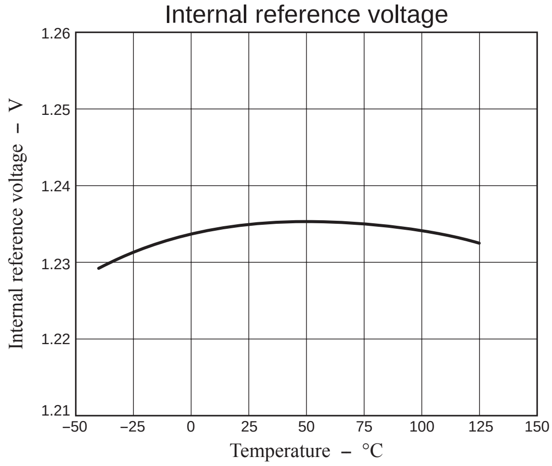


Characterization Curves at Ta = 25°C, V_{IN} = 15V

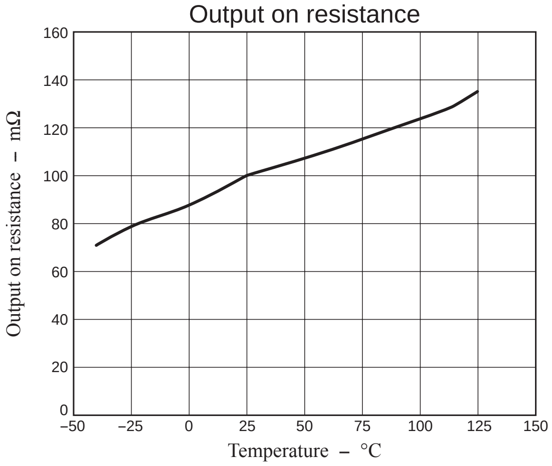
No load supply current



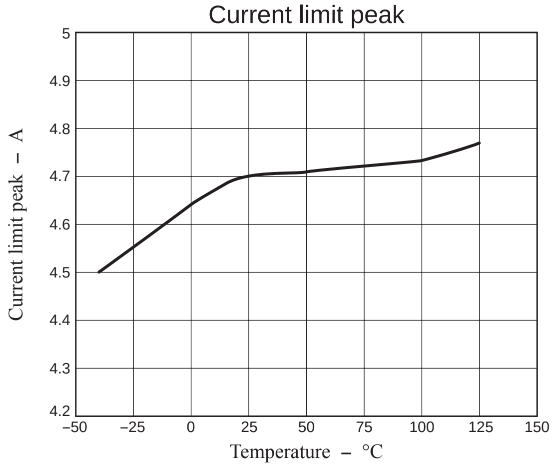
Internal reference voltage



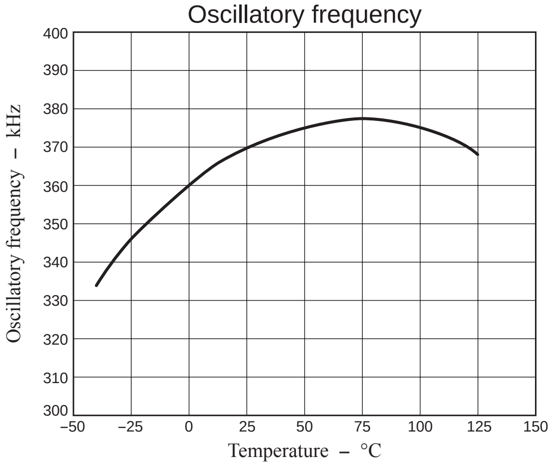
Output on resistance



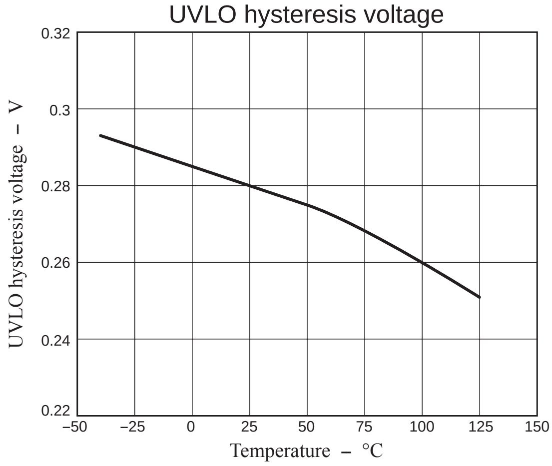
Current limit peak



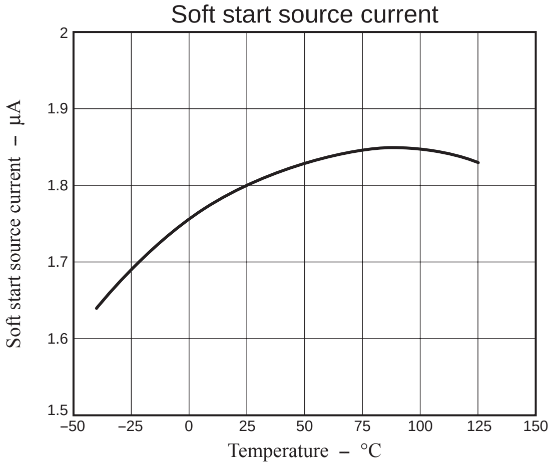
Oscillatory frequency



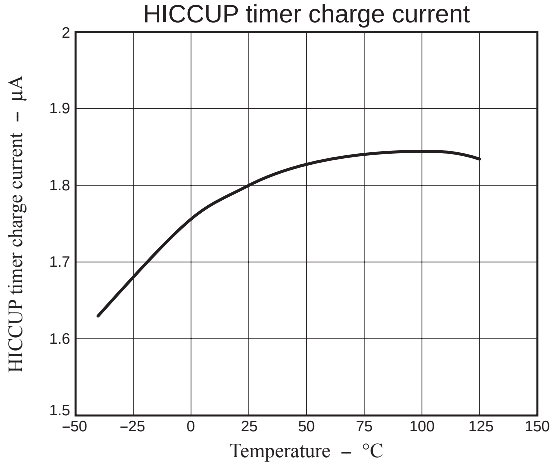
UVLO hysteresis voltage

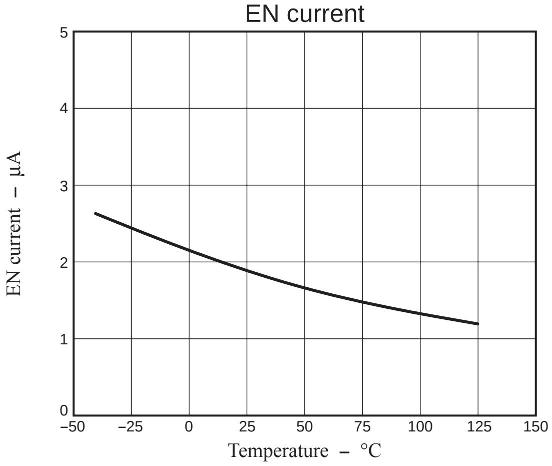


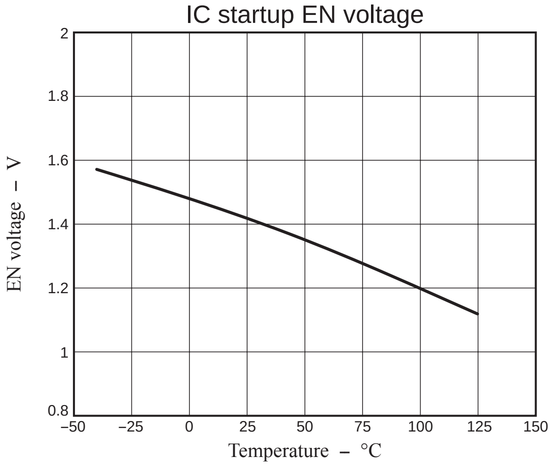
Soft start source current

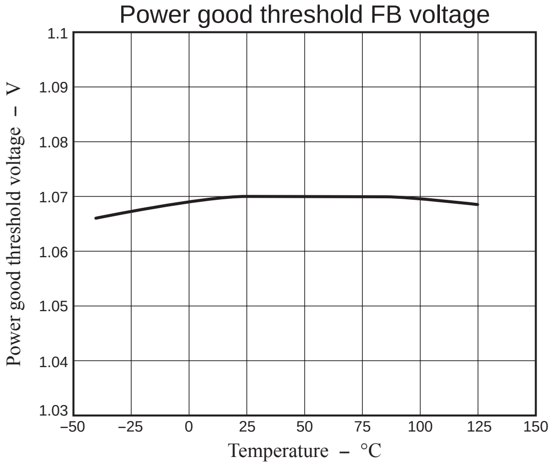


HICCUP timer charge current









This catalog provides information as of October, 2011. Specifications and information herein are subject to change without notice.