

### FEATURES

- Bandwidth: >400 MHz**
- Low insertion loss and on resistance: 2.2  $\Omega$  typical**
- On resistance flatness: 0.3  $\Omega$  typical**
- Single 3 V/5 V supply operation**
- Very low distortion: <0.3%**
- Low quiescent supply current: 1 nA typical**
- Fast switching times**
  - $t_{ON} = 6$  ns
  - $t_{OFF} = 3$  ns
- TTL-/CMOS-compatible**
- Pb-free packages**
  - 16-lead QSSOP
  - 16-lead 3 mm  $\times$  3 mm body LFCSP

### GENERAL DESCRIPTION

The ADG774A is a monolithic CMOS device comprising four 2:1 multiplexer/demultiplexers with high impedance outputs. The CMOS process provides low power dissipation yet offers high switching speed and low on resistance. The on resistance variation is typically less than 0.5  $\Omega$  over the input signal range.

The bandwidth of the ADG774A is typically 400 MHz and this, coupled with low distortion (typically 0.3%), makes the part suitable for switching of high speed data signals.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion. CMOS construction ensures ultralow power dissipation.

The ADG774A operates from a single 3.3 V/5 V supply and is TTL logic-compatible. The control logic for each switch is shown in the truth table (see Table 5).

### FUNCTIONAL BLOCK DIAGRAM

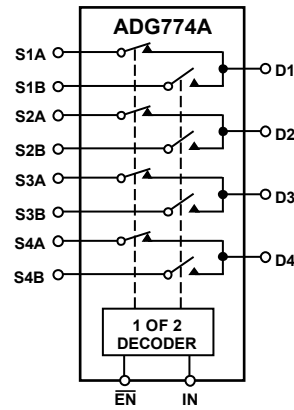


Figure 1.

These switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The ADG774A switches exhibit break-before-make switching action.

### PRODUCT HIGHLIGHTS

1. Wide bandwidth data rates of >400 MHz.
2. Ultralow power dissipation.
3. Low leakage over temperature.
4. Break-before-make switching prevents channel shorting when the switches are configured as a multiplexer.
5. Crosstalk is typically -70 dB @ 10 MHz.
6. Off isolation is typically -65 dB @ 10 MHz.
7. Available in compact 3 mm  $\times$  3 mm LFCSP.

#### Rev. B

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## REVISION HISTORY

### 8/06—Rev. A to Rev. B

Updated Format .....	Universal
Added LFCSP Model.....	Universal
Added Lead-Free Models .....	Universal
Changes to Table 3.....	5
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	13

### 4/03—Rev. 0 to Rev. A

Changes to TPCs 9–11 .....	5
Updated Outline Dimensions .....	8

### 7/01—Revision 0: Initial Version

# SPECIFICATIONS

## SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

**Table 1.**

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	$T_{MIN}$ to $T_{MAX}$		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 to 2.5	V	
On Resistance, $R_{ON}$	2.2		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$
	3.5	4	$\Omega$ max	
On Resistance Match Between Channels, $\Delta R_{ON}$	0.15		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$
		0.5	$\Omega$ max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.3		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$
		0.6	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (OFF)	$\pm 0.001$		nA typ	$V_D = 3\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/3\text{ V}$ , see Figure 17
	$\pm 0.1$	$\pm 0.25$	nA max	
Drain Off Leakage, $I_D$ (OFF)	$\pm 0.001$		nA typ	$V_D = 3\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/3\text{ V}$ , see Figure 17
	$\pm 0.1$	$\pm 0.25$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (ON)	$\pm 0.001$		nA typ	$V_D = V_S = 3\text{ V}/1\text{ V}$ , see Figure 18
	$\pm 0.1$	$\pm 0.25$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$	0.001		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$		3	pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$ , $t_{ON}(\overline{EN})$		6	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 22
		12	ns max	
$t_{OFF}$ , $t_{OFF}(\overline{EN})$		3	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 22
		6	ns max	
Break-Before-Make Time Delay, $t_D$		3	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_{S1} = V_{S2} = 2\text{ V}$ , see Figure 23
		1	ns min	
Off Isolation		-65	dB typ	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 20
Channel-to-Channel Crosstalk		-70	dB typ	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 21
Bandwidth -3 dB		400	MHz typ	$R_L = 50\ \Omega$ , see Figure 19
Distortion		0.3	% typ	$R_L = 100\ \Omega$
Charge Injection		6	pC typ	$C_L = 1\text{ nF}$ , see Figure 24, $V_S = 0\text{ V}$
$C_S$ (OFF)		5	pF typ	
$C_D$ (OFF)		7.5	pF typ	
$C_D$ , $C_S$ (ON)		12	pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$		1	$\mu\text{A}$ max	$V_{DD} = 5.5\text{ V}$
	0.001		$\mu\text{A}$ typ	Digital inputs = $0\text{ V}$ or $V_{DD}$

<sup>1</sup> Temperature range for B version is  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG774A

$V_{DD} = 3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

**Table 2.**

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	$T_{MIN}$ to $T_{MAX}$		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 to 1.5	V	
On Resistance, $R_{ON}$	4		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ ; $I_S = -10\text{ mA}$
	6	7	$\Omega$ max	
On Resistance Match Between Channels, $\Delta R_{ON}$	0.15		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ ; $I_S = -10\text{ mA}$
		0.5	$\Omega$ max	
On Resistance Flatness, $R_{FLAT(ON)}$	1.5		$\Omega$ typ	$V_D = 0\text{ V}$ to $1\text{ V}$ ; $I_S = -10\text{ mA}$
		3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (OFF)	$\pm 0.001$		nA typ	$V_D = 2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/2\text{ V}$ , see Figure 17
	$\pm 0.1$	$\pm 0.25$	nA max	
Drain Off Leakage, $I_D$ (OFF)	$\pm 0.001$		nA typ	$V_D = 2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/2\text{ V}$ , see Figure 17
	$\pm 0.1$	$\pm 0.25$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (ON)	$\pm 0.001$		nA typ	$V_D = V_S = 2\text{ V}/1\text{ V}$ , see Figure 18
	$\pm 0.1$	$\pm 0.25$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.4	V max	
Input Current				
$I_{INL}$ or $I_{INH}$	0.001		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$		3	pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$ , $t_{ON}(\overline{EN})$		7	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 1.5\text{ V}$ , see Figure 22
		14	ns max	
$t_{OFF}$ , $t_{OFF}(\overline{EN})$		4	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 1.5\text{ V}$ , see Figure 22
		8	ns max	
Break-Before-Make Time Delay, $t_D$		3	ns typ	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_{S1} = V_{S2} = 1.5\text{ V}$ , see Figure 23
		1	ns min	
Off Isolation		-65	dB typ	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$
Channel-to-Channel Crosstalk		-70	dB typ	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 21
Bandwidth -3 dB		400	MHz typ	$R_L = 50\ \Omega$ , see Figure 19
Distortion		1.5	% typ	$R_L = 100\ \Omega$
Charge Injection		4	pC typ	$C_L = 1\text{ nF}$ , see Figure 24, $V_S = 0\text{ V}$
$C_S$ (OFF)		5	pF typ	
$C_D$ (OFF)		7.5	pF typ	
$C_D$ , $C_S$ (ON)		12	pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$		1	$\mu\text{A}$ max	$V_{DD} = 3.3\text{ V}$
	0.001		$\mu\text{A}$ typ	Digital inputs = $0\text{ V}$ or $V_{DD}$

<sup>1</sup> Temperature range for B version is  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameters	Rating
$V_{DD}$ to GND	-0.3 V to +6 V
Analog, Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, $\theta_{JA}$	
16-Lead QSSOP	105.44°C/W <sup>2</sup>
16-Lead LFCSP(3 mm × 3 mm)	48.7°C/W <sup>2</sup>
Lead Temperature Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Reflow Soldering (Pb-free)	
Peak Temperature	260°C (+0°C/-5°C)
Time at Peak Temperature	10 sec to 40 sec

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

<sup>2</sup> Measured with the device soldered on a four-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG774A

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

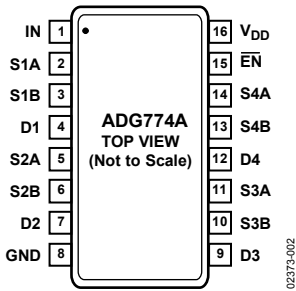
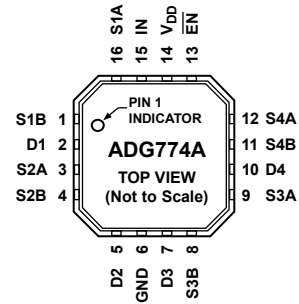


Figure 2. QSOP Pin Configuration



- NOTES**  
 1. THE EXPOSED PAD SHOULD BE TIED TO GND.

Figure 3. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.		Mnemonic	Function
QSOP	LFCSP		
1	15	IN	Logic Control Input.
2	16	S1A	Source Terminal 1A. May be an input or output.
3	1	S1B	Source Terminal 1B. May be an input or output.
4	2	D1	Drain Terminal D1. May be an input or output.
5	3	S2A	Source Terminal 2A. May be an input or output.
6	4	S2B	Source Terminal 2B. May be an input or output.
7	5	D2	Drain Terminal D2. May be an input or output.
8	6	GND	Ground (0 V) Reference.
9	7	D3	Drain Terminal D3. May be an input or output.
10	8	S3B	Source Terminal 3B. May be an input or output.
11	9	S3A	Source Terminal 3A. May be an input or output.
12	10	D4	Drain Terminal D4. May be an input or output.
13	11	S4B	Source Terminal 4B. May be an input or output.
14	12	S4A	Source Terminal 4A. May be an input or output.
15	13	EN	Logic Control Input. When high, all switches are disabled.
16	14	V <sub>DD</sub>	Most Positive Power Supply Potential.

Table 5. Truth Table

EN	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

# TYPICAL PERFORMANCE CHARACTERISTICS

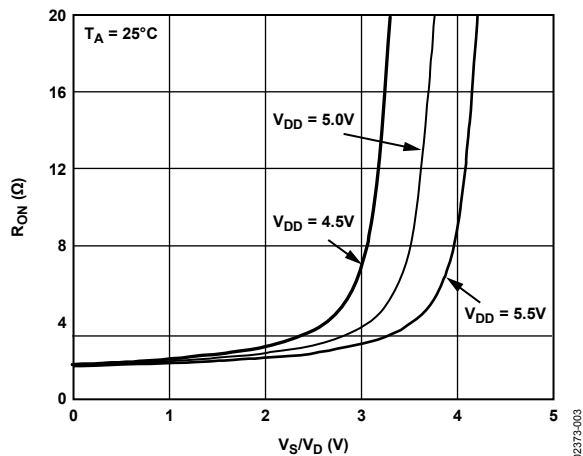


Figure 4. On Resistance as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for  $V_{DD} = 5 V \pm 10\%$

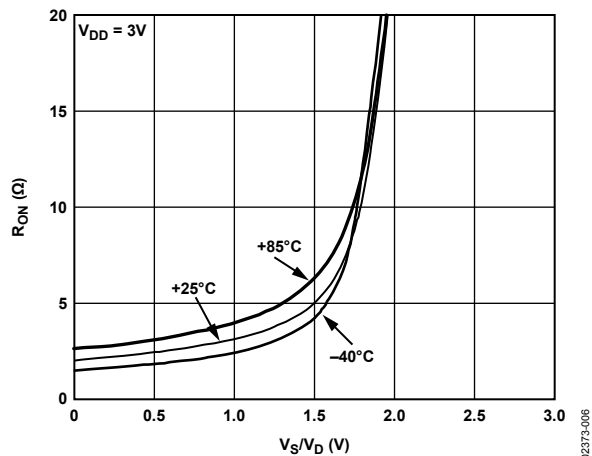


Figure 7. On Resistance as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for Different Temperatures with 3 V Single Supplies

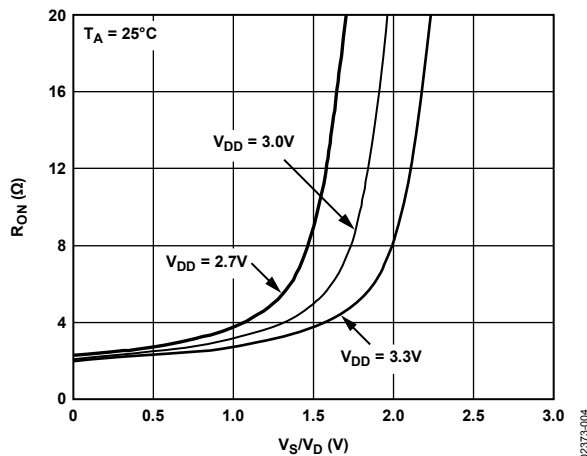


Figure 5. On Resistance as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for  $V_{DD} = 3 V \pm 10\%$

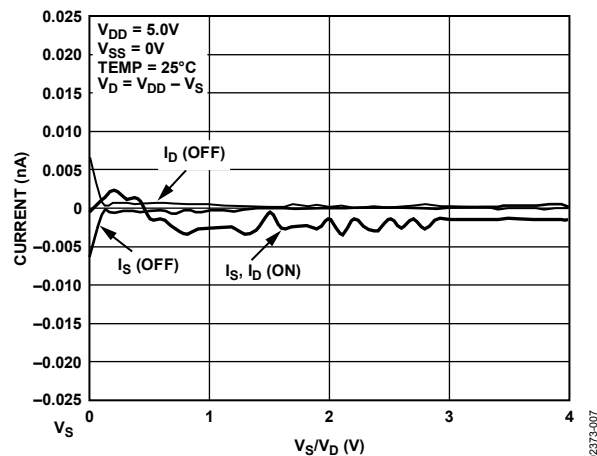


Figure 8. Leakage Current as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for  $V_{DD} = 5 V$

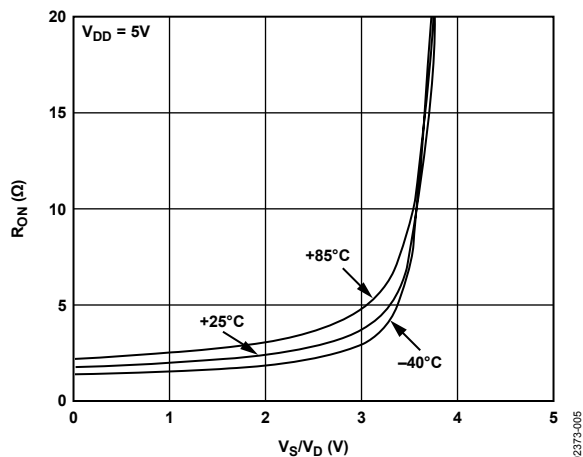


Figure 6. On Resistance as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for Different Temperatures with 5 V Single Supplies

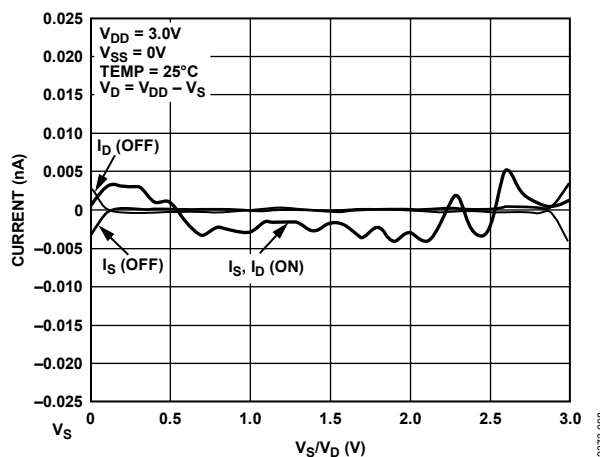


Figure 9. Leakage Current as a Function of Drain ( $V_D$ ) or Source ( $V_S$ ) Voltage for  $V_{DD} = 3 V$

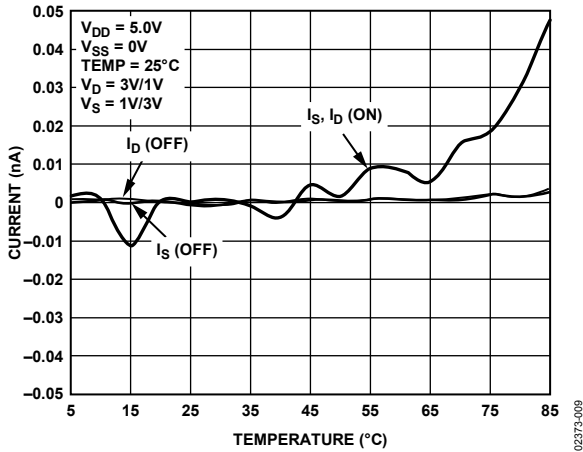


Figure 10. Leakage Current as a Function of Temperature,  $V_{DD} = 5V$

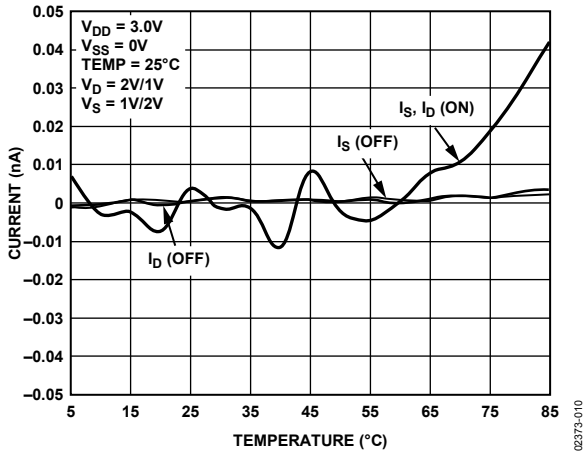


Figure 11. Leakage Current as a Function of Temperature,  $V_{DD} = 3V$

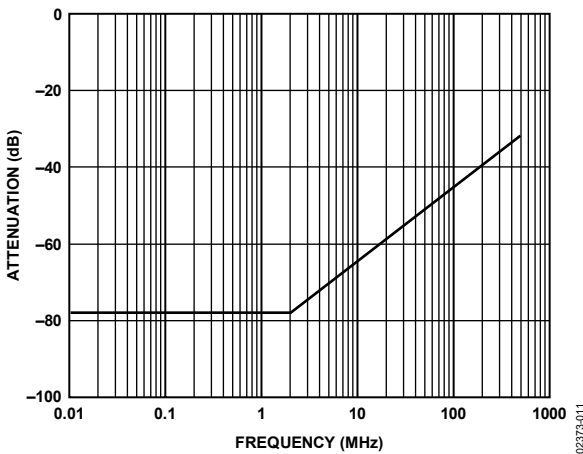


Figure 12. Off Isolation vs. Frequency

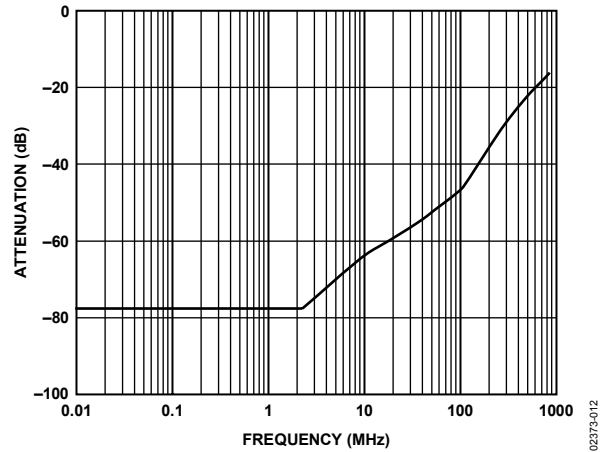


Figure 13. Crosstalk vs. Frequency

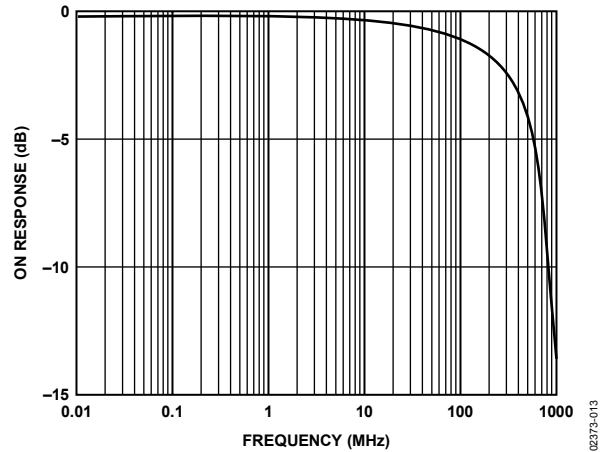


Figure 14. Bandwidth

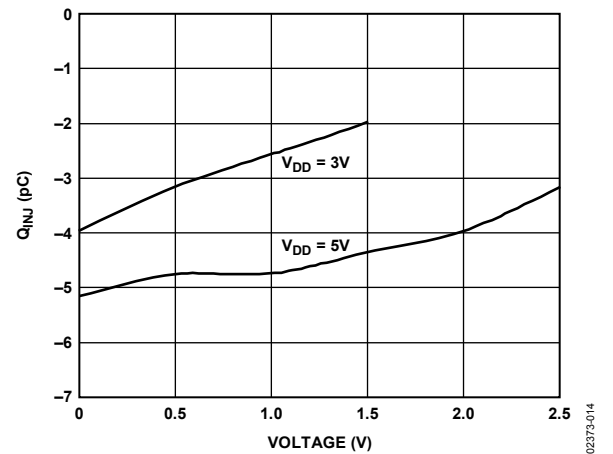


Figure 15. Charge Injection vs. Source Voltage



TEST CIRCUITS

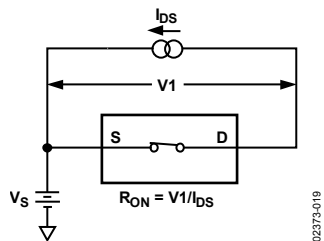


Figure 16. On Resistance

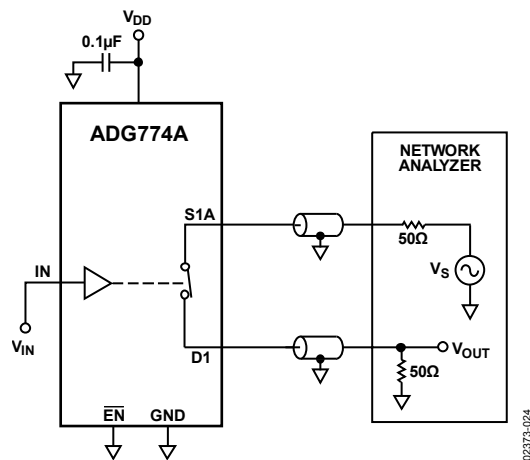


Figure 19. Bandwidth

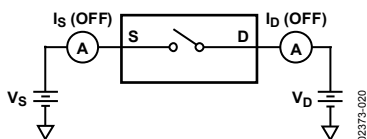


Figure 17. Off Leakage

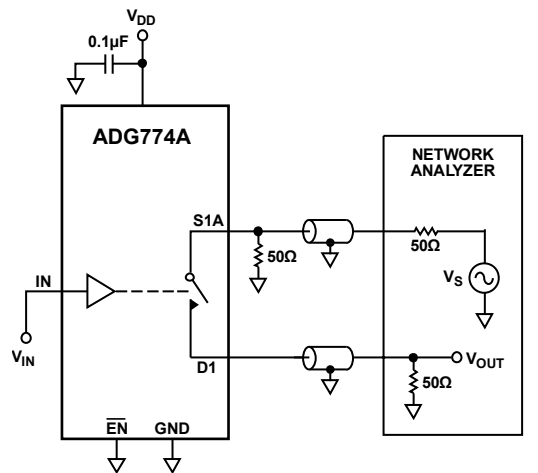


Figure 20. Off Isolation

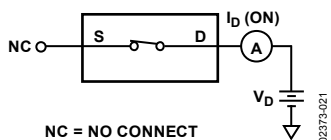


Figure 18. On Leakage

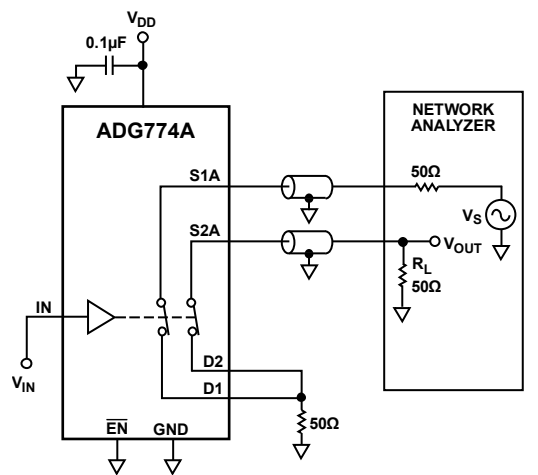


Figure 21. Channel-to-Channel Crosstalk

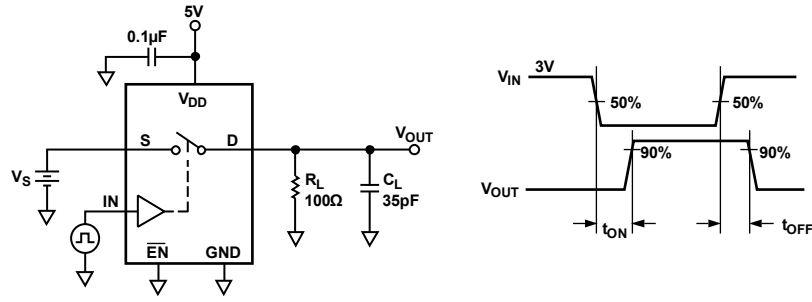


Figure 22. Switching Times

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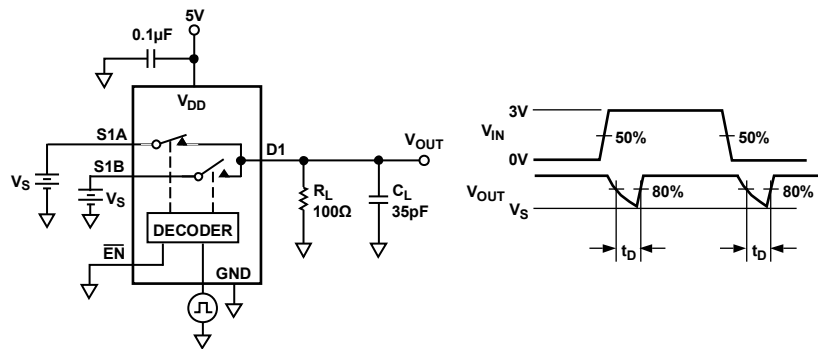


Figure 23. Break-Before-Make Time Delay

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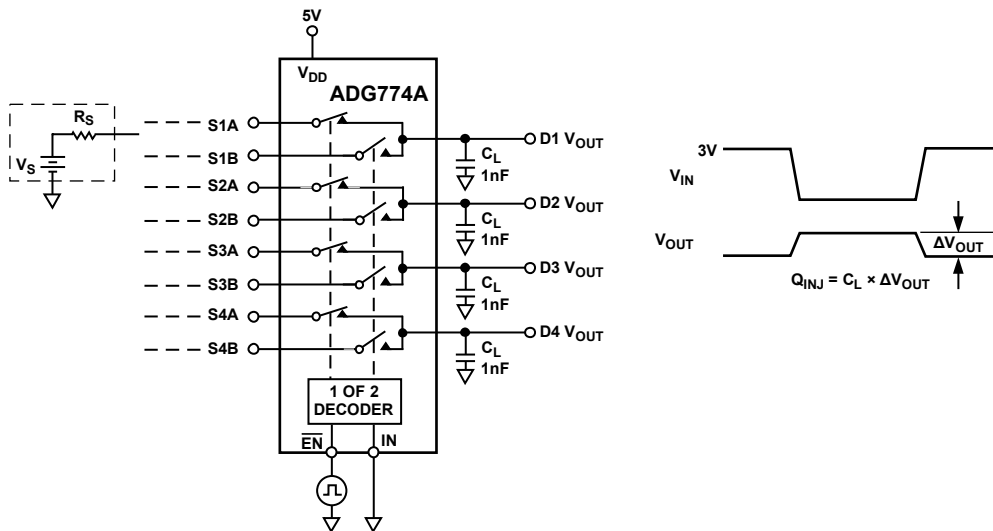


Figure 24. Charge Injection

02373-027

## TERMINOLOGY

### $V_{DD}$

Most positive power supply potential.

### GND

Ground (0 V) reference.

### S

Source terminal. May be an input or output.

### D

Drain terminal. May be an input or output.

### IN

Logic control input.

### $\overline{\text{EN}}$

Logic control input.

### $R_{ON}$

Ohmic resistance between D and S.

### $\Delta R_{ON}$

On resistance match between any two channels, that is,  $R_{ON \text{ max}} - R_{ON \text{ min}}$ .

### $R_{\text{FLAT(ON)}}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### $I_S$ (OFF)

Source leakage current with the switch off.

### $I_D$ (OFF)

Drain leakage current with the switch off.

### $I_D, I_S$ (ON)

Channel leakage current with the switch on.

### $V_D$ ( $V_S$ )

Analog voltage on the D and S terminals.

### $C_S$ (OFF)

Off switch source capacitance.

### $C_D$ (OFF)

Off switch drain capacitance.

### $C_D, C_S$ (ON)

On switch capacitance.

### $t_{ON}$

Delay between applying the digital control input and the output switching on. See Figure 22.

### $t_{OFF}$

Delay between applying the digital control input and the output switching off.

### $t_D$

Off time or on time measured between the 80% points of both switches when switching from one address state to another. See Figure 23.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Bandwidth

Frequency response of the switch in the on state measured at 3 dB down.

### Distortion

$R_{\text{FLAT(ON)}}/R_L$

## APPLICATION CIRCUITS

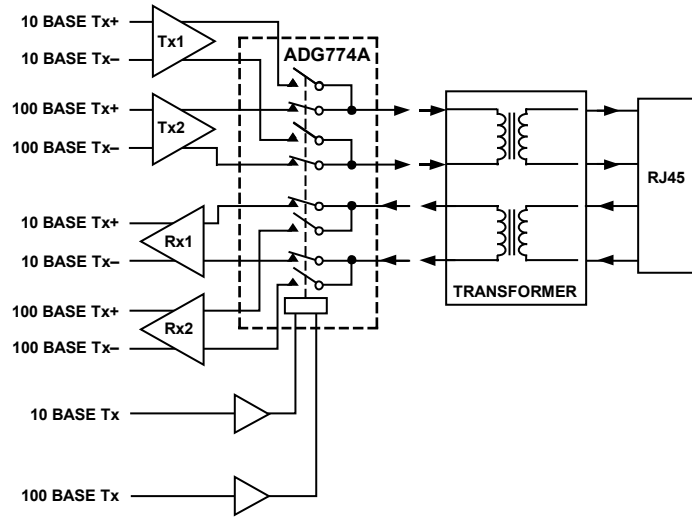


Figure 25. Full Duplex Transceiver

02373-015

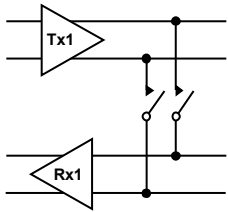


Figure 26. Loop Back

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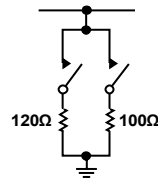


Figure 27. Line Termination

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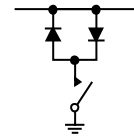


Figure 28. Line Clamp

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