

# Dual, Fast, Accurate Step-Down DC/DC Controller with External Reference Voltage and Dual Differential Output Sensing

## FEATURES

- Wide  $V_{IN}$  Range: 4.5V to 38V
- $V_{OUT1}$ : 0.6V to 5.5V,  $\pm 0.67\%$  Output Regulation Accuracy, with Internal 0.6V  $V_{REFERENCE}$
- $V_{OUT2}$ : 0.4V to 5.5V,  $\pm 4mV$  Regulation Accuracy, with Differential External  $V_{REFERENCE}$  Sensing
- Differential Remote Output Sensing; Up to  $\pm 500mV$  ( $V_{OUT1}$ ) and  $\pm 200mV$  ( $V_{OUT2}$ ) Ground Deviations
- Fast Load Transient Response Without Clock Delay
- Detect Transient Release (DTR) Reduces  $V_{OUT}$  Overshoot
- Frequency Programmable from 200kHz to 2MHz, Synchronizable to External Clock
- $t_{ON(MIN)} = 30ns$ ,  $t_{OFF(MIN)} = 90ns$
- $R_{SENSE}$  or Inductor DCR Current Sensing
- Overvoltage Protection and Current Limit Foldback
- Power Good Output Voltage Monitor
- Thermally Enhanced 38-Pin (5mm  $\times$  7mm) QFN Package

## APPLICATIONS

- Power for ASICs with Dynamic Voltage Scaling
- Low Voltage, High Current, High Step-Down Ratio Converters That Demand Tight Transient Regulation

## DESCRIPTION

The LTC<sup>®</sup>3838-2 is a dual-channel, PolyPhase<sup>®</sup> synchronous step-down DC/DC switching regulator controller. Two independent channels drive all N-channel power MOSFETs. The two channels can also be combined into a multiphase single output configuration with external reference.

The controlled on-time, valley current mode control architecture allows for not only fast response to transients without a clock delay, but also constant frequency switching at a steady-load condition. Its proprietary load-release transient detection feature (DTR) significantly reduces overshoot at low output voltages.

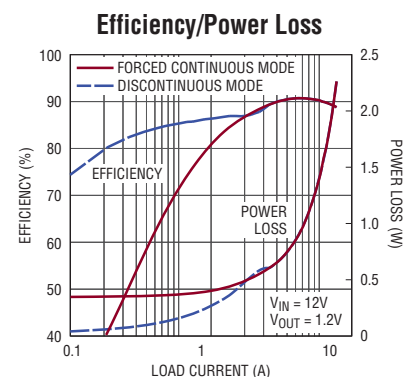
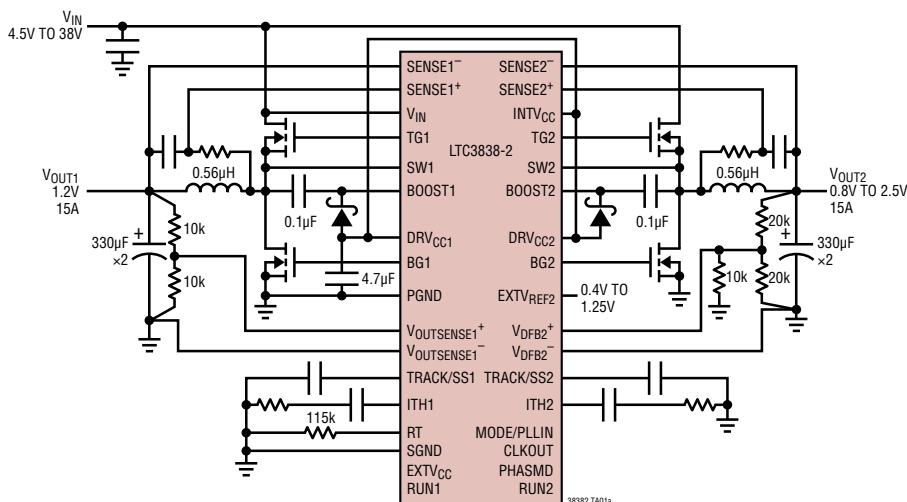
The switching frequency can be programmed from 200kHz to 2MHz with an external resistor, and can be synchronized to an external clock. Very low  $t_{ON}$  and  $t_{OFF}$  times allow for near 0% and near 100% duty cycles, respectively. Voltage tracking soft start-up and multiple safety features are provided.

See Table 1 for a comparison of LTC3838, LTC3838-1 and LTC3838-2.

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## TYPICAL APPLICATION

1.2V/15A and 0.8V to 2.5V/15A, 350kHz Step-Down Converter (See Figure 16 for Complete Design)



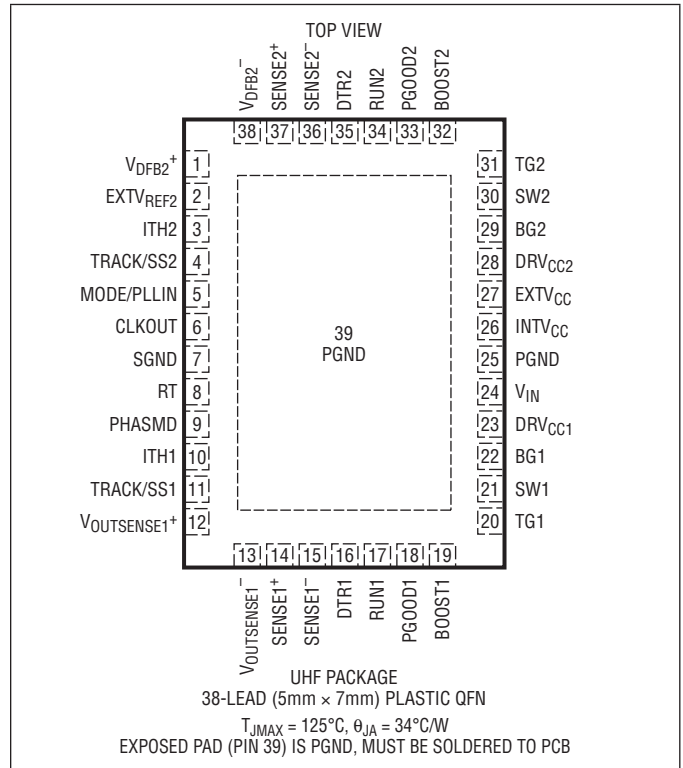
# LTC3838-2

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ Voltage	-0.3V to 40V
BOOST1, BOOST2 Voltages	-0.3V to 46V
SW1, SW2 Voltages	-5V to 40V
INTV <sub>CC</sub> , DRV <sub>CC1</sub> , DRV <sub>CC2</sub> , EXTV <sub>CC</sub> , PGOOD1, PGOOD2, RUN1, RUN2, (BOOST1-SW1), (BOOST2-SW2), MODE/PLLIN Voltages	-0.3V to 6V
SENSE1 <sup>+</sup> , SENSE2 <sup>+</sup> , SENSE1 <sup>-</sup> , SENSE2 <sup>-</sup> Voltages	-0.6V to 6V
$V_{OUTSENSE1+}$ , Voltage	-0.6V to (INTV <sub>CC</sub> + 0.3V)
$V_{OUTSENSE1-}$ , Voltage	-0.6V to $V_{OUTSENSE1+}$
TRACK/SS1, TRACK/SS2 Voltages	-0.3V to 5V
DTR1, DTR2, PHASMD, RT, EXTV <sub>REF2</sub> , $V_{DFB2+}$ , $V_{DFB2-}$ , ITH1, ITH2 Voltages	-0.3V to (INTV <sub>CC</sub> + 0.3V)
Operating Junction Temperature Range (Notes 2, 3, 4)	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3838EUHF-2#PBF	LTC3838EUHF-2#TRPBF	38382	38-Lead (5mm × 7mm) Plastic QFN	-40°C to 125°C
LTC3838IUHF-2#PBF	LTC3838IUHF-2#TRPBF	38382	38-Lead (5mm × 7mm) Plastic QFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

Table 1. Comparison of LTC3838 Options

PART NUMBER	DESCRIPTION
LTC3838	±0.67% Differential Output Regulation on Channel 1 ±1% Output Regulation on Channel 2 Separate-Per-Channel Continuous 30mV to 100mV Current Sense Range Controls
LTC3838-1	±0.67% on Channel 1 and ±0.75% on Channel 2, Differential Output Regulation on Both Channel 1 and 2 Single-Pin 30mV/60mV Current Sense Range Control
LTC3838-2	±0.67% Differential Output Regulation with Internal Reference on Channel 1 ±4mV Differential Output Regulation with External Reference Voltage on Channel 2 Fixed 30mV Current Sense Range

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$  unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Main Control Loops</b>							
$V_{IN}$	Input Voltage Operating Range		4.5		38	V	
$V_{OUT1,2}$	Regulated Output Voltage Operating Range	$V_{OUT1}$ Regulated Differentially with Respect to $V_{OUTSENSE1^-}$ , $V_{OUT2}$ Regulated Differentially with Respect to $V_{DFB2^-}$	0.6		5.5	V	
$I_Q$	Input DC Supply Current Both Channels Enabled Only One Channel Enabled Shutdown Supply Current	MODE/PLLIN = 0V, No Load		3		mA	
		RUN1 or RUN2 (But Not Both) = 0V		2		mA	
		RUN1 = RUN2 = 0V		15		$\mu\text{A}$	
$V_{FB1}$	Regulated Feedback Voltage on Channel 1 ( $V_{OUTSENSE1^+} - V_{OUTSENSE1^-}$ )	ITH1 = 1.2V, $V_{OUTSENSE1^-} = 0\text{V}$ (Note 5) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	● 0.5985 ● 0.596 ● 0.594	0.6	0.6015 0.604 0.606	V V V	
	Regulated Feedback Voltage on Channel 1 Over Line, Load and Common Mode	$V_{IN} = 4.5\text{V}$ to $38\text{V}$ , ITH1 = 0.5V to 1.9V, $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ (Note 5) $-0.5\text{V} < V_{OUTSENSE1^-} < 0.5\text{V}$	● 0.591	0.6	0.609	V	
$V_{FB2}$	Regulated Feedback Voltage on Channel 2 ( $2 \cdot V_{DFB2^+} - V_{DFB2^-}$ )	$V_{DFB2^-} = 0\text{V}$ , ITH2 = 1.2V (Note 5) EXTVREF2 = 0.6V, $T_A = 25^\circ\text{C}$		0.598	0.6	0.602	V
	Regulated Feedback Voltage on Channel 2 Over Line, Load and Common Mode	ITH2 = 0.5V to 1.9V, $-0.2\text{V} < V_{DFB2^-} < 0.2\text{V}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ (Note 5) EXTVREF2 = 0.6V, $V_{IN} = 4.5\text{V}$ to $38\text{V}$ EXTVREF2 = 1.5V, $V_{IN} = 4.5\text{V}$ to $38\text{V}$ EXTVREF2 = 2.5V, $V_{IN} = 5.5\text{V}$ to $38\text{V}$	● 0.596 ● 1.494 ● 2.493	0.6	0.604 1.506 2.507	V V V	
$I_{VOUTSENSE1^+}$	$V_{OUTSENSE1^+}$ Input Bias Current	$V_{OUTSENSE1^+} = 0.6\text{V}$ , $V_{OUTSENSE1^-} = 0\text{V}$		0	$\pm 25$	nA	
$I_{VOUTSENSE1^-}$	$V_{OUTSENSE1^-}$ Input Bias Current	$V_{OUTSENSE1^+} = 0.6\text{V}$ , $V_{OUTSENSE1^-} = 0\text{V}$		-25	-50	$\mu\text{A}$	
$I_{EXTVREF2}$	EXTVREF2 Input Bias Current	EXTVREF2 = 0.6V		-5	$\pm 50$	nA	
$V_{EXTVREF2}$	Maximum EXTVREF2 Input Operating Voltage	$V_{IN} \geq \text{INTV}_{CC} \geq 5\text{V}$ , TRACK/SS2 > 2.5V $V_{IN} \geq \text{INTV}_{CC} \geq 4\text{V}$ , TRACK/SS2 > 1.5V	● 2.5 ● 1.5			V V	
	Minimum EXTVREF2 Input Operating Voltage		●		0.4	V	
$I_{VDFB2^+}$	$V_{DFB2^+}$ Input Bias Current	$V_{DFB2^+} = 0.3\text{V}$ , $V_{DFB2^-} = 0\text{V}$		0	$\pm 25$	nA	
$I_{VDFB2^-}$	$V_{DFB2^-}$ Input Bias Current	$V_{DFB2^+} = 0.3\text{V}$ , $V_{DFB2^-} = 0\text{V}$		-6	-12	$\mu\text{A}$	
$g_{m(EA)1,2}$	Error Amplifier Transconductance ( $\Delta I_{TH1,2} / \Delta V_{FB1,2}$ )	ITH = 1.2V (Note 5)		1.7		mS	
$t_{ON(MIN)1,2}$	Minimum Top Gate On-Time	$V_{IN} = 38\text{V}$ , $V_{OUT} = 0.6\text{V}$ , $R_T = 20\text{k}$ (Note 6)		30		ns	
$t_{OFF(MIN)1,2}$	Minimum Top Gate Off-Time	(Note 6)		90		ns	
<b>Current Sensing</b>							
$V_{SENSE(MAX)1,2}$	Maximum Valley Current Sense Threshold ( $V_{SENSE1,2^+} - V_{SENSE1,2^-}$ )	$V_{OUTSENSE1^+} = 0.57\text{V}$ , $V_{OUTSENSE1^-} = 0\text{V}$ , EXTVREF2 = 0.6V, $V_{DFB2^+} = 0.285\text{V}$ , $V_{DFB2^-} = 0\text{V}$ , $V_{SENSE1,2^-} = 2.5\text{V}$	●	24	30	36	mV
$V_{SENSE(MIN)1,2}$	Minimum Valley Current Sense Threshold ( $V_{SENSE1,2^+} - V_{SENSE1,2^-}$ ) (Forced Continuous Mode)	$V_{OUTSENSE1^+} = 0.63\text{V}$ , $V_{OUTSENSE1^-} = 0\text{V}$ , EXTVREF2 = 0.6V, $V_{DFB2^+} = 0.315\text{V}$ , $V_{DFB2^-} = 0\text{V}$ , $V_{SENSE1,2^-} = 2.5\text{V}$			-15		mV
$I_{SENSE1,2^+}$	SENSE1,2 <sup>+</sup> Pins Input Bias Current	$V_{SENSE^+} = 0.6\text{V}$		$\pm 5$	$\pm 50$	nA	
		$V_{SENSE^+} = 5\text{V}$		1	$\pm 2$	$\mu\text{A}$	
$I_{SENSE1,2^-}$	SENSE1,2 <sup>-</sup> Pins Input Bias Current (Internal 500k Resistor to SGND)	$V_{SENSE^-} = 0.6\text{V}$		1.2		$\mu\text{A}$	
		$V_{SENSE^-} = 5\text{V}$		10		$\mu\text{A}$	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$  unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Start-Up and Shutdown</b>						
$V_{RUN1,2}$	RUN Pin On Threshold	$V_{RUN1,2}$ Rising	● 1.1	1.2	1.3	V
	RUN Pin On Hysteresis	$V_{RUN1,2}$ Falling from On Threshold		100		mV
$I_{RUN1,2}$	RUN Pin Pull-Up Current when Off	$RUN1,2 = SGND$		1.2		$\mu\text{A}$
	RUN Pin Pull-Up Current Hysteresis	$I_{RUN1,2(HYS)} = I_{RUN1,2(ON)} - I_{RUN1,2(OFF)}$		5		$\mu\text{A}$
UVLO	INTV <sub>CC</sub> Undervoltage Lockout	INTV <sub>CC</sub> Falling	● 3.3	3.7		V
		INTV <sub>CC</sub> Rising	●	4.2	4.5	V
$I_{TRACK/SS1,2}$	Soft-Start Pull-Up Current	$0\text{V} < TRACK/SS1,2 < 0.6\text{V}$		1		$\mu\text{A}$
<b>Frequency and Clock Synchronization</b>						
f	Clock Output Frequency (Steady-State Switching Frequency)	$R_T = 205\text{k}$ $R_T = 80.6\text{k}$ $R_T = 18.2\text{k}$		450 200 500 2000	550	kHz kHz kHz
	Channel 2 Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = INTV <sub>CC</sub>		180 180 240		Deg Deg Deg
	CLKOUT Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = INTV <sub>CC</sub>		60 90 120		Deg Deg Deg
$V_{PLLIN(H)}$	Clock Input High Level Into MODE/PLLIN		2			V
$V_{PLLIN(L)}$	Clock Input Low Level Into MODE/PLLIN				0.5	V
$R_{MODE/PLLIN}$	MODE/PLLIN Input DC Resistance	With Respect to SGND		600		k $\Omega$
<b>Gate Drivers</b>						
$R_{TG(UP)1,2}$	TG Driver Pull-Up On Resistance	TG High		2.5		$\Omega$
$R_{TG(DOWN)1,2}$	TG Driver Pull-Down On Resistance	TG Low		1.2		$\Omega$
$R_{BG(UP)1,2}$	BG Driver Pull-Up On Resistance	BG High		2.5		$\Omega$
$R_{BG(DOWN)1,2}$	BG Driver Pull-Down On Resistance	BG Low		0.8		$\Omega$
$t_{D(TG/BG)1,2}$	Top Gate Off to Bottom Gate On Delay Time	(Note 6)		20		ns
$t_{D(BG/TG)1,2}$	Bottom Gate Off to Top Gate On Delay Time	(Note 6)		15		ns
<b>Internal V<sub>CC</sub> Regulator</b>						
$V_{DRVCC1}$	Internally Regulated DRV <sub>CC1</sub> Voltage	$6\text{V} < V_{IN} < 38\text{V}$	5.0	5.3	5.6	V
	DRV <sub>CC1</sub> Load Regulation	$I_{DRVCC1} = 0\text{mA}$ to $-100\text{mA}$		-1.5	-3	%
$V_{EXTVCC}$	EXTV <sub>CC</sub> Switchover Voltage	EXTV <sub>CC</sub> Rising	4.4	4.6	4.8	V
	EXTV <sub>CC</sub> Switchover Hysteresis			200		mV
	EXTV <sub>CC</sub> to DRV <sub>CC2</sub> Voltage Drop	$V_{EXTVCC} = 5\text{V}$ , $I_{DRVCC2} = -100\text{mA}$		200		mV
<b>PGood Output</b>						
OV	PGOOD Overvoltage Threshold	$V_{FB1,2}$ Rising from Regulated Voltage	5	7.5	10	%
UV	PGOOD Undervoltage Threshold	$V_{FB1,2}$ Falling from Regulated Voltage	-5	-7.5	-10	%
	PGOOD Threshold Hysteresis	$V_{FB1,2}$ Returning to Regulated Voltage		15		mV
$V_{PGOOD(L)1,2}$	PGOOD Low Voltage	$I_{PGOOD} = 2\text{mA}$		0.1	0.3	V
$t_{D(PGOOD)1,2}$	Delay from $V_{FB}$ Fault (OV/UV) to PGOOD Falling Delay from $V_{FB}$ Good (OV/UV Cleared) to PGOOD Rising			50 20		$\mu\text{s}$ $\mu\text{s}$

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The junction temperature ( $T_J$ , in  $^{\circ}\text{C}$ ) is calculated from the ambient temperature ( $T_A$ , in  $^{\circ}\text{C}$ ) and power dissipation ( $P_D$ , in Watts) according to the formula:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where  $\theta_{JA}$  (in  $^{\circ}\text{C}/\text{W}$ ) is the package thermal impedance.

**Note 3:** The LTC3838-2 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTC3838E-2 is guaranteed to meet specifications over the  $0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  operating junction temperature range. Specifications over the  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3838I-2 is guaranteed to meet specifications over the  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum

rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 5:** The LTC3838-2 is tested in a feedback loop that adjusts voltages on  $V_{\text{OUTSENSE1}^+}$  and  $V_{\text{DFB2}^+}$  pins to achieve specified error amplifier output voltages (ITH1,2).

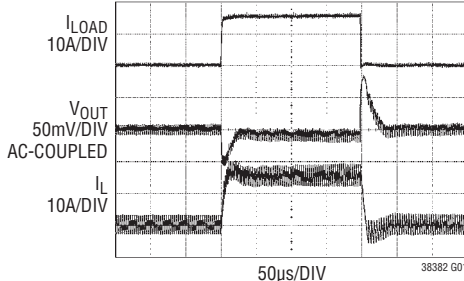
In order to simplify the total system error computation, the regulated voltage is defined in one combined specification which includes the effects of line, load and common mode variation. The combined regulated voltage specification is tested by independently varying line, load, and common mode, which by design do not significantly affect one another. For any combination of line, load, and common mode variation, the regulated voltage should be within the limits specified that are tested in production to the following conditions:

Line:  $V_{\text{IN}} = 4.5\text{V to } 38\text{V}$ ,  $\text{ITH} = 1.2\text{V}$ ,  $V_{\text{OUTSENSE1}^-} = 0\text{V}$ ,  $V_{\text{DFB2}^-} = 0\text{V}$   
 Load:  $V_{\text{IN}} = 15\text{V}$ ,  $\text{ITH} = 0.5\text{V to } 1.9\text{V}$ ,  $V_{\text{OUTSENSE1}^-} = 0\text{V}$ ,  $V_{\text{DFB2}^-} = 0\text{V}$   
 Common mode:  $V_{\text{IN}} = 15\text{V}$ ,  $\text{ITH} = 1.2\text{V}$ ,  $V_{\text{OUTSENSE1}^-} = \pm 0.5\text{V}$ ,  $\pm 0.2\text{V}$ ,  
 $V_{\text{DFB2}^-} = \pm 0.2\text{V}$ .

**Note 6:** Delay times are measured with top gate (TG) and bottom gate (BG) driving minimum load, and using 50% levels.

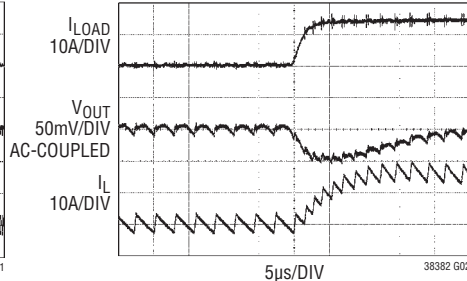
## TYPICAL PERFORMANCE CHARACTERISTICS

**Transient Response  
(Forced Continuous Mode)**



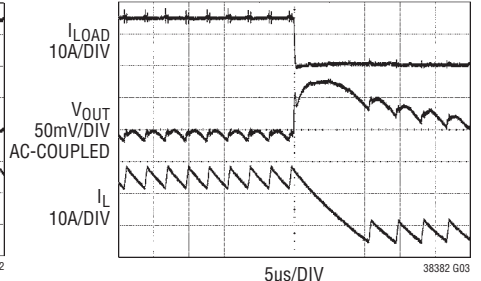
LOAD TRANSIENT = 0A TO 15A TO 0A  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Load Step  
(Forced Continuous Mode)**



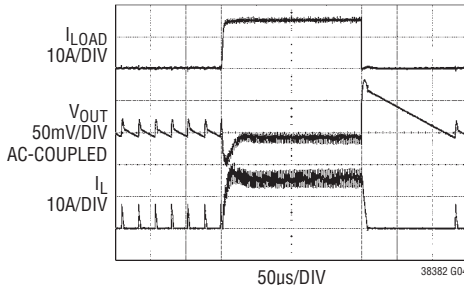
LOAD STEP = 0A TO 15A  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Load Release  
(Forced Continuous Mode)**



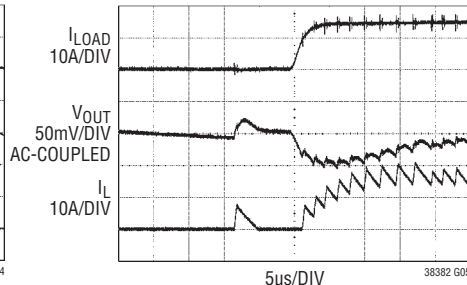
LOAD RELEASE = 15A TO 0A  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Transient Response  
(Discontinuous Mode)**



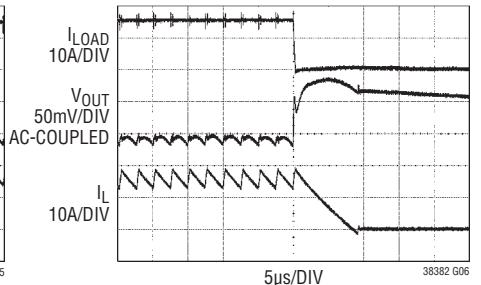
LOAD TRANSIENT = 500mA TO 15A TO 500mA  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Load Step  
(Discontinuous Mode)**



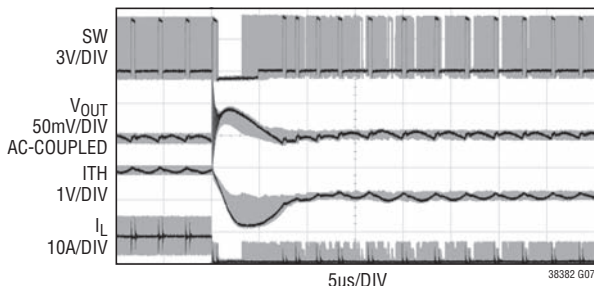
LOAD STEP = 500mA TO 15A  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Load Release  
(Discontinuous Mode)**



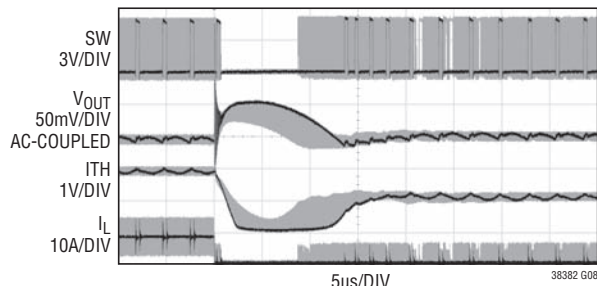
LOAD RELEASE = 15A TO 500mA  
 $V_{IN} = 12V$   
 $V_{OUT} = 1.2V$   
 FIGURE 17 CIRCUIT, CHANNEL 1

**Load Release with Detect Transient (DTR)  
Feature Enabled**



LOAD RELEASE = 15A TO 5A  
 $V_{IN} = 5V$   
 $V_{OUT} = 0.6V$   
 FIGURE 17 CIRCUIT, CHANNEL 1 MODIFIED:  
 $R_{FB2} = 0\Omega$ ,  $C_{ITH1} = 120pF$ ,  $C_{ITH2} = 0pF$   
 FROM DTR1 PIN:  $R_{ITH1} = 46.4k$  TO SGND,  $R_{ITH2} = 42.2k$  TO INTV<sub>CC</sub>  
 SHADING OBTAINED WITH INFINITE PERSISTENCE ON  
 OSCILLOSCOPE WAVEFORMS

**Load Release with Detect Transient (DTR)  
Feature Disabled**

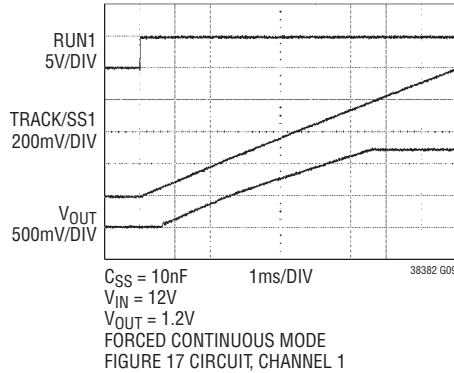


LOAD RELEASE = 15A TO 5A  
 $V_{IN} = 5V$   
 $V_{OUT} = 0.6V$   
 FIGURE 17 CIRCUIT, CHANNEL 1 MODIFIED:  
 $R_{FB2} = 0\Omega$ ,  $C_{ITH1} = 120pF$ ,  $C_{ITH2} = 0pF$   
 $R_{ITH1/2} = 46.4k$  TO SGND//42.2k TO INTV<sub>CC</sub>,  
 CONNECTION FROM  $R_{ITH1/2}$  AND  $C_{ITH1}$  TO DTR1 PIN REMOVED.  
 DTR1 PIN TIED TO INTV<sub>CC</sub>

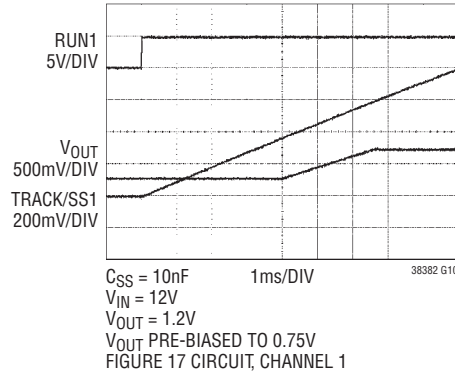
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# TYPICAL PERFORMANCE CHARACTERISTICS

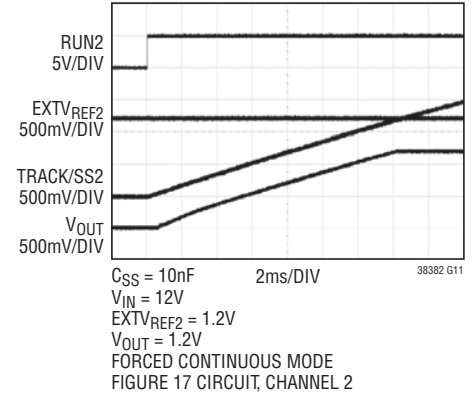
## Soft Start-Up with Internal Reference



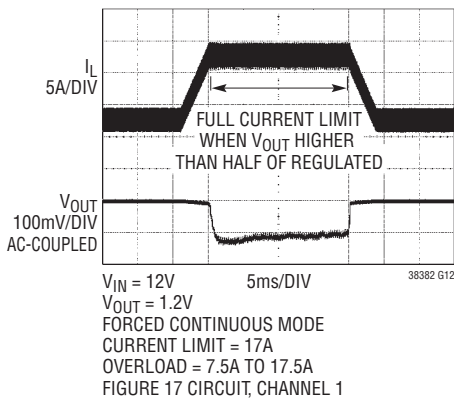
## Soft Start-Up Into Prebiased Output



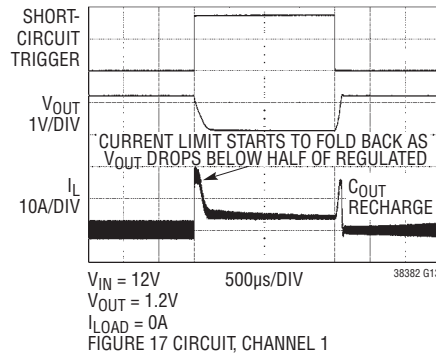
## Soft Start-Up with External Reference



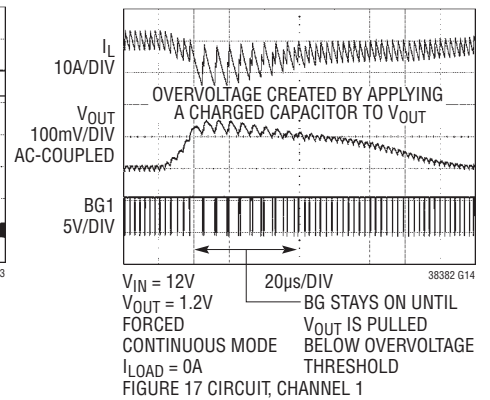
## Overcurrent Protection



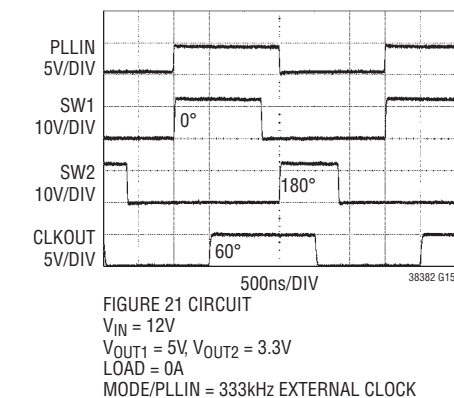
## Short-Circuit Protection



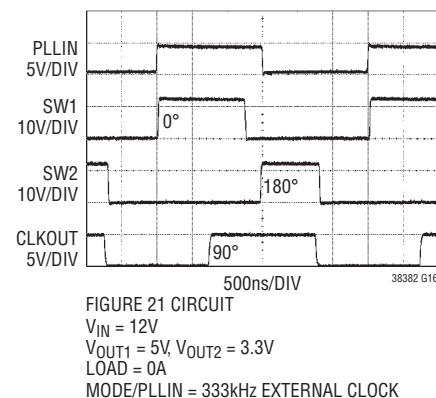
## Overvoltage Protection



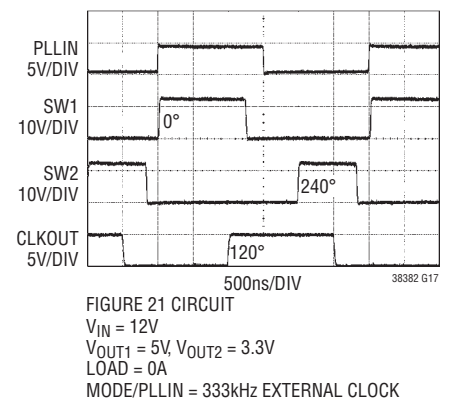
## Phase Relationship: PHASMD = Ground



## Phase Relationship: PHASMD = Float

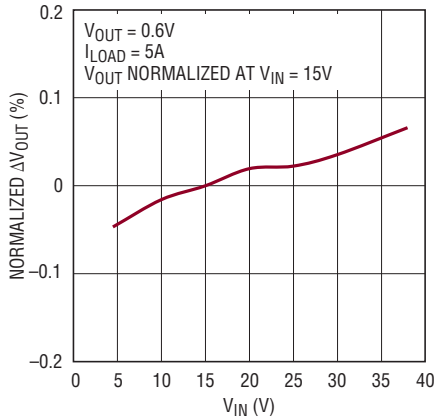


## Phase Relationship: PHASMD = INTV<sub>CC</sub>

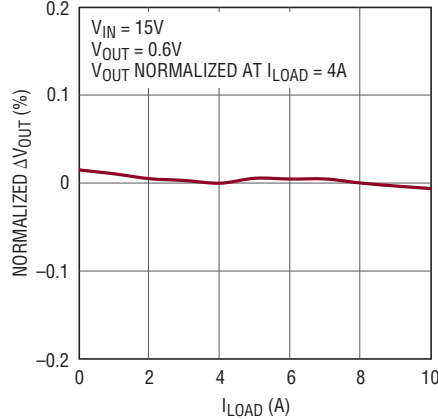


## TYPICAL PERFORMANCE CHARACTERISTICS

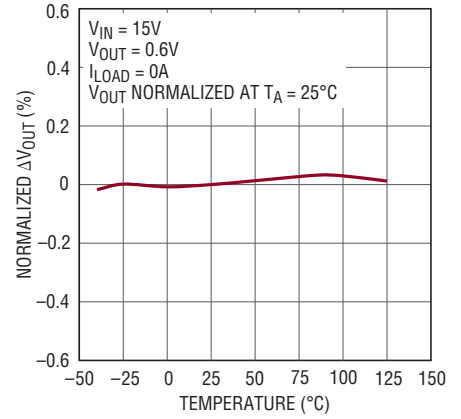
**Output Regulation vs Input Voltage**



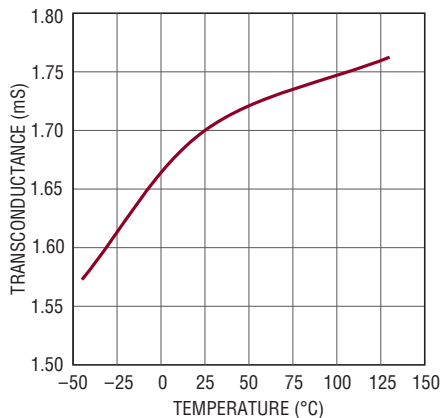
**Output Regulation vs Load Current**



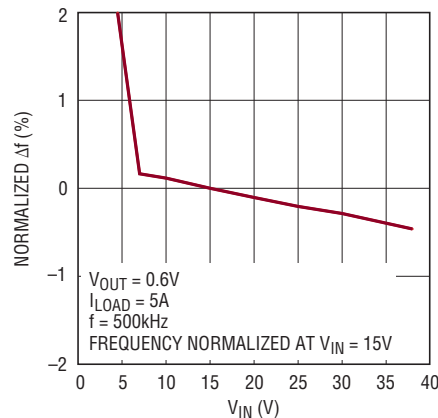
**Output Regulation vs Temperature**



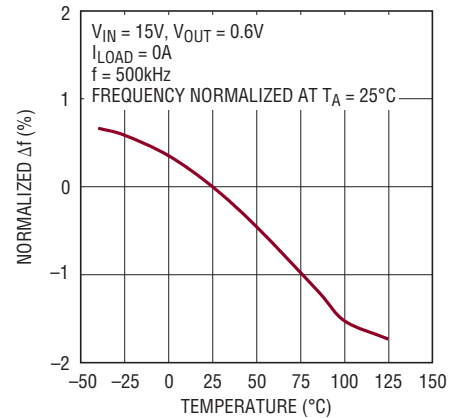
**Error Amplifier Transconductance vs Temperature**



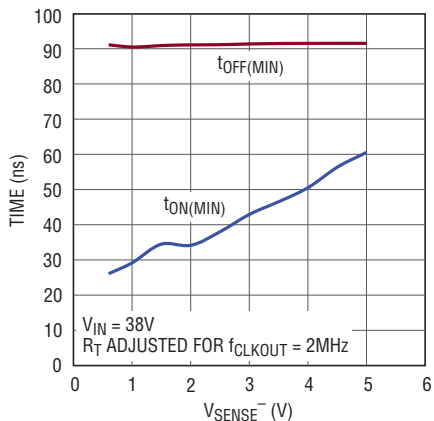
**CLKOUT/Switching Frequency vs Input Voltage**



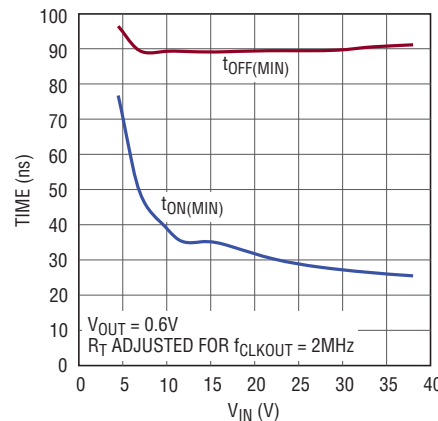
**CLKOUT/Switching Frequency vs Temperature**



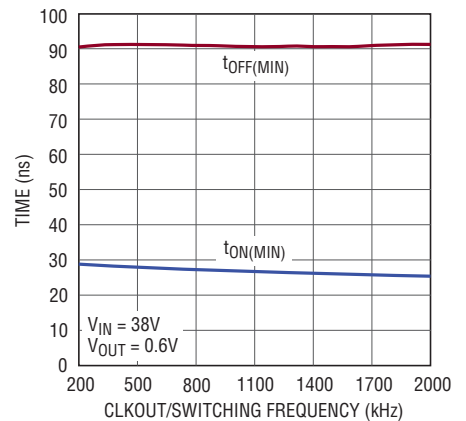
**tON(MIN) and tOFF(MIN) vs VOUT (Voltage on SENSE- Pin)**



**tON(MIN) and tOFF(MIN) vs Voltage on VIN Pin**



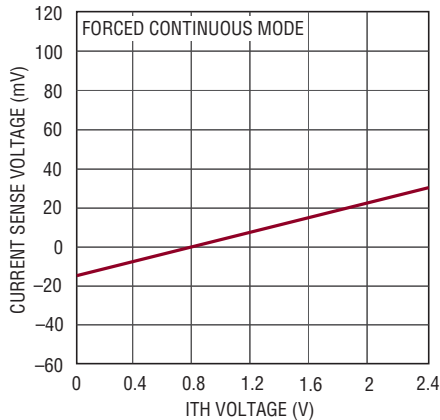
**tON(MIN) and tOFF(MIN) vs Switching Frequency**





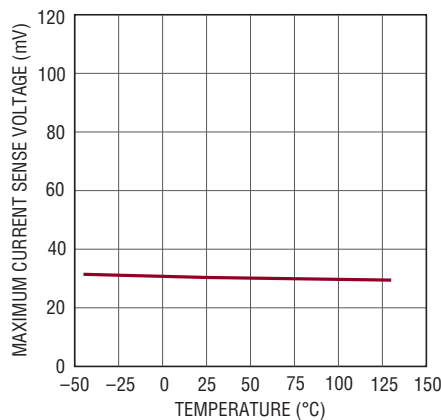
# TYPICAL PERFORMANCE CHARACTERISTICS

**Current Sense Voltage vs ITH Voltage**



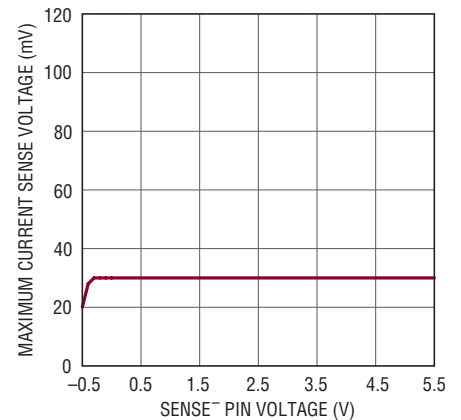
38382 G28

**Maximum Current Sense Voltage vs Temperature**



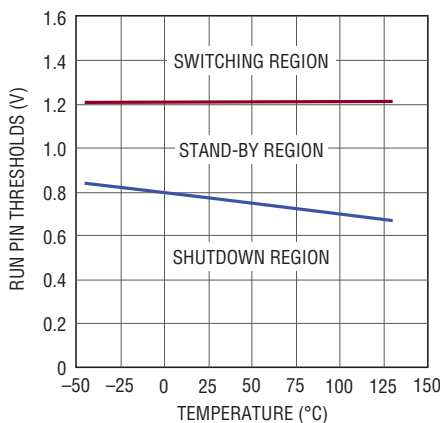
38382 G29

**Maximum Current Sense Voltage vs Voltage on SENSE<sup>-</sup> Pin**



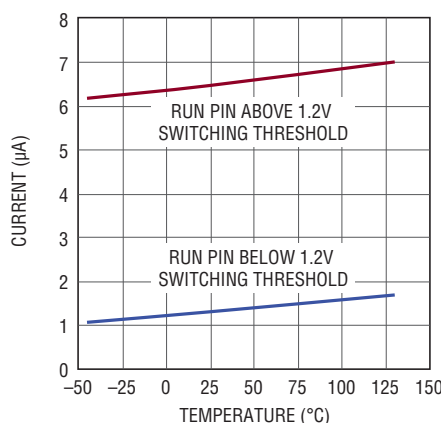
38382 G22

**RUN Pin Thresholds vs Temperature**



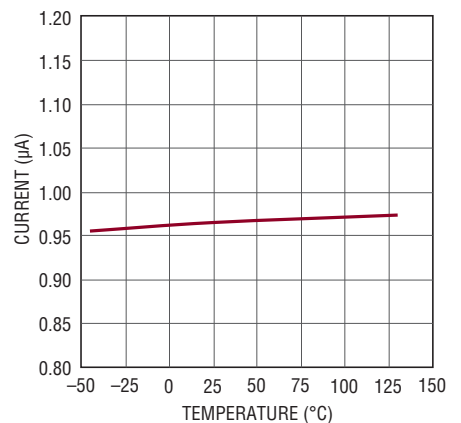
38382 G30

**RUN Pull-Up Currents vs Temperature**



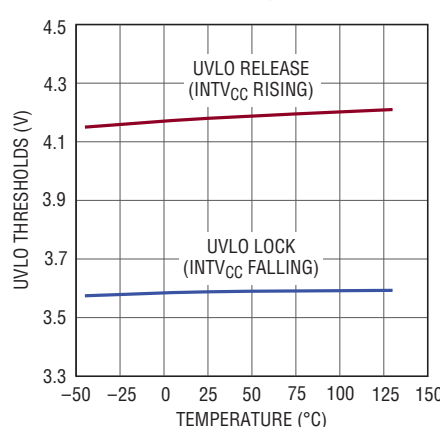
38381 G31

**TRACK/SS Pull-Up Currents vs Temperature**



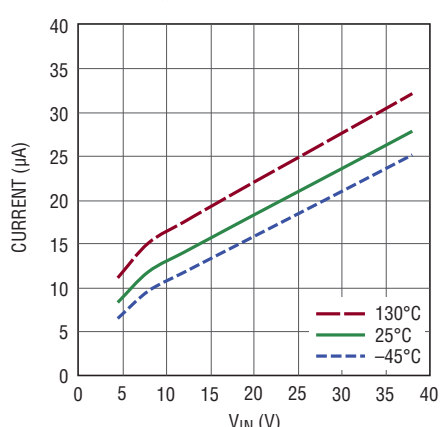
38382 G32

**INTV<sub>CC</sub> Undervoltage Lockout Thresholds vs Temperature**



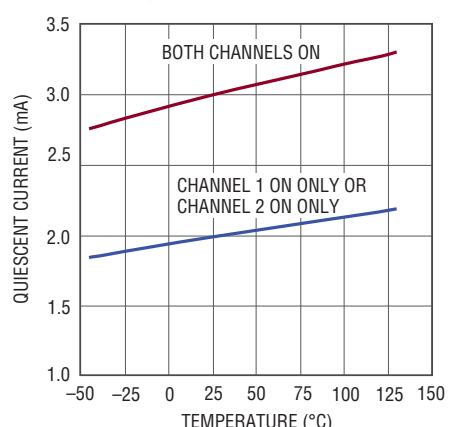
38382 G33

**Shutdown Current Into V<sub>IN</sub> Pin vs Voltage on V<sub>IN</sub> Pin**



38382 G34

**Quiescent Current Into V<sub>IN</sub> Pin vs Temperature**



38382 G35

## PIN FUNCTIONS

**$V_{DFB2}^+$  (Pin 1):** Differential Feedback Amplifier Positive (+) Input of Channel 2. As shown in the Functional Diagram, connect this pin to a 3-resistor feedback divider network, which is composed of  $R_{DFB1}$  and  $R_{DFB2}$  from this pin to the negative and positive terminals of  $V_{OUT2}$  respectively, and a third resistor from this pin to the remote ground of external reference voltage ( $V_{REF2}^-$ ). The third resistor must have a value equal to  $R_{DFB1} // R_{DFB2}$  for accurate differential regulation. With the 3-resistor feedback divider network, the LTC3838-2 will regulate the differential output ( $V_{OUT2}^+ - V_{OUT2}^-$ ) to  $(V_{REF2}^+ - V_{REF2}^-) \cdot (R_{DFB1} + R_{DFB2}) / R_{DFB1}$ .

**$EXTV_{REF2}$  (Pin 2):** External Reference Voltage for Channel 2. Connect this pin to the positive (+) terminal of external reference voltage ( $V_{REF2}^+$ ). The internal feedback voltage  $V_{FB2}$  (i.e.,  $2 \cdot V_{DFB2}^+ - V_{DFB2}^-$ ) will be regulated to the voltage on this pin, so that the differential  $V_{OUT2}$  equals  $(V_{REF2}^+ - V_{REF2}^-) \cdot (R_{DFB1} + R_{DFB2}) / R_{DFB1}$ . When this pin is less than around 100mV, the TRACK/SS2 pin will be pulled to ground to keep channel 2 from switching. Channel 2's overvoltage and undervoltage thresholds are  $\pm 7.5\%$  of this  $EXTV_{REF2}$  pin voltage. For valid PGOOD2 signal upon startup and to avoid prebiased  $V_{OUT2}$  (if any) being pulled down, apply  $EXTV_{REF2}$  before RUN2 is enabled. Normal operations are only guaranteed with an  $EXTV_{REF2}$  of 0.4V minimum and 1.5V maximum at  $INTV_{CC} \geq 4V$ , or 2.5V maximum at  $INTV_{CC} \geq 5V$ . Note its small bias current (see the Electrical Characteristics section) may cause offset if external R-C filter is connected to this pin for either limiting voltage slew rate or filtering noise.

**MODE/PLLIN (Pin 5):** Operation Mode Selection or External Clock Synchronization Input. When this pin is tied to  $INTV_{CC}$ , forced continuous mode operation is selected. Tying this pin to SGND allows discontinuous mode operation. When an external clock is applied at this pin, both channels operate in forced continuous mode and synchronize to the external clock. This pin has an internal 600k pull-down resistor to SGND.

**CLKOUT (Pin 6):** Clock Output of Internal Clock Generator. Its output level swings between  $INTV_{CC}$  and SGND. If clock input is present at the MODE/PLLIN pin, it will be synchronized to the input clock, with phase set by the PHASMD pin. If no clock is present at MODE/PLLIN, its

frequency will be set by the RT pin. To synchronize other controllers, it can be connected to their MODE/PLLIN pins.

**SGND (Pin 7):** Signal Ground. All small-signal analog and compensation components should be connected to this ground. Connect SGND to the exposed pad and PGND pin using a single PCB trace.

**RT (Pin 8):** Clock Generator Frequency Programming Pin. Connect an external resistor from RT to SGND to program the switching frequency between 200kHz and 2MHz. An external clock applied to MODE/PLLIN should be within  $\pm 30\%$  of this programmed frequency to ensure frequency lock. When the RT pin is floating, the frequency is internally set to be slightly under 200kHz.

**PHASMD (Pin 9):** Phase Selector Input. This pin determines the relative phases of channels and the CLKOUT signal. With zero phase being defined as the rising edge of TG1: Pulling this pin to SGND locks TG2 to 180°, and CLKOUT to 60°. Connecting this pin to  $INTV_{CC}$  locks TG2 to 240° and CLKOUT to 120°. Floating this pin locks TG2 to 180° and CLKOUT to 90°.

**ITH1, ITH2 (Pin 10, Pin 3):** Current Control Threshold. This pin is the output of the error amplifier and the switching regulator's compensation point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V, with 0.8V corresponding to zero sense voltage (zero inductor valley current).

**TRACK/SS1, TRACK/SS2 (Pin 11, Pin 4):** External Tracking and Soft-Start Input. Channel 1 regulates the feedback voltage  $V_{FB1} = V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$  to the smaller of 0.6V or the voltage on the TRACK/SS1 pin. Channel 2 regulates the  $V_{FB2} = 2 \cdot V_{DFB2}^+ - V_{DFB2}^-$  to the smaller of the voltage on the  $EXTV_{REF2}$  pin or the voltage on the TRACK/SS2 pin. An internal 1 $\mu$ A temperature-independent pull-up current source is connected to each TRACK/SS pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, another voltage supply connected to this pin allows the output to track the other supply during start-up. In applications that operate simultaneously at both high  $EXTV_{REF2}$  (>1.5V) and low  $V_{IN}$  (<6V) pin voltages, external pull-up (resistor or fixed current from  $INTV_{CC}$ ) may be required so that TRACK/SS2 rises well above  $EXTV_{REF2}$ .

## PIN FUNCTIONS

**V<sub>OUTSENSE1+</sub> (Pin 12):** Differential Output Sense Amplifier (+) Input of Channel 1. Connect this pin to a feedback resistor divider between the positive and negative output capacitor terminals of V<sub>OUT1</sub>, as shown in the Functional Diagram. In normal operation, the LTC3838-2 will regulate the differential output voltage V<sub>OUT1</sub> to 0.6V divided by the feedback resistor divider ratio, i.e.,  $V_{OUT1}^+ - V_{OUT2}^- = 0.6V \cdot (R_{FB1} + R_{FB2})/R_{FB1}$ .

Shorting the V<sub>OUTSENSE1+</sub> pin to INTV<sub>CC</sub> will disable channel 1's error amplifier, and internally connect ITH1 to ITH2. (As a result, TRACK/SS1 is no longer functional and PGOOD1 is always pulling low.) By doing so, this part can function as a dual phase, single V<sub>OUT</sub> step-down controller, and the two channels use a *single* channel 2's error amplifier for the ITH output and compensation.

**V<sub>OUTSENSE1-</sub> (Pin 13):** Differential Output Sense Amplifier (-) Input of Channel 1. Connect this pin to the negative terminal of the output load capacitor of V<sub>OUT1</sub>.

**SENSE1+, SENSE2+ (Pin 14, Pin 37):** Differential Current Sense Comparator (+) Inputs. The ITH pin voltage and controlled offsets between the SENSE+ and SENSE- pins set the current trip threshold. The comparator can be used for R<sub>SENSE</sub> sensing or inductor DCR sensing. For R<sub>SENSE</sub> sensing, Kelvin (4-wire) connect the SENSE+ pin to the (+) terminal of R<sub>SENSE</sub>. For DCR sensing, tie the SENSE+ pins to the connection between the DCR sense capacitor and sense resistor tied across the inductor.

**SENSE1-, SENSE2- (Pin 15, Pin 36):** Differential Current Sense Comparator (-) Input. The comparator can be used for R<sub>SENSE</sub> sensing or inductor DCR sensing. For R<sub>SENSE</sub> sensing, Kelvin (4-wire) connect the SENSE- pin to the (-) terminal of R<sub>SENSE</sub>. For DCR sensing, tie the SENSE- pin to the DCR sense capacitor tied to the inductor V<sub>OUT</sub> node connection. These pins also function as output voltage sense pins for the top MOSFET on-time adjustment. The impedance looking into these pins is different from the SENSE+ pins because there is an additional 500k internal resistor from each of the SENSE- pins to SGND.

**DTR1, DTR2 (Pin 16, Pin 35):** Detect Load-Release Transient for Overshoot Reduction. When load current suddenly drops, if voltage on this DTR pin drops below half of INTV<sub>CC</sub>, the bottom gate (BG) could turn off, allowing the inductor current to drop to zero faster, thus reducing the V<sub>OUT</sub> overshoot. (Refer to Load-Release Transient Detection in the Applications Information section for more details.) An internal 2.5μA current source pulls this pin toward INTV<sub>CC</sub>. To disable the DTR feature, simply tie the DTR pin to INTV<sub>CC</sub>.

**RUN1, RUN2 (Pin 17, Pin 34):** Run Control Inputs. An internal proportional-to-absolute-temperature (PTAT) pull-up current source (~1.2μA at 25°C) is constantly connected to this pin. Taking both RUN1 and RUN2 pins below a threshold voltage (~0.8V at 25°C) shuts down all bias of INTV<sub>CC</sub> and DRV<sub>CC</sub> and places the LTC3838-2 into micropower shutdown mode. Allowing either RUN pin to rise above this threshold would turn on the internal bias supply and the circuitry for the particular channel. When a RUN pin rises above 1.2V, its corresponding channel's TG and BG drivers are turned on and an additional 5μA temperature-independent pull-up current is connected internally to the RUN pin. Either RUN pin can sink up to 50μA, or be forced no higher than 6V.

**PGOOD1, PGOOD2 (Pin 18, Pin 33):** Power Good Indicator Outputs. This open-drain logic output is pulled to ground when the output voltage goes out of a ±7.5% window around the regulation point, after a 50μs power-bad-masking delay. Returning to the regulation point, there is a delay of around 20μs to power good, and a hysteresis of around 15mV (on the same scale as each channel's reference and internal feedback voltages V<sub>FB1,2</sub>) on both sides of the voltage window. Channel 2's ±7.5% window is based on the EXT<sub>VREF2</sub> pin voltage, and only guaranteed with a minimum EXT<sub>VREF2</sub> of 0.4V. To ensure valid PGOOD2 upon start-up, apply stable EXT<sub>VREF2</sub> before RUN2 is enabled.

**BOOST1, BOOST2 (Pin 19, Pin 32):** Boosted Floating Supplies for Top MOSFET Drivers. The (+) terminal of the bootstrap capacitor, C<sub>B</sub>, connects to this pin. The BOOST pins swing by a V<sub>IN</sub> between a diode drop below DRV<sub>CC</sub>, or (V<sub>DRVCC</sub> - V<sub>D</sub>) and (V<sub>IN</sub> + V<sub>DRVCC</sub> - V<sub>D</sub>).

## PIN FUNCTIONS

**TG1, TG2 (Pin 20, Pin 31):** Top Gate Driver Outputs. The TG pins drive the gates of the top N-channel power MOSFET with a voltage swing of  $V_{DRVCC}$  between SW and BOOST.

**SW1, SW2 (Pin 21, Pin 30):** Switch Node Connection to Inductors. Voltage swings are from a diode voltage below ground to  $V_{IN}$ . The (-) terminal of the bootstrap capacitor,  $C_B$ , connects to this node.

**BG1, BG2 (Pin 22, Pin 29):** Bottom Gate Driver Outputs. The BG pins drive the gates of the bottom N-channel power MOSFET between PGND and  $DRV_{CC}$ .

**$DRV_{CC1}$ ,  $DRV_{CC2}$  (Pin 23, Pin 28):** Supplies of Bottom Gate Drivers.  $DRV_{CC1}$  is also the output of an internal 5.3V regulator.  $DRV_{CC2}$  is also the output of the  $EXTV_{CC}$  switch. Normally the two  $DRV_{CC}$  pins are shorted together on the PCB, and decoupled to PGND with a minimum of 4.7 $\mu$ F ceramic capacitor,  $C_{DRVCC}$ .

**$V_{IN}$  (Pin 24):** Input Voltage Supply. The supply voltage can range from 4.5V to 38V. For increased noise immunity decouple this pin to SGND with an RC filter. Voltage at this pin is also used to adjust top gate on-time, therefore it is recommended to tie this pin to the main power input supply through an RC filter.

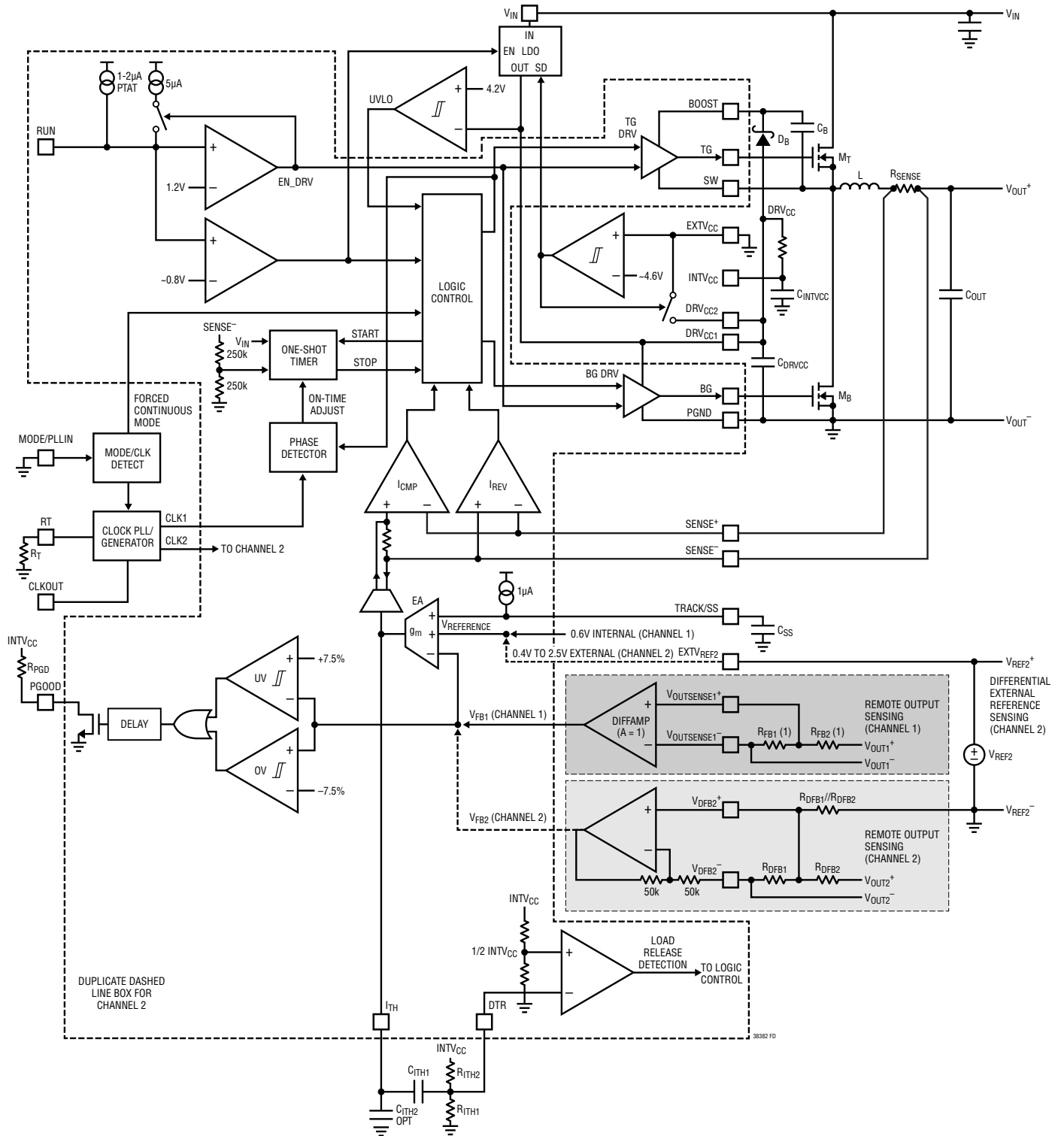
**PGND (Pin 25, Exposed Pad Pin 39):** Power Ground. Connect this pin as close as practical to the source of the bottom N-channel power MOSFET, the (-) terminal of  $C_{DRVCC}$  and the (-) terminal of  $C_{IN}$ . Connect the exposed pad and PGND pin to SGND pin using a single PCB trace under the IC. The exposed pad must be soldered to the circuit board for electrical and rated thermal performance.

**$INTV_{CC}$  (Pin 26):** Supply Input for Internal Circuitry (Not Including Gate Drivers). Normally powered from the  $DRV_{CC}$  pins through a decoupling RC filter to SGND (typically 2 $\Omega$  and 1 $\mu$ F).

**$EXTV_{CC}$  (Pin 27):** External Power Input. When  $EXTV_{CC}$  exceeds the switchover voltage (typically 4.6V), an internal switch connects this pin to  $DRV_{CC2}$  and shuts down the internal regulator so that  $INTV_{CC}$  and gate drivers draw power from  $EXTV_{CC}$ . The  $V_{IN}$  pin still needs to be powered up but draws minimum current.

**$V_{DFB2}^-$  (Pin 38):** Differential Feedback Amplifier Negative (-) Input of Channel 2. Connect this pin to the negative terminal of the output load capacitor of  $V_{OUT2}$ .

# FUNCTIONAL DIAGRAM



## OPERATION (Refer to Functional Diagram)

### Main Control Loop

The LTC3838-2 is a controlled on-time, valley current mode step-down DC/DC dual controller with two channels operating out of phase. Each channel drives both main and synchronous N-channel MOSFETs. The two channels can be either configured to two independently regulated outputs, or combined into a single output.

The top MOSFET is turned on for a time interval determined by a one-shot timer. The duration of the one-shot timer is controlled to maintain a fixed switching frequency. As the top MOSFET is turned off, the bottom MOSFET is turned on after a small delay. The delay, or dead time, is to avoid both top and bottom MOSFETs being on at the same time, causing shoot-through current from  $V_{IN}$  directly to power ground. The next switching cycle is initiated when the current comparator,  $I_{CMP}$ , senses that inductor current falls below the trip level set by voltages at the ITH and  $V_{RNG}$  pins. The bottom MOSFET is turned off immediately and the top MOSFET on again, restarting the one-shot timer and repeating the cycle. In order to avoid shoot-through current, there is also a small dead-time delay before the top MOSFET turns on. At this moment, the inductor current hits its “valley” and starts to rise again.

Inductor current is determined by sensing the voltage between  $SENSE^+$  and  $SENSE^-$ , either by using an explicit resistor connected in series with the inductor or by implicitly sensing the inductor’s DC resistive (DCR) voltage drop through an RC filter connected across the inductor. The trip level of the current comparator,  $I_{CMP}$ , is proportional to the voltage at the ITH pin, with a zero-current threshold corresponding to an ITH voltage of around 0.8V.

The error amplifier (EA) adjusts this ITH voltage by comparing the feedback signal ( $V_{FB}$ ) derived from the difference amplifier (DIFFAMP) to an internal or external reference voltage. The ITH voltage controls the output by adjusting the current in the inductor. Output voltage is regulated so that the feedback voltage is equal to the reference. If the

load current increases/decreases, it causes a momentary drop/rise in the differential feedback voltage relative to the reference. The EA then moves ITH voltage, or inductor valley current setpoint, higher/lower until the average inductor current again matches the load current, so that the output voltage comes back to the regulated voltage.

The LTC3838-2 features a detect transient (DTR) pin to detect “load-release”, or a transient where the load current suddenly drops, by monitoring the first derivative of the ITH voltage. When detected, the bottom gate (BG) is turned off and inductor current flows through the body diode in the bottom MOSFET, allowing the SW node voltage to drop below PGND by the body diode’s forward-conduction voltage. This creates a more negative differential voltage ( $V_{SW} - V_{OUT}$ ) across the inductor, allowing the inductor current to drop faster to zero, thus creating less overshoot on  $V_{OUT}$ . See Load-Release Transient Detection in Applications Information for details.

### Differential Output Sensing and External Reference

Both channels of this dual controller have differential output voltage sensing. The output voltage is resistively divided externally to create a feedback voltage for the controller. As shown in the Functional Diagram, channel 1 uses an external 2-resistor voltage divider, and an internal unity-gain difference amplifier (DIFFAMP) that converts the differential feedback signal to a single-ended internal feedback voltage  $V_{FB1} = V_{OUTSENSE1^+} - V_{OUTSENSE1^-}$  with respect to SGND. With the external resistor divider,  $V_{OUT1^+} - V_{OUT1^-} = V_{FB1} \cdot (R_{FB1} + R_{FB2})/R_{FB1}$ . Channel 2 has a unique feedback amplifier that produces  $V_{FB2} = 2 \cdot V_{DFB2^+} - V_{DFB2^-}$ . Its external feedback network requires a third resistor tied to the external reference remote ground ( $V_{REF2^-}$ ). The third resistor must have a value equal to the parallel value of the two voltage divider resistors  $R_{DFB1}$  and  $R_{DFB2}$  so that  $V_{OUT2^+} - V_{OUT2^-} = (V_{FB2} - V_{REF2^-}) \cdot (R_{DFB1} + R_{DFB2})/R_{DFB1}$ .

## OPERATION (Refer to Functional Diagram)

Both channels adjust outputs through system feedback loops so that the internally-generated single-ended feedback voltages ( $V_{FB1,2}$  in the Functional Diagram) equal either the internal 0.6V reference (for channel 1) or the  $EXTV_{REF2} = V_{REF2}^+$  (for channel 2) when in regulation. Therefore, the differential  $V_{OUT1}$  is regulated to  $0.6V \cdot (R_{FB1} + R_{FB2})/R_{FB1}$ , and the differential  $V_{OUT2}$  is regulated to  $(V_{REF2}^+ - V_{REF2}^-) \cdot (R_{DFB1} + R_{DFB2})/R_{DFB1}$ . Such schemes eliminate any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. Channel 1 allows remote output ground to deviate as much as  $\pm 500mV$ , and channel 2 allows as much as  $\pm 200mV$ , with respect to local ground (SGND).

Channel 2 senses the external reference voltage  $V_{REF2}$  differentially. The positive terminal of the external reference  $V_{REF2}^+$  is fed into the  $EXTV_{REF2}$  pin. The remote ground of the external reference  $V_{REF2}^-$  is connected to the third resistor in the external output voltage feedback network. The IC itself does not see the  $V_{REF2}^-$  directly, but to keep the regulation accuracy, the common mode voltage of the external reference is practically limited by the voltages on  $EXTV_{REF2}$  pin as specified in the Electrical Characteristic table, and the  $V_{DFB2}^+$  pin ( $\geq -0.2V$ ), etc.

### DRV<sub>CC</sub>/EXTV<sub>CC</sub>/INTV<sub>CC</sub> Power

DRV<sub>CC1,2</sub> are the power for the bottom MOSFET drivers. Normally the two DRV<sub>CC</sub> pins are shorted together on the PCB, and decoupled to PGND with a minimum 4.7 $\mu F$  ceramic capacitor, C<sub>DRVCC</sub>. The top MOSFET drivers are biased from the floating bootstrap capacitors (C<sub>B1,2</sub>) which are recharged during each cycle through an external Schottky diode when the top MOSFET turns off and the SW pin swings down.

The DRV<sub>CC</sub> can be powered two ways: an internal low-dropout (LDO) linear voltage regulator that is powered from V<sub>IN</sub> and can output 5.3V to DRV<sub>CC1</sub>. Alternatively, an internal EXTV<sub>CC</sub> switch (with on-resistance of around 2 $\Omega$ ) can short the EXTV<sub>CC</sub> pin to DRV<sub>CC2</sub>.

If the EXTV<sub>CC</sub> pin is below the EXTV<sub>CC</sub> switchover voltage (typically 4.6V with 200mV hysteresis, see the Electrical Characteristics Table), then the internal 5.3V LDO is enabled. If the EXTV<sub>CC</sub> pin is tied to an external voltage source greater than this EXTV<sub>CC</sub> switchover voltage, then the LDO is shut down and the internal EXTV<sub>CC</sub> switch shorts the EXTV<sub>CC</sub> pin to the DRV<sub>CC2</sub> pin. In this case, DRV<sub>CC</sub> and INTV<sub>CC</sub> draw power from the external voltage source which helps to increase overall efficiency and decrease internal self heating from power dissipated in the LDO. If the output voltage of the converter itself is above the upper switchover voltage limit (4.8V), it can provide power for EXTV<sub>CC</sub>. The V<sub>IN</sub> pin still needs to be powered up but now draws minimum current.

Power for most internal control circuitry other than gate drivers is derived from the INTV<sub>CC</sub> pin. INTV<sub>CC</sub> can be powered from the combined DRV<sub>CC</sub> pins through an external RC filter to SGND to filter out noises due to switching.

### Shutdown and Start-Up

Each of the RUN1 and RUN2 pins has an internal proportional-to-absolute-temperature (PTAT) current source (around 1.2 $\mu A$  at 25°C) to pull up the pins. Taking both RUN1 and RUN2 pins below a certain threshold voltage (around 0.8V at 25°C) shuts down all bias of INTV<sub>CC</sub> and DRV<sub>CC</sub> and places the LTC3838-2 into micropower shutdown mode with a minimum I<sub>Q</sub> at the V<sub>IN</sub> pin. The LTC3838-2's DRV<sub>CC</sub> (through the internal 5.3V LDO regulator or EXTV<sub>CC</sub>) and the corresponding channel's internal circuitry off INTV<sub>CC</sub> will be biased up when either or both RUN pins are pulled up above the 0.8V threshold, either by the internal pull-up current or driven directly by an external voltage source such as a logic gate output.

A channel of the LTC3838-2 will not start switching until the RUN pin of the respective channel is pulled up to 1.2V. When a RUN pin rises above 1.2V, the corresponding channel's TG and BG drivers are enabled, and TRACK/SS released. An additional 5 $\mu A$  temperature-independent

## OPERATION (Refer to Functional Diagram)

pull-up current is connected internally to the channel's respective RUN pin. To turn off TG, BG and the additional 5 $\mu$ A pull-up current, RUN needs to be pulled down below 1.2V by about 100mV. These built-in current and voltage hystereses prevent false jittery turn-on and turn-off due to noise. These features on the RUN pins allow input undervoltage lockout (UVLO) to be set up using external voltage dividers from  $V_{IN}$ .

The start-up of a channel's output voltage ( $V_{OUT}$ ) is controlled by the voltage on its TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.6V internal reference (channel 1) or the external reference voltage on  $EXTV_{REF2}$  pin (channel 2), the feedback voltage ( $V_{FB}$ ) is regulated to the TRACK/SS voltage instead of the reference. The TRACK/SS pin can be used to program the output voltage soft-start ramp-up time by connecting an external capacitor from a TRACK/SS pin to signal ground. An internal temperature-independent 1 $\mu$ A pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises from ground to the reference voltage, the switching starts, and  $V_{OUT}$  ramps up smoothly to its final regulated value. TRACK/SS will keep rising until the pull-up current stops at well above 3V when the  $V_{IN}$  pin is greater than 6V.

Note, when the  $V_{IN}$  pin voltage is close to its low end, the pull-up current may stop at a lower voltage. In applications that require both low  $V_{IN}$  pin voltage (< 6V, down to 4.5V) and high  $EXTV_{REF2}$  (>1.5V, up to 2.5V) at the same time, an external pull-up (current or resistor from  $INTV_{CC}$ ) could be added to the TRACK/SS2 pin so that TRACK/SS2 settles well above  $EXTV_{REF2}$ . This prevents  $V_{FB2}$  from being regulated to an insufficient TRACK/SS2 voltage instead of the desired  $EXTV_{REF2}$  after soft-start.

Upon enabling the RUN pin, if  $V_{OUT}$  is prebiased at a level above zero, the top gate (TG) will remain off and  $V_{OUT}$  stays prebiased. Once TRACK/SS rises above the prebiased feedback level, and TG starts switching,  $V_{OUT}$  will be regulated according to TRACK/SS or the reference, whichever is lower.

Alternatively, the TRACK/SS pin can be used to track an external supply like in a master slave configuration. Typically, this requires connecting a resistor divider from the master supply to the TRACK/SS pin (see the Applications Information section).

TRACK/SS is pulled low internally when the corresponding channel's RUN pin is pulled below the 1.2V threshold (hysteresis applies), or when  $INTV_{CC}$  or either of the  $DRV_{CC1,2}$  pins drop below their respective undervoltage lockout (UVLO) thresholds. TRACK/SS2 is also pulled low internally when voltage on the  $EXTV_{REF2}$  pin is less than 0.1V, which prevents channel 2 from starting to switch until a valid  $EXTV_{REF2}$  is present and TRACK/SS2 is released.

When  $EXTV_{REF2}$  rises from below 0.1V, a fast voltage step up can be applied on  $EXTV_{REF2}$ , as TRACK/SS2 allows  $V_{OUT2}$  to soft-start. However, once the soft-start ends and TRACK/SS2 rises above  $EXTV_{REF2}$ , it is recommended that dynamic voltage change on  $EXTV_{REF2}$  be rate-limited. If  $EXTV_{REF2}$  jumps up, inductor current may reach its full limit. If  $EXTV_{REF2}$  steps down, overvoltage (OV) may be triggered, which turns on BG2 and discharges  $V_{OUT2}$  without any limit on inductor current. If any external R-C filter is connected in series to control the slew rate of  $EXTV_{REF2}$  voltage, be careful about the offset caused by the pin's bias current (see the Electrical Characteristics section) through the resistor.



## OPERATION (Refer to Functional Diagram)

### Light Load Current Operation

If the MODE/PLLIN pin is tied to  $INTV_{CC}$  or an external clock is applied to MODE/PLLIN, the LTC3838-2 will be forced to operate in continuous mode. With load current less than one-half of the full load peak-to-peak ripple, the inductor current valley can drop to zero or become negative. This allows constant-frequency operation but at the cost of low efficiency at light loads.

If the MODE/PLLIN pin is left open or connected to signal ground, the channel will transition into discontinuous mode operation, where a current reversal comparator ( $I_{REV}$ ) shuts off the bottom MOSFET ( $M_B$ ) as the inductor current approaches zero, thus preventing negative inductor current and improving light-load efficiency. In this mode, both switches can remain off for extended periods of time. As the output capacitor discharges by load current and the output voltage droops lower, EA will eventually move the ITH voltage above the zero current level (0.8V) to initiate another switching cycle.

### Power Good and Fault Protection

Each PGOOD pin is connected to an internal open-drain N-channel MOSFET. An external resistor or current source can be used to pull this pin up to 6V (e.g.,  $V_{OUT1,2}$  or  $DRV_{CC}$ ). Overvoltage or undervoltage comparators (OV, UV) turn on the MOSFET and pull the PGOOD pin low when the feedback voltage is outside the  $\pm 7.5\%$  window of the channel's reference voltage. The PGOOD pin is also pulled low when the channel's RUN pin is below the 1.2V threshold (hysteresis applies), or in undervoltage lockout (UVLO).

When the feedback voltage is within the  $\pm 7.5\%$  window, the open-drain NMOS is turned off and the pin is pulled up by the external source. The PGOOD pin will indicate power good immediately after the feedback is within the window. But when a feedback voltage of a channel goes out of the window, there is an internal 50 $\mu$ s delay before its PGOOD is pulled low.

In an overvoltage (OV) condition,  $M_T$  is turned off and  $M_B$  is turned on immediately without delay and held on until the overvoltage condition clears. Upon enabling the RUN1 pin, if  $V_{OUT1}$  is prebiased so that the  $V_{FB1}$  is at more than 7.5% above the regulated voltage, OV stays triggered and bottom gate (BG) forced to pull  $V_{OUT1}$  low until  $V_{FB1}$  is  $\sim 15$ mV (or  $\sim 2.5\%$  of 0.6V internal reference) hysteresis below the OV threshold. For channel 2, the OV threshold is set at 7.5% above the voltage on  $EXTV_{REF2}$  pin, but the  $\sim 15$ mV hysteresis remains the same regardless of the OV threshold. To ensure that OV and UV thresholds are not determined by extremely low reference voltages, apply a stable  $EXTV_{REF2}$  before enabling RUN2, which also prevents BG from being turned on, and any prebiased  $V_{OUT2}$  from being pulled low upon start-up.

Foldback current limiting is provided if the output is below one-half of the regulated voltage, such as being shorted to ground. As the feedback approaches 0V, the internal clamp voltage for the ITH pin drops from 2.4V to around 1.3V, which reduces the inductor valley current level to about 30% of its maximum value. Foldback current limiting is disabled at start-up.

## OPERATION (Refer to Functional Diagram)

### Frequency Selection and External Clock Synchronization

An internal oscillator (clock generator) provides phase-interleaved internal clock signals for individual channels to lock up to. The switching frequency and phase of each switching channel is independently controlled by adjusting the top MOSFET turn-on time (on-time) through the one-shot timer. This is achieved by sensing the phase relationship between a top MOSFET turn-on signal and its internal reference clock through a phase detector, and the time interval of the one-shot timer is adjusted on a cycle-by-cycle basis, so that the rising edge of the top MOSFET turn-on is always trying to synchronize to the internal reference clock signal for the respective channel.

The frequency of the internal oscillator can be programmed from 200kHz to 2MHz by connecting a resistor,  $R_T$ , from the RT pin to signal ground (SGND). The RT pin is regulated to 1.2V internally.

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE/PLLIN pin can be used to synchronize the internal clock signals through a clock phase-locked loop (Clock PLL). The LTC3838-2 operates in forced continuous mode of operation when it is synchronized to the external clock. The external clock frequency has to be within  $\pm 30\%$  of the internal oscillator frequency for successful synchronization. The clock input levels should be no less than 2V for “high” and no greater than 0.5V for “low”. The MODE/PLLIN pin has an internal 600k pull-down resistor.

### Multichip Operations

The PHASMD pin determines the relative phases between the internal reference clock signals for the two channels as well as the CLKOUT signal, as shown in Table 2. The phases tabulated are relative to zero degree ( $0^\circ$ ) being defined as the rising edge of the internal reference clock signal of channel 1. The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding either a single high current output, or separate outputs.

The system can be configured for up to 12-phase operation with a multichip solution. Typical configurations are shown in Table 3 to interleave the phases of the channels.

Table 2

PHASMD	SGND	FLOAT	INTV <sub>CC</sub>
Channel 1	$0^\circ$	$0^\circ$	$0^\circ$
Channel 2	$180^\circ$	$180^\circ$	$240^\circ$
CLKOUT	$60^\circ$	$90^\circ$	$120^\circ$

Table 3

NUMBER OF PHASES	NUMBER OF LTC3838-2	PIN CONNECTIONS [PIN NAME (CHIP NUMBER)]
2	1	PHASMD(1) = FLOAT or SGND
3	2	PHASMD(1) = INTV <sub>CC</sub> MODE/PLLIN(2) = CLKOUT(1)
4	2	PHASMD(1) = FLOAT PHASMD(2) = FLOAT or SGND MODE/PLLIN(2) = CLKOUT(1)
6	3	PHASMD(1) = SGND PHASMD(2) = SGND MODE/PLLIN(2) = CLKOUT(1) PHASMD(3) = FLOAT or SGND MODE/PLLIN(3) = CLKOUT(2)
12	6	PHASMD(1) = SGND PHASMD(2) = SGND MODE/PLLIN(2) = CLKOUT(1) PHASMD(3) = FLOAT MODE/PLLIN(3) = CLKOUT(2) PHASMD(4) = SGND MODE/PLLIN(4) = CLKOUT(3) PHASMD(5) = SGND MODE/PLLIN(5) = CLKOUT(4) PHASMD(6) = FLOAT or SGND MODE/PLLIN(6) = CLKOUT(5)

## OPERATION (Refer to Functional Diagram)

### Single-Output External-Reference PolyPhase Configurations

To use LTC3838-2 for a 2-phase single output external-referenced step-down controller: Tie the  $V_{OUTSENSE1}^+$  pin to  $INTV_{CC}$ , which will disable channel 1's error amplifier and internally connect ITH2 to ITH1. Tie the compensation R-C components to the ITH2 pin. The ITH1 pin can be either left open or shorted to ITH2 externally. The TRACK/SS1 and PGOOD1 pins become defunct and can be left open. Note that the RUN1 and RUN2, as well as DTR1 and DTR2 pins still function for the two channels individually, therefore should be shorted externally for single-output applications. Set PHASMD to SGND or FLOAT so that the two channels are 180° out-of-phase. Efficiency losses may be substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A 2-phase implementation can reduce the input path power loss by up to 75%.

To make a single-output converter of three or more phases, additional LTC3838-2 ICs can be used. The first chip should be tied the same way as the 2-phase above. If only one more channel of an additional LTC3838-2 is needed, use channel 2 for the additional phase:

- Tie the ITH2 pin to the ITH2 pin of the first chip
- Tie the RUN2 pin to the RUN pins of the first chip
- Tie the  $V_{DFB2}^+$  pin to the  $V_{DFB2}^+$  pin of the first chip
- Tie the  $V_{DFB2}^-$  pin to the  $V_{DFB2}^-$  pin of the first chip
- Tie the TRACK/SS2 pin to the TRACK/SS2 pin of the first chip

If both channels are needed, the additional LTC3838-2 chip should be tied the same way as the first LTC3838-2 chip to disable channel 1's EA:

- Tie the  $V_{OUTSENSE1}^+$  pin to the chip's own  $INTV_{CC}$
- Tie the ITH2 pin to the ITH2 pin of the first chip
- Tie the RUN pins to the RUN pins of the first chip
- Tie the  $V_{DFB2}^+$  pin to the  $V_{DFB2}^+$  pin of the first chip
- Tie the  $V_{DFB2}^-$  pin to the  $V_{DFB2}^-$  pin of the first chip
- Tie the TRACK/SS2 pin to the TRACK/SS2 pin of the first chip

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Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirement, and begins with the selection of inductors and current sense method (either sense resistors  $R_{SENSE}$  or inductor DCR sensing). Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

### Output Voltage Programming

As shown in Figure 1, external resistor dividers are used from the regulated outputs to their respective ground references to program the output voltages. On Channel 1, the resistive divider is tapped by the  $V_{OUTSENSE1+}$  pin, and the ground reference is remotely sensed by the  $V_{OUTSENSE1-}$  pin; this voltage is sensed differentially. By regulating the tapped (differential) feedback voltages to the internal reference 0.6V, the resulting output voltages are:

$$V_{OUT1+} - V_{OUT1-} = 0.6V \cdot (1 + R_{FB2}/R_{FB1})$$

The minimum (differential)  $V_{OUT1}$  is limited to the internal reference 0.6V, when  $R_{FB1}$  is removed (effectively  $R_{FB1} = \infty$ ), and/or  $R_{FB2}$  is shorted (effectively  $R_{FB2} = 0$ ).

On channel 2, add a 3rd resistor with value equal to the two voltage-divider resistors in parallel (or simply add two parallel resistors equal to each of the two voltage divider resistors). Note the external reference  $V_{REF2}$  is sensed differentially through the  $EXTV_{REF2}$  pin and the 3rd resistor:

$$V_{OUT2+} - V_{OUT2-} = (V_{REF2+} - V_{REF2-}) \cdot (1 + R_{DFB2}/R_{DFB1})$$

The minimum (differential)  $V_{OUT2}$  is limited to the (differential) external reference  $V_{REF2}$ . To program  $V_{OUT2} =$

$V_{REF2}$ ,  $R_{DFB1}$  can be removed and the  $R_{DFB3} = R_{DFB1} // R_{DFB2}$  uses the same value as  $R_{DFB2}$ , as effectively  $R_{DFB1} = \infty$ .

The maximum output voltages on both channels can be set up to 5.5V, as limited by the maximum voltage that can be applied on the SENSE pins.

$V_{OUTSENSE1+}$  and  $V_{DFB2+}$  are high impedance pins with no input bias current other than leakage in the nA range. The  $V_{OUTSENSE1-}$  pin has about 25 $\mu$ A of current flowing out of the pin. The  $V_{DFB2-}$  pin has a current of around  $(V_{DFB2+} - V_{DFB2-})/50k$  flowing out of the pin.

Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 2 illustrates the potential variations in the power and ground lines due to parasitic elements. The variations may be exacerbated in multi-application systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage. The LTC3838-2's differential output sensing can correct for up to  $\pm 500$ mV of common-mode deviation in the output's power and ground lines on channel 1, and  $\pm 200$ mV on channel 2.

The LTC3838-2's differential output sensing schemes are distinct from conventional schemes where the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistor divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

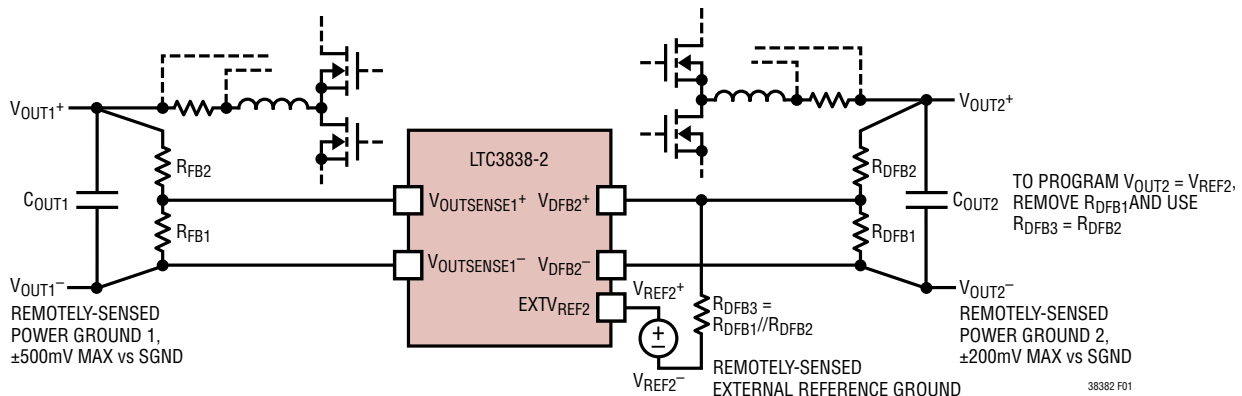
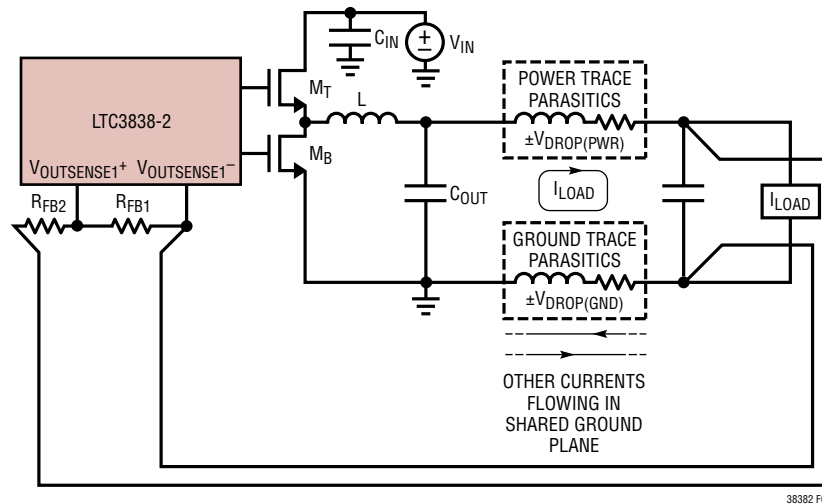


Figure 1. Setting Output Voltage

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**Figure 2. Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane**

The LTC3838-2 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output ranges. Channel 1's difference amplifier (DIFFAMP) has a bandwidth of around 8MHz, and channel 2's feedback amplifier has a bandwidth of around 4MHz, both high enough so as not to affect main loop compensation and transient behavior.

To avoid noise coupling into the feedback voltages, the resistor dividers should be placed close to the  $V_{OUTSENSE1+}$  and  $V_{OUTSENSE1-}$ , or  $V_{DFB2+}$  and  $V_{DFB2-}$  pins. Remote output and ground traces should be routed together as a differential pair to the remote output. For best accuracy, these traces to the remote output and ground should be connected as close as possible to the desired regulation point.

### Switching Frequency Programming

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The switching frequency of the LTC3838-2 can be programmed from 200kHz to 2MHz by connecting a resistor from the RT pin to signal ground. The value of this resistor can be chosen according to the following formula:

$$R_T [\text{k}\Omega] = \frac{41550}{f [\text{kHz}]} - 2.2$$

The overall controller system, including the clock PLL and switching channels, has a synchronization range of no less than  $\pm 30\%$  around this programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this  $\pm 30\%$  range of the RT programmed frequency. It is advisable that the RT programmed frequency be equal the external clock for maximum synchronization margin. Refer to the "Phase and Frequency Synchronization" section for more details.

### Inductor Value Calculation

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

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The inductor value has a direct effect on ripple current. The inductor ripple current  $\Delta I_L$  decreases with higher inductance or frequency and increases with higher  $V_{IN}$ :

$$\Delta I_L = \left( \frac{V_{OUT}}{f \cdot L} \right) \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Accepting larger values of  $\Delta I_L$  allows the use of low inductances, but results in higher output voltage ripple, higher ESR losses in the output capacitor, and greater core losses. A reasonable starting point for setting ripple current is  $\Delta I_L = 0.4 \cdot I_{MAX}$ . The maximum  $\Delta I_L$  occurs at the maximum input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left( \frac{V_{OUT}}{f \cdot \Delta I_{L(MAX)}} \right) \left( 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. The two basic types are iron powder and ferrite. The iron powder types have a soft saturation curve which means they do not saturate hard like ferrites do. However, iron powder type inductors have higher core losses. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation.

Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite core material saturates *hard*, which means that inductance collapses abruptly when the peak design current is exceeded. This results an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse and Würth. In designs of higher switching

frequency, especially in the MHz range, core loss can be very significant. Be sure to check with the manufacturer on the frequency characteristics of the core material.

### Current Sense Pins

Inductor current is sensed through voltage between SENSE<sup>+</sup> and SENSE<sup>-</sup> pins, the inputs of the internal current comparators. Care must be taken not to float these pins during normal operation. The SENSE<sup>+</sup> pins are quasi-high impedance inputs. There is no bias current into a SENSE<sup>+</sup> pin when its corresponding channel's SENSE<sup>-</sup> pin ramps up from below 1.1V and stays below 1.4V. But there is a small (~1 $\mu$ A) current flowing into a SENSE<sup>+</sup> pin when its corresponding SENSE<sup>-</sup> pin ramps down from 1.4V and stays above 1.1V. Such currents also exist on SENSE<sup>-</sup> pins. But in addition, each SENSE<sup>-</sup> pin has an internal 500k resistor to SGND. The resulted current ( $V_{OUT}/500k$ ) will dominate the total current flowing into the SENSE<sup>-</sup> pins. SENSE<sup>+</sup> and SENSE<sup>-</sup> pin currents have to be taken into account when designing either R<sub>SENSE</sub> or DCR inductor current sensing.

### Current Limit Programming

The current sense comparators' maximum trip voltage between SENSE<sup>+</sup> and SENSE<sup>-</sup> (or  $V_{SENSE(MAX)}$ ), when ITH is clamped at its maximum 2.4V, is 30mV typical.

The valley current mode control loop does not allow the inductor current valley to exceed  $V_{SENSE(MAX)}$ . But note that the peak inductor current is higher than this valley current limit by the amount of the inductor ripple current. Also when calculating the peak current limit, allow sufficient margin to account for the tolerance of  $V_{SENSE(MAX)}$  as given in the Electrical Characteristics table, and variations in values of external components (such as the inductor), as well as the range of the input voltage (since ripple current is a function of input voltage).

Either low value series current sensing resistor (R<sub>SENSE</sub>) or the DC resistance of the inductor (DCR) can be used to monitor the inductor current. The choice between the two current sensing schemes is largely a design trade-off among accuracy, power consumption, and cost. The R<sub>SENSE</sub> method offers more precise control of the current

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limit but the resistor will dissipate loss. The DCR method saves the cost of the sense resistors and may offer better efficiency, especially in high current applications, but tolerance and the variation over temperature in the DCR value usually requires larger design margins.

### $R_{\text{SENSE}}$ Inductor Current Sensing

The LTC3838-2 can be configured to sense the inductor currents through either current sensing resistors ( $R_{\text{SENSE}}$ ) or inductor DC resistance (DCR). The current sensing resistors provide the most accurate current limits for the controller.

A typical  $R_{\text{SENSE}}$  inductor current sensing scheme is shown in Figure 3a. The filter components ( $R_F$ ,  $C_F$ ) need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair close together and Kelvin (4-wire) connected underneath the sense resistor, as shown in Figure 3b. Sensing current elsewhere can effectively add parasitic inductance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable.

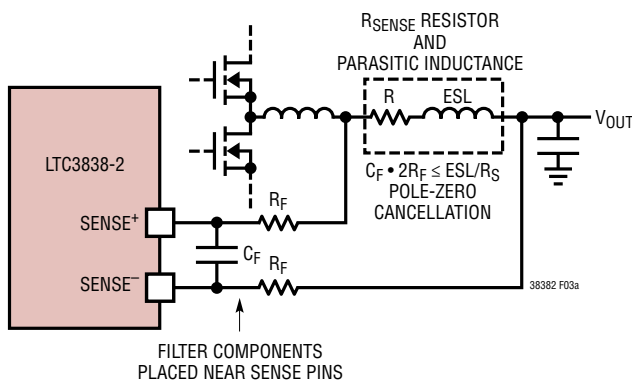


Figure 3a.  $R_{\text{SENSE}}$  Current Sensing

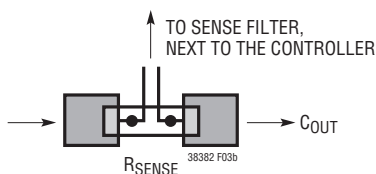


Figure 3b. Sense Lines Placement with Sense Resistor

$R_{\text{SENSE}}$  is chosen based on the required maximum output current. Given the maximum current,  $I_{\text{OUT(MAX)}}$ , maximum sense voltage,  $V_{\text{SENSE(MAX)}}$ , and maximum inductor ripple current  $\Delta I_{\text{L(MAX)}}$ , the value of  $R_{\text{SENSE}}$  can be chosen as:

$$R_{\text{SENSE}} = \frac{V_{\text{SENSE(MAX)}}}{I_{\text{OUT(MAX)}} - \frac{\Delta I_{\text{L(MAX)}}}{2}}$$

Conversely, given  $R_{\text{SENSE}}$  and  $I_{\text{OUT(MAX)}}$ ,  $V_{\text{SENSE(MAX)}}$  can be determined from the above equation. To ensure the maximum output current, sufficient margin should be built in the calculations to account for variations of the ICs under different operating conditions and tolerances of external components.

Because of possible PCB noise in the current sensing loop, the current sensing voltage ripple  $\Delta V_{\text{SENSE}} = \Delta I_{\text{L}} \cdot R_{\text{SENSE}}$  also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, 10mV of  $\Delta V_{\text{SENSE}}$  is recommended as a conservative number to start with, either for  $R_{\text{SENSE}}$  or Inductor DCR sensing applications.

For today's highest current density solutions the value of the sense resistor can be less than 1m $\Omega$  and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 2MHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance becomes more relevant. A small RC filter placed near the IC has been traditionally used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10 $\Omega$  resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 4a illustrates the voltage waveform across a 2m $\Omega$  sense resistor with a 2010 footprint for a 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential

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measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \cdot \frac{t_{ON} \cdot t_{OFF}}{t_{ON} + t_{OFF}}$$

where  $V_{ESL(STEP)}$  is the voltage step caused by the ESL and shown in Figure 4a, and  $t_{ON}$  and  $t_{OFF}$  are top MOSFET on-time and off-time respectively. If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor ( $L/R$ ), the resulting waveform looks resistive again, as shown in Figure 4b. For applications using low  $V_{SENSE(MAX)}$ , check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on  $V_{RSENSE}$ .

Note that the SENSE1<sup>-</sup> and SENSE2<sup>-</sup> pins are also used for sensing the output voltage for the adjustment of top gate on time,  $t_{ON}$ . For this purpose, there is an additional internal 500k resistor from each SENSE<sup>-</sup> pin to SGND,

therefore there is an impedance mismatch with their corresponding SENSE<sup>+</sup> pins. The voltage drop across the  $R_F$  causes an offset in sense voltage. For example, with  $R_F = 100\Omega$ , at  $V_{OUT} = V_{SENSE^-} = 5V$ , the sense-voltage offset  $V_{SENSE(OFFSET)} = V_{SENSE^-} \cdot R_F/500k = 1mV$ . Such small offset may seem harmless for current limit, but could be significant for current reversal detection ( $I_{REV}$ ), causing excess negative inductor current at discontinuous mode. Also, at  $V_{SENSE(MAX)} = 30mV$ , a mere 1mV offset will cause a significant shift of zero-current ITH voltage by  $(2.4V - 0.8V) \cdot 1mV/30mV = 53mV$ . Too much shift may not allow the output voltage to return to its regulated value after the output is shorted due to ITH foldback. Therefore, when a larger filter resistor  $R_F$  value is used, it is recommended to use an *external* 500k resistor from each SENSE<sup>+</sup> pin to SGND, to balance the *internal* 500k resistor at its corresponding SENSE<sup>-</sup> pin.

The previous discussion generally applies to high density/high current applications where  $I_{OUT(MAX)} > 10A$  and low inductor values are used. For applications where  $I_{OUT(MAX)} < 10A$ , set  $R_F$  to  $10\Omega$  and  $C_F$  to 1000pF. This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin (4-wire) connected to the sense resistor.

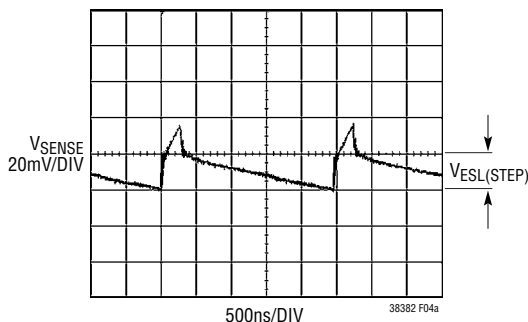


Figure 4a. Voltage Waveform Measured Directly Across the Sense Resistor

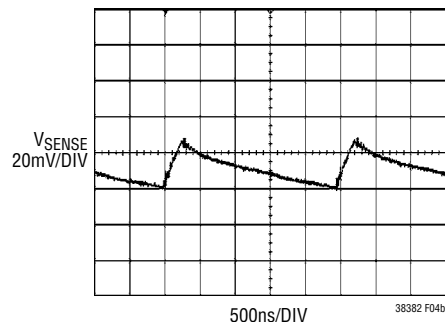


Figure 4b. Voltage Waveform Measured After the Sense Resistor Filter.  $C_F = 1000pF$ ,  $R_F = 100\Omega$



## APPLICATIONS INFORMATION

### DCR Inductor Current Sensing

For applications requiring higher efficiency at high load currents, the LTC3838-2 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 5. The DCR of the inductor represents the small amount of DC winding resistance, which can be less than 1mΩ for today's low value, high current inductors.

In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

The inductor DCR is sensed by connecting an RC filter across the inductor. This filter typically consists of one or two resistors (R1 and R2) and one capacitor (C1) as shown in Figure 5. If the external  $(R1||R2) \cdot C1$  time constant is chosen to be exactly equal to the  $L/DCR$  time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by  $R2/(R1 + R2)$ . Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. C1 is usually selected in the range of 0.01μF to 0.47μF. This forces  $R1||R2$  to around 2k to 4k, reducing error that might have been caused by the SENSE pins' input bias currents.

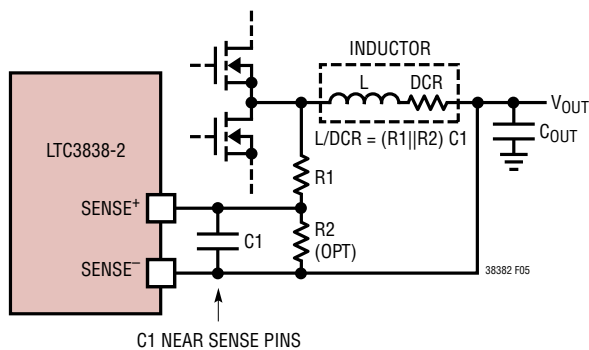


Figure 5. DCR Current Sensing

Resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. Capacitor C1 should be placed close to the IC pins.

The first step in designing DCR current sensing is to determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 25°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for inductor temperature  $T_L$  is 100°C. The DCR of the inductor can also be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

From the DCR value,  $V_{SENSE(MAX)}$  is easily calculated as:

$$V_{SENSE(MAX)} = DCR_{MAX(25^{\circ}C)} \cdot \left[ 1 + 0.4\% (T_{L(MAX)} - 25^{\circ}C) \right] \cdot \left( I_{OUT(MAX)} - \frac{\Delta I_L}{2} \right)$$

If  $V_{SENSE(MAX)}$  is within the maximum sense voltage (30mV typical) of the LTC3838-2, then the RC filter only needs R1. If  $V_{SENSE(MAX)}$  is higher, then R2 may be used to scale down the maximum sense voltage so that it falls within range.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1) = \frac{(V_{IN(MAX)} - V_{OUT}) \cdot V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or  $R_{SENSE}$  sensing. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

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To maintain a good signal-to-noise ratio for the current sense signal, start with a  $\Delta V_{\text{SENSE}}$  of 10mV. For a DCR sensing application, the actual ripple voltage will be determined by:

$$\Delta V_{\text{SENSE}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{R1 \cdot C1} \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}} \cdot f}$$

### Power MOSFET Selection

Two external N-channel power MOSFETs must be selected for each channel of the LTC3838-2 controller: one for the top (main) switch and one for the bottom (synchronous) switch. The gate drive levels are set by the  $DRV_{\text{CC}}$  voltage. This voltage is typically 5.3V. Pay close attention to the  $BV_{\text{DSS}}$  specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance,  $R_{\text{DS(ON)}}$ , Miller capacitance,  $C_{\text{MILLER}}$ , input voltage and maximum output current. Miller capacitance,  $C_{\text{MILLER}}$ , can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet.  $C_{\text{MILLER}}$  is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat (or the parameter  $Q_{\text{GD}}$  if specified on a manufacturer's data sheet), divided by the specified  $V_{\text{DS}}$  test voltage:

$$C_{\text{MILLER}} \cong \frac{Q_{\text{GD}}}{V_{\text{DS(TEST)}}$$

When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$D_{\text{TOP}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

$$D_{\text{BOT}} = 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{\text{TOP}} = D_{\text{TOP}} \cdot I_{\text{OUT(MAX)}}^2 \cdot R_{\text{DS(ON)(MAX)}} (1 + \delta) + V_{\text{IN}}^2 \cdot \left( \frac{I_{\text{OUT(MAX)}}}{2} \right) \cdot C_{\text{MILLER}} \left[ \frac{R_{\text{TG(UP)}}}{V_{\text{DRVCC}} - V_{\text{MILLER}}} + \frac{R_{\text{TG(DOWN)}}}{V_{\text{MILLER}}} \right] \cdot f$$

$$P_{\text{BOT}} = D_{\text{BOT}} \cdot I_{\text{OUT(MAX)}}^2 \cdot R_{\text{DS(ON)(MAX)}} \cdot (1 + \delta)$$

where  $\delta$  is the temperature dependency of  $R_{\text{DS(ON)}}$ ,  $R_{\text{TG(UP)}}$  is the TG pull-up resistance, and  $R_{\text{TG(DOWN)}}$  is the TG pull-down resistance.  $V_{\text{MILLER}}$  is the Miller effect  $V_{\text{GS}}$  voltage and is taken graphically from the MOSFET's data sheet.

Both MOSFETs have  $I^2R$  losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For  $V_{\text{IN}} < 20\text{V}$ , the high current efficiency generally improves with larger MOSFETs, while for  $V_{\text{IN}} > 20\text{V}$ , the transition losses rapidly increase to the point that the use of a higher  $R_{\text{DS(ON)}}$  device with lower  $C_{\text{MILLER}}$  actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

The term  $(1 + \delta)$  is generally given for a MOSFET in the form of a normalized  $R_{\text{DS(ON)}}$  vs temperature curve in the power MOSFET data sheet. For low voltage MOSFETs, 0.5% per degree ( $^{\circ}\text{C}$ ) can be used to estimate  $\delta$  as an approximation of percentage change of  $R_{\text{DS(ON)}}$ :

$$\delta = 0.005/^{\circ}\text{C} \cdot (T_{\text{J}} - T_{\text{A}})$$

where  $T_{\text{J}}$  is estimated junction temperature of the MOSFET and  $T_{\text{A}}$  is ambient temperature.

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### $C_{IN}$ Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The worst-case RMS current occurs by assuming a single-phase application. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT(MAX)}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3838-2, additional ceramic capacitors should also be used in parallel for  $C_{IN}$  close to the IC and power switches to bypass the high frequency switching noises. Typically multiple X5R or X7R ceramic capacitors are put in parallel with either conductive-polymer or aluminum-electrolytic types of bulk capacitors. Because of its low ESR, the ceramic capacitors will take most of the RMS ripple current. Vendors do not consistently specify the ripple current rating for ceramics, but ceramics *could* also fail due to excessive ripple current. Always consult the manufacturer if there is any question.

Figure 6 represents a simplified circuit model for calculating the ripple currents in each of these capacitors. The input inductance ( $L_{IN}$ ) between the input source and the input of the converter will affect the ripple current through the capacitors. A lower input inductance will result in less ripple current through the input capacitors since more ripple current will now be flowing out of the input source.

For simulations with this model, look at the ripple current during steady-state for the case where one phase is fully loaded and the other was not loaded. This will in *general*

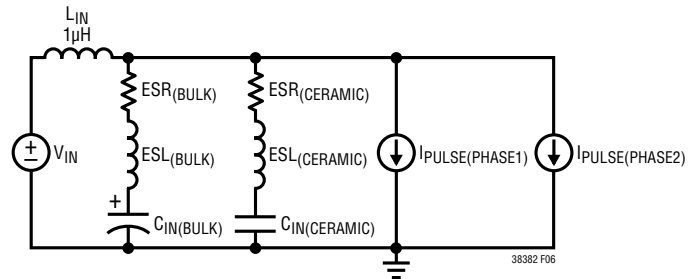


Figure 6. Circuit Model for Input Capacitor Ripple Current Simulation

be the worst case for ripple current since the ripple current from one phase will not be cancelled by ripple current from the other phase.

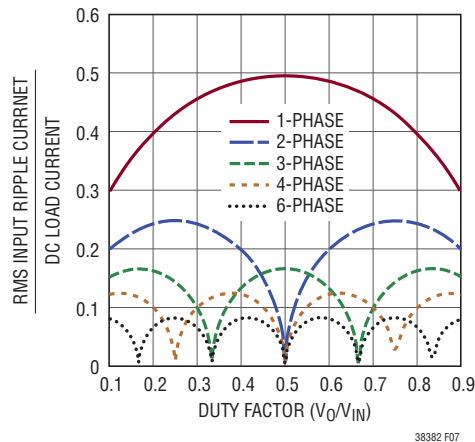
Note that the bulk capacitor also has to be chosen for RMS rating with ample margin beyond its RMS current per simulation with the circuit model provided. For a lower  $V_{IN}$  range, a conductive-polymer type (such as Sanyo OS-CON) can be used for its higher ripple current rating and lower ESR. For a wide  $V_{IN}$  range that also require higher voltage rating, aluminum-electrolytic capacitors are more attractive since it can provide a larger capacitance for more damping. An aluminum-electrolytic capacitor with a ripple current rating that is high enough to handle all of the ripple current by itself will be very large. But when in parallel with ceramics, an aluminum-electrolytic capacitor will take a much smaller portion of the RMS ripple current due to its high ESR. However, it is crucial that the ripple current through the aluminum-electrolytic capacitor should not exceed its rating since this will produce significant heat, which will cause the electrolyte inside the capacitor to dry over time and its capacitance to go down and ESR to go up.

The benefit of PolyPhase operation is reduced RMS currents and therefore less power loss on the input capacitors. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a PolyPhase system. The details of a close form equation can be found in Application Note 77 High Efficiency, High Density, PolyPhase Converters for High Current Applications. Figure 7 shows the input capacitor RMS ripple currents normalized against the DC output currents with respect to the duty

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cycle. This graph can be used to estimate the maximum RMS capacitor current for a multiple-phase application, assuming the channels are identical and their phases are fully interleaved.

Figure 7 shows that the use of more phases will reduce the ripple current through the input capacitors due to ripple current cancellation. However, since LTC3838-2 is only truly phase-interleaved at steady state, transient RMS currents could be higher than the curves for the designated number of phase. Therefore, it is advisable to choose capacitors by taking account the specific load situations of the applications. It is always the safest to choose input capacitors' RMS current rating closer to the worst case of a single-phase application discussed above, calculated by assuming the loss that would have resulted if controller channels switched on at the same time.



**Figure 7. Normalized RMS Input Ripple Current**

However, it is generally not needed to size the input capacitor for such worst-case conditions where on-times of the phases coincide all the time. During a load step event, the overlap of on-time will only occur for a small percentage of time, especially when duty cycles are low. A transient event where the switch nodes align for several cycles at a time should not damage the capacitor. In most applications, sizing the input capacitors for 100% steady-state load should be adequate. For example, a microprocessor load may cause frequent overlap of the on-times, which makes the ripple current higher, but the load current may

rarely be at 100% of  $I_{OUT(MAX)}$ . Using the worst-case load current should already have margin built in for transient conditions.

The  $V_{IN}$  sources of the top MOSFETs should be placed close to each other and share common  $C_{IN}(s)$ . Separating the sources and  $C_{IN}$  may produce undesirable voltage and current resonances at  $V_{IN}$ .

A small ( $0.1\mu F$  to  $1\mu F$ ) bypass capacitor between the IC's  $V_{IN}$  pin and ground, placed close to the IC, is suggested. A  $2.2\Omega$  to  $10\Omega$  resistor placed between  $C_{IN}$  and the  $V_{IN}$  pin is also recommended as it provides further isolation from switching noise of the two channels.

### $C_{OUT}$ Selection

The selection of output capacitance  $C_{OUT}$  is primarily determined by the effective series resistance, ESR, to minimize voltage ripple. The output voltage ripple  $\Delta V_{OUT}$ , in continuous mode is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left( R_{ESR} + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

where  $f$  is operating frequency, and  $\Delta I_L$  is ripple current in the inductor. The output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage. Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds that required from ripple current.

In multiphase single-output applications, it is advisable to consider ripple requirements at specific load conditions. At steady state, the LTC3838-2's individual phases are interleaved, and their ripples cancel each other at the output, so ripple on  $C_{OUT}$  is reduced. During transient, when the phases are not fully interleaved, the ripple cancellation may not be as effective. While the worst-case  $\Delta I_L$  is the sum of the  $\Delta I_L$ s of individual phases aligned during a fast transient, such ripple tends to counteract the effect of load transient itself and lasts for only a short time. For example, during sudden load current increase, the phases align to ramp up the total inductor current to quickly pull the  $V_{OUT}$  up from the droop.

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The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability.

Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller.

For high switching frequencies, reducing output ripple and better EMI filtering may require small value capacitors that have low ESL (and correspondingly higher self-resonant frequencies) to be placed in parallel with larger value capacitors that have higher ESL. This will ensure good noise and EMI filtering in the entire frequency spectrum of interest. Even though ceramic capacitors generally have good high frequency performance, small ceramic capacitors may still have to be parallel connected with large ones to optimize performance.

High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance. Remember also to place high frequency decoupling capacitors as close as possible to the power pins of the load.

### Top MOSFET Driver Supply ( $C_B$ , $D_B$ )

An external bootstrap capacitor,  $C_B$ , connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode  $D_B$  from  $DRV_{CC}$  when the switch node is low. When the top MOSFET turns on, the switch node rises to  $V_{IN}$  and the BOOST pin rises to approximately  $V_{IN} + INTV_{CC}$ . The boost capacitor needs to store approximately 100 times the gate charge required by the top MOSFET. In most applications a 0.1 $\mu$ F to 0.47 $\mu$ F, X5R or X7R dielectric capacitor is adequate. It is recommended that the BOOST capacitor be no larger than 10% of the  $DRV_{CC}$  capacitor,  $C_{DRV_{CC}}$ , to ensure that the  $C_{DRV_{CC}}$  can supply the upper MOSFET gate charge and BOOST capacitor under all operating conditions. Variable frequency in response to load steps offers superior transient performance but requires higher instantaneous gate drive. Gate charge demands are greatest in high frequency low duty factor applications under high load steps and at start-up.

### $DRV_{CC}$ Regulator and $EXTV_{CC}$ Power

The LTC3838-2 features a PMOS low dropout (LDO) linear regulator that supplies power to  $DRV_{CC}$  from the  $V_{IN}$  supply. The LDO regulates its output at the  $DRV_{CC1}$  pin to 5.3V. The LDO can supply a maximum current of 100mA and must be bypassed to ground with a minimum of 4.7 $\mu$ F ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to minimize interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3838-2 to be exceeded, especially if the LDO is active and provides  $DRV_{CC}$ . Power dissipation for the IC in this case is highest and is approximately equal to  $V_{IN} \cdot I_{DRV_{CC}}$ . The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equation given in Note 2 of the Electrical Characteristics. For example, when using the LDO, LTC3838-2's  $DRV_{CC}$  current is limited to less than 42mA from a 38V supply at  $T_A = 70^\circ\text{C}$ :

$$T_J = 70^\circ\text{C} + (42\text{mA})(38\text{V})(34^\circ\text{C}/\text{W}) = 125^\circ\text{C}$$

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To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode at maximum  $V_{IN}$ .

When the voltage applied to the  $EXTV_{CC}$  pin rises above the switchover voltage (typically 4.6V), the  $V_{IN}$  LDO is turned off and the  $EXTV_{CC}$  is connected to  $DRV_{CC2}$  pin with an internal switch. This switch remains on as long as the voltage applied to  $EXTV_{CC}$  remains above the hysteresis (around 200mV) below the switchover voltage. Using  $EXTV_{CC}$  allows the MOSFET driver and control power to be derived from the LTC3838-2's switching regulator output  $V_{OUT}$  during normal operation and from the LDO when the output is out of regulation (e.g., start up, short circuit). If more current is required through the  $EXTV_{CC}$  than is specified, an external Schottky diode can be added between the  $EXTV_{CC}$  and  $DRV_{CC}$  pins. Do not apply more than 6V to the  $EXTV_{CC}$  pin and make sure that  $EXTV_{CC}$  is less than  $V_{IN}$ .

Significant efficiency and thermal gains can be realized by powering  $DRV_{CC}$  from the switching converter output, since the  $V_{IN}$  current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the  $EXTV_{CC}$  pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70^\circ\text{C} + (42\text{mA})(5\text{V})(34^\circ\text{C/W}) = 77^\circ\text{C}$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive  $DRV_{CC}$  power from the converter output.

The following list summarizes the four possible connections for  $EXTV_{CC}$ :

1.  $EXTV_{CC}$  left open (or grounded). This will cause  $INTV_{CC}$  to be powered from the internal 5.3V LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2.  $EXTV_{CC}$  connected directly to switching converter output  $V_{OUT}$  is higher than the switchover voltage's higher limit (4.8V). This provides the highest efficiency.

3.  $EXTV_{CC}$  connected to an external supply. If a 4.8V or greater external supply is available, it may be used to power  $EXTV_{CC}$  providing that the external supply is sufficient for MOSFET gate drive requirements.
4.  $EXTV_{CC}$  connected to an output-derived boost network. For 3.3V and other low voltage converters, efficiency gains can still be realized by connecting  $EXTV_{CC}$  to an output-derived voltage that has been boosted to greater than 4.8V.

For applications where the main input power never exceeds 5.3V, tie the  $DRV_{CC1}$  and  $DRV_{CC2}$  pins to the  $V_{IN}$  input through a small resistor, (such as 1Ω to 2Ω) as shown in Figure 8 to minimize the voltage drop caused by the gate charge current. This will override the LDO and will prevent  $DRV_{CC}$  from dropping too low due to the dropout voltage. Make sure the  $DRV_{CC}$  voltage exceeds the  $R_{DS(ON)}$  test voltage for the external MOSFET which is typically at 4.5V for logic-level devices.

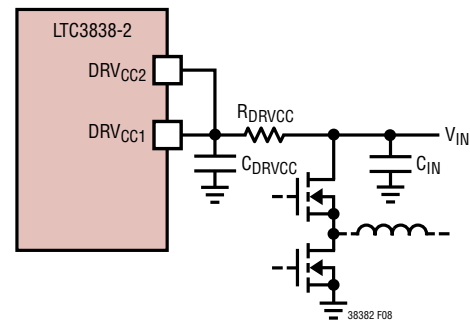


Figure 8. Setup for  $V_{IN} \leq 5.3\text{V}$

### Input Undervoltage Lockout (UVLO)

The LTC3838-2 has two functions that help protect the controller in case of input undervoltage conditions. An internal UVLO comparator constantly monitors the  $INTV_{CC}$  and  $DRV_{CC}$  voltages to ensure that adequate voltages are present. The comparator enables internal UVLO signal, which locks out the switching action of both channels, until the  $INTV_{CC}$  and  $DRV_{CC1,2}$  pins are all above their respective UVLO thresholds. The rising threshold (to release UVLO)

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of the  $INTV_{CC}$  is typically 4.2V, with 0.5V falling hysteresis (to re-enable UVLO). The UVLO thresholds for  $DRV_{CC1,2}$  are lower than that of  $INTV_{CC}$  but higher than typical threshold voltages of power MOSFETs, to prevent them from turning on without sufficient gate drive voltages.

Generally for  $V_{IN} > 6V$ , a UVLO can be set through monitoring the  $V_{IN}$  supply by using external voltage dividers at the RUN pins from  $V_{IN}$  to SGND. To design the voltage divider, note that both RUN pins have two levels of threshold voltages. The precision gate-drive-enable threshold voltage of 1.2V can be used to set a  $V_{IN}$  to turn on a channel's switching. If resistor dividers are used on both RUN pins, when  $V_{IN}$  is low enough and both RUN pins are pulled below the ~0.8V threshold, the part will shut down all bias of  $INTV_{CC}$  and  $DRV_{CC}$  and be put in micropower shutdown mode.

The RUN pins' bias currents depend on the RUN voltages. The bias current changes should be taken into account when designing the external voltage divider UVLO circuit. An internal proportional-to-absolute-temperature (PTAT) pull-up current source (~1.2 $\mu$ A at 25°C) is constantly connected to this pin. When a RUN pin rises above 1.2V, the corresponding channel's TG and BG drives are turned on and an *additional* 5 $\mu$ A temperature-independent pull-up current is connected internally to the RUN pin. Pulling the RUN pin to fall below 1.2V by more than an 80mV hysteresis turns off TG and BG of the corresponding channel, and the additional 5 $\mu$ A pull-up current is disconnected.

As voltage on a RUN pin increases, typically beyond 3V, its bias current will start to reverse direction and flow into the RUN pin. Keep in mind that *neither* of the RUN pins can sink more than 50 $\mu$ A; Even if a RUN pin may slightly exceed 6V when sinking 50 $\mu$ A, a RUN pin should *never* be forced to higher than 6V by a low impedance voltage source to prevent faulty conditions.

### Soft-Start and Tracking

The LTC3838-2 has the ability to either soft-start by itself with a capacitor or track the output of another channel or an external supply. Note that the soft-start and tracking features are achieved not by limiting the maximum output current of the controller, but by controlling the output ramp voltage according to the ramp rate on the TRACK/SS pin.

When a channel is configured to soft-start by itself, a capacitor should be connected to its TRACK/SS pin. TRACK/SS is pulled low until the RUN pin voltage exceeds 1.2V and UVLO is cleared (also for channel 2, a valid external reference voltage greater than 0.1V is present at the  $EXTV_{REF2}$  pin). After the pull-down of TRACK/SS is released, an internal current of 1 $\mu$ A charges the soft-start capacitor,  $C_{SS}$ , connected to the TRACK/SS pin. Current-limit foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to the reference  $V_{REF}$  (internal 0.6V for channel 1, or  $EXTV_{REF2}$  pin voltage for channel 2) on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SS}(\text{SEC}) = V_{REF}(\text{V}) \cdot \frac{C_{SS}(\mu\text{F})}{1(\mu\text{A})}$$

Care should be taken for channel 2 to assure that TRACK/SS2 settles well above the  $EXTV_{REF2}$  voltage after soft-start is complete under all operating conditions. Typically TRACK/SS will be pulled up by the internal current source to well above 3V when the  $V_{IN}$  pin is greater than 6V. However, when the  $V_{IN}$  pin voltage is close to its low end, the internal pull-up current may stop at a voltage less than 3V.

An external pull-up circuit to TRACK/SS2 may be required in applications that operate with low  $V_{IN}$  pin voltages and high  $EXTV_{REF2}$  voltages simultaneously, especially when both the  $V_{IN}$  pin is less than 6V (down to 4.5V) and  $EXTV_{REF2}$  is greater than 1.5V (up to 2.5V). The external pull-up circuit to the TRACK/SS2 pin can be a fixed current source, or simply a resistor from  $INTV_{CC}$ . Note that the soft-start time will change according to the external pull-up used. The external pull-up is to prevent  $V_{FB2}$  from being regulated to a low TRACK/SS2 voltage instead of the intended  $EXTV_{REF2}$ .

When one particular channel is configured to track an external supply, a voltage divider can be used from the external supply to the TRACK/SS pin to scale the ramp rate appropriately. Two common implementations are coincidental tracking and ratiometric tracking. For coincidental tracking, make the divider ratio from the external supply the same as the divider ratio for the differential feedback voltage. Ratiometric tracking could be achieved by using a different ratio than the differential feedback.

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Note that the 1 $\mu$ A soft-start capacitor charging current is still flowing, producing a small offset error. To minimize this error, select the tracking resistive divider values to be small enough to make this offset error negligible.

The LTC3838-2 allows the user to program how its two channels' outputs track each other ramping up or down. Since channel 2 uses  $EXTV_{REF2}$  as reference, by tying  $EXTV_{REF2}$  to  $V_{OUT1}$ , either directly or through a voltage divider of a certain ratio,  $V_{OUT2}$  can be set to track  $V_{OUT1}$ . Note the  $EXTV_{REF2}$  pin has a small bias current (see Electrical Characteristics). If any series external resistor is connected to this pin, make sure the offset caused by the bias current through its resistance is within the tolerance of  $V_{OUT2}$  regulation. Place a 100k resistor from the  $EXTV_{REF2}$  pin to ground in case this pin is disconnected from the external reference. Do not let this pin float.

In addition, TRACK/SS pins can be utilized for either channel to track each other. In the following discussions,  $V_{OUT1}$  refers to the LTC3838-2's output 1 as a master channel and  $V_{OUT2}$

refers to the LTC3838-2's output 2 as a slave channel. In practice though, either channel can be used as the master.

By selecting different resistors, the LTC3838-2 can achieve different modes of tracking including the two in Figure 9. To implement the coincident tracking, connect an additional resistive divider to  $V_{OUT1}$  and connect its midpoint to the TRACK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 9b. In this tracking mode,  $V_{OUT1}$  must be set higher than  $V_{OUT2}$ . To implement the ratiometric tracking as shown in Figure 9, the additional divider should be of the same ratio as the master channel's feedback divider.

Under the ratiometric mode, when the master channel's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric, or use the additional divider with a ratio of somewhere between coincident and ratiometric tracking modes.

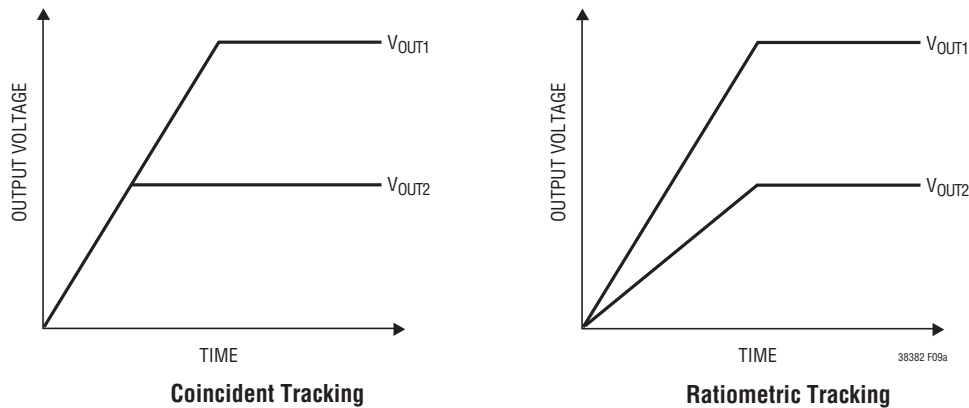


Figure 9a. Two Different Modes of Output Tracking

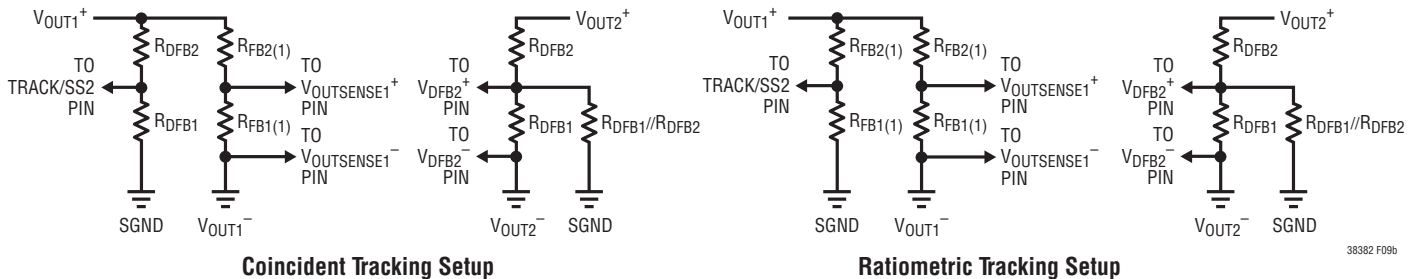


Figure 9b. Setup for Coincident and Ratiometric Tracking



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### Phase and Frequency Synchronization

For applications that require better control of EMI and switching noise or have special synchronization needs, the LTC3838-2 can synchronize the turn-on of the top MOSFET to an external clock signal applied to the MODE/PLLIN pin. The applied clock signal needs to be within  $\pm 30\%$  of the RT programmed frequency to ensure proper frequency and phase lock. The clock signal levels should generally comply to  $V_{PLLIN(H)} > 2V$  and  $V_{PLLIN(L)} < 0.5V$ . The MODE/PLLIN pin has an internal 600k pull-down resistor to ensure discontinuous current mode operation if the pin is left open.

The LTC3838-2 uses the voltages on  $V_{IN}$  and  $V_{OUT}$  as well as  $R_T$  to adjust the top gate on-time in order to maintain phase and frequency lock for wide ranges of  $V_{IN}$ ,  $V_{OUT}$  and  $R_T$ -programmed switching frequency  $f$ :

$$t_{ON} \approx \frac{V_{OUT}}{V_{IN} \cdot f}$$

As the on-time is a function of the switching regulator's output voltage, this output is measured by the SENSE<sup>-</sup> pin to set the required on-time. The SENSE<sup>-</sup> pin is tied to the regulator's local output point to the IC for most applications, as the remotely regulated output point could be significantly different from the local output point due to line losses, and local output versus local ground is typically the  $V_{OUT}$  required for the calculation of  $t_{ON}$ .

However, there could be circumstances where this  $V_{OUT}$  programmed on-time differs significantly different from the on-time required in order to maintain frequency and phase lock. For example, lower efficiencies in the switching regulator can cause the required on-time to be substantially higher than the internally set on-time (see Efficiency Considerations). If a regulated  $V_{OUT}$  is relatively low, proportionally there could be significant error caused by the difference between the local ground and remote ground, due to other currents flowing through the shared ground plane.

If necessary, the  $R_T$  resistor value, voltage on the  $V_{IN}$  pin, or even the common mode voltage of the SENSE pins may be programmed externally to correct for such systematic errors. The goal is to set the on-time programmed by  $V_{IN}$ ,  $V_{OUT}$  and  $R_T$  close to the steady-state on-time so that the system will have sufficient range to correct for component and operating condition variations, or to synchronize to the external clock. Note that there is an internal 500k resistor on each SENSE<sup>-</sup> pin to SGND, but not on the SENSE<sup>+</sup> pin.

During dynamic transient conditions either in the line voltage or load current (e.g., load step or release), the top switch will turn on more or less frequently in response to achieve faster transient response. This is the benefit of the LTC3838-2's controlled on-time, valley current mode architecture. However, this process may understandably lose phase and even frequency lock momentarily. For relatively slow changes, phase and frequency lock can

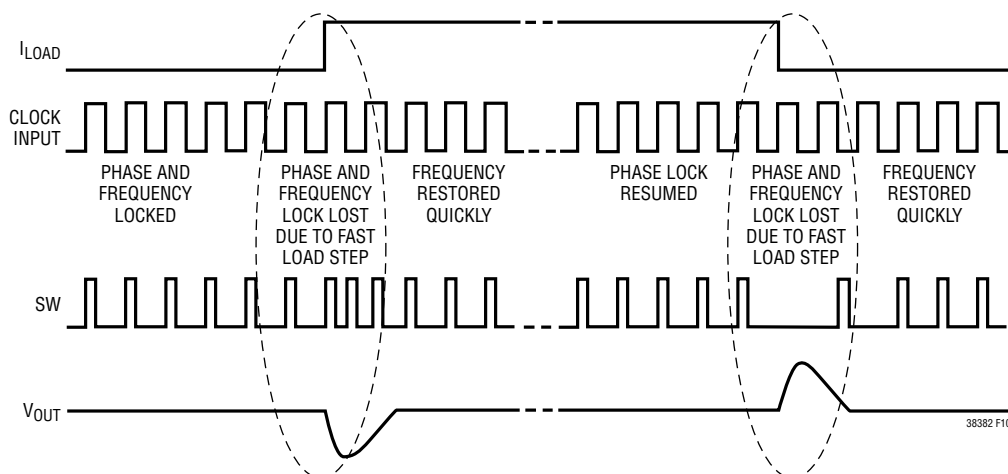


Figure 10. Phase and Frequency Locking Behavior During Transient Conditions

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still be maintained. For large load current steps with fast slew rates, phase lock will be lost until the system returns back to a steady-state condition (see Figure 10). It may take up to several hundred microseconds to fully resume the phase lock, but the frequency lock generally recovers quickly, long before phase lock does.

For light load conditions, the phase and frequency synchronization depends on the MODE/PLLIN pin setting. If the external clock is applied, synchronization will be active and switching in continuous mode. If MODE/PLLIN is tied to INTV<sub>CC</sub>, it will operate in forced continuous mode at the R<sub>T</sub>-programmed frequency. If the MODE/PLLIN pin is tied to SGND, the LTC3838-2 will operate in discontinuous mode at light load and switch into continuous conduction at the R<sub>T</sub> programmed frequency as load increases. The TG on-time during discontinuous conduction is intentionally slightly extended (approximately 1.2 times the continuous conduction on-time as calculated from V<sub>IN</sub>, V<sub>OUT</sub> and f) to create hysteresis at the load-current boundary of continuous/discontinuous conduction.

If an application requires very low (approaching minimum) on-time, the system may not be able to maintain its full frequency synchronization range. Getting closer to minimum on-time, it may even lose phase/frequency lock at no load or light load conditions, under which the SW on-time is effectively longer than TG on-time due to TG/BG dead times. This is discussed further under Minimum On-Time, Minimum Off-Time and Dropout Operation.

### Minimum On-Time, Minimum Off-Time and Dropout Operation

The minimum on-time is the smallest duration that LTC3838-2's TG (top gate) pin can be in high or "on" state. It has dependency on the operating conditions of the switching regulator, and is a function of voltages on the V<sub>IN</sub> and V<sub>OUT</sub> pins, as well as the value of external resistor R<sub>T</sub>. As shown by the t<sub>ON(MIN)</sub> curves in the Typical Performance Characteristics section, a minimum on-time of 30ns can be achieved when V<sub>OUT</sub>, sensed by the SENSE<sup>-</sup> pin, is at 0.6V or lower, while the V<sub>IN</sub> is tied to its maximum value of 38V. For larger values of V<sub>OUT</sub>, smaller values of V<sub>IN</sub> and/or larger values of R<sub>T</sub> (i.e. lower f), the minimum achievable on-time will be longer. The valley mode control

architecture allows low on-time, making the LTC3838-2 suitable for high step-down ratio applications.

The *effective* on-time, as determined by the SW node pulse width, can be different from this TG on-time, as it also depends on external components, as well as loading conditions of the switching regulator. One of the factors that contributes to this discrepancy is the characteristics of the power MOSFETs. For example, if the top power MOSFET's turn-on delay is much smaller than the turn-off delay, the effective on-time will be longer than the TG on-time, limiting the effective minimum on-time to a larger value.

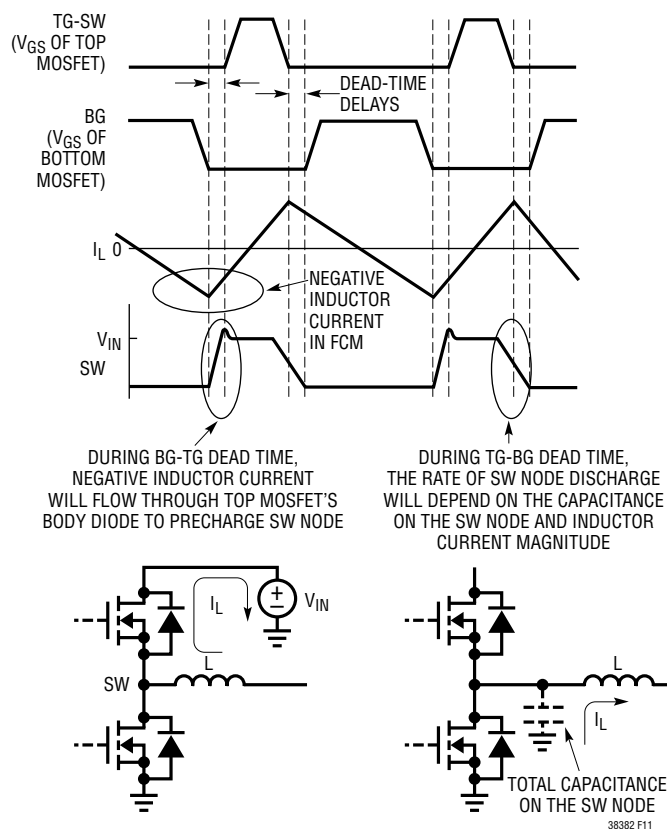
Light-load operation, in forced continuous mode, will further elongate the effective on-time due to the dead times between the "on" states of TG and BG, as shown in Figure 11. During the dead time from BG turn-off to TG turn-on, the inductor current flows in the reverse direction, charging the SW node high before the TG actually turns on. The reverse current is typically small, causing a slow rising edge. On the falling edge, after the top FET turns off and before the bottom FET turns on, the SW node lingers high for a longer duration due to a smaller peak inductor current available in light load to pull the SW node low. As a result of the sluggish SW node rising and falling edges, the effective on-time is extended and not fully controlled by the TG on-time. Closer to minimum on-time, this may cause some phase jitter to appear at light load. As load current increase, the edges become sharper, and the phase locking behavior improves.

In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$D_{\text{MIN}} = f \cdot t_{\text{ON(MIN)}}$$

where t<sub>ON(MIN)</sub> is the effective minimum on-time for the switching regulator. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. If the minimum on-time that LTC3838-2 can provide is longer than the on-time required by the duty cycle to maintain the switching frequency, the switching frequency will have to decrease to maintain the duty cycle, but the output voltage will still remain in regulation. This is generally more preferable to skipping cycles and causing larger ripple at the output, which is typically seen in fixed frequency switching regulators.

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**Figure 11. Light Loading On-Time Extension for Forced Continuous Mode Operation**

The  $t_{ON(MIN)}$  curves in the Typical Performance Characteristics are measured with minimum load on TG and BG, at extreme cases of  $V_{IN} = 38V$ , and/or  $V_{OUT} = 0.6V$ , and/or programmed  $f = 2MHz$  (i.e.,  $R_T = 18k$ ). In applications with different  $V_{IN}$ ,  $V_{OUT}$  and/or  $f$ , the  $t_{ON(MIN)}$  that can be achieved will generally be larger. Also, to guarantee frequency and phase locking at light load, sufficient margin needs to be added to account for the dead times ( $t_{D(TG/BG)} + t_{D(TG/BG)}$  in the Electrical Characteristics).

For applications that require relatively low on-time, proper caution has to be taken when choosing the power MOSFET. If the gate of the MOSFET is not able to fully turn on due to insufficient on-time, there could be significant heat dissipation and efficiency loss as a result of larger  $R_{DS(ON)}$ . This may even cause early failure of the power MOSFET.

The minimum off-time is the smallest duration of time that the TG pin can be turned low and then immediately turned back high. This minimum off-time includes the time to turn on the BG (bottom gate) and turn it back off, plus the dead-time delays from TG off to BG on and from BG off to TG on. The minimum off-time that the LTC3838-2 can achieve is 90ns.

The *effective* minimum off-time of the switching regulator, or the shortest period of time that the SW node can stay low, can be different from this minimum off-time. The main factor impacting the effective minimum off-time is the top and bottom power MOSFETs' electrical characteristics, such as  $Q_g$  and turn-on/off delays. These characteristics can either extend or shorten the SW nodes' effective minimum off-time. Large size (high  $Q_g$ ) power MOSFETs generally tend to increase the effective minimum off-time due to longer gate charging and discharging times. On the other hand, imbalances in turn-on and turn-off delays could reduce the effective minimum off-time.

The minimum off-time limit imposes a maximum duty cycle of:

$$D_{MAX} = 1 - f \cdot t_{OFF(MIN)}$$

where  $t_{OFF(MIN)}$  is the effective minimum off-time of the switching regulator. Reducing the operating frequency can alleviate the maximum duty cycle constraint.

If the maximum duty cycle is reached, due to a drooping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{D_{MAX}}$$

At the onset of drop-out, there is a region of  $V_{IN}$  of about 500mV that generates two discrete off-times, one being the minimum off time and the other being an off-time that is about 40ns to 60ns longer than the minimum off-time. This secondary off-time is due to the extra delay in tripping the internal current comparator. The two off-times average out to the required duty cycle to keep the output in regulation. There may be higher SW node jitter, apparent especially when synchronized to an external clock, but the output voltage ripple remains relatively small.

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### Fault Conditions: Current Limiting and Overvoltage

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3838-2, the maximum sense voltage is controlled by the voltage on the  $V_{\text{RNG}}$  pin. With valley current mode control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{\text{LIMIT}} = \frac{V_{\text{SENSE(MAX)}}}{R_{\text{SENSE}}} + \frac{1}{2} \cdot \Delta I_{\text{L}}$$

The current limit value should be checked to ensure that  $I_{\text{LIMIT(MIN)}} > I_{\text{OUT(MAX)}}$ . The current limit value should be greater than the inductor current required to produce maximum output power at the worst-case efficiency.

Worst-case efficiency typically occurs at the highest  $V_{\text{IN}}$  and highest ambient temperature. It is important to check for consistency between the assumed MOSFET junction temperatures and the resulting value of  $I_{\text{LIMIT}}$  which heats the MOSFET switches.

To further limit current in the event of a short circuit to ground, the LTC3838-2 includes foldback current limiting. If the output falls by more than 50%, the maximum sense voltage is progressively lowered, to about one-fourth of its full value as the feedback voltage reaches 0V.

A feedback voltage exceeding 7.5% of the regulated target of 0.6V is considered as overvoltage (OV). In such an OV condition, the top MOSFET is immediately turned off and the bottom MOSFET is turned on indefinitely until the OV condition is removed, i.e., the feedback voltage falling back below the 7.5% threshold by more than a hysteresis of around 15mV (on the same scale as each channel's reference and internal feedback voltages  $V_{\text{FB1,2}}$ ). Current limiting is not active during an OV. If the OV persists, and the BG turns on for a longer time, the current through the inductor and the bottom MOSFET may exceed their maximum ratings, sacrificing themselves to protect the load.

### OPTI-LOOP® Compensation

OPTI-LOOP compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control-loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly 2nd order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The external series  $R_{\text{ITH}}\text{-}C_{\text{ITH1}}$  filter at the ITH pin sets the dominant pole-zero loop compensation. The values can be adjusted to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected first because their various types and values determine the loop feedback factor gain and phase.

An additional small capacitor,  $C_{\text{ITH2}}$ , can be placed from the ITH pin to SGND to attenuate high frequency noise. Note this  $C_{\text{ITH2}}$  contributes an additional pole in the loop gain therefore can affect system stability if too large. It should be chosen so that the added pole is higher than the loop bandwidth by a significant margin.

The regulator loop response can also be checked by looking at the load transient response. An output current pulse of 20% to 100% of full-load current having a rise time of 1 $\mu$ s to 10 $\mu$ s will produce  $V_{\text{OUT}}$  and ITH voltage transient-response waveforms that can give a sense of the overall loop stability without breaking the feedback loop. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{\text{OUT}}$  immediately shifts by an amount equal to  $\Delta I_{\text{LOAD}} \cdot \text{ESR}$ , where ESR is the effective series resistance of  $C_{\text{OUT}}$ .  $\Delta I_{\text{LOAD}}$  also begins to charge or discharge  $C_{\text{OUT}}$ , generating a feedback error signal used by the regulator to return  $V_{\text{OUT}}$  to its steady-state value. During this recovery time,  $V_{\text{OUT}}$  can be monitored for overshoot or ringing that would indicate a stability problem.

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Connecting a resistive load in series with a power MOSFET, then placing the two directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in load current may not be within the bandwidth of the feedback loop, so it cannot be used to determine phase margin. The output voltage settling behavior is more related to the stability of the closed-loop system. However, it is better to look at the filtered and compensated feedback loop response at the ITH pin.

The gain of the loop increases with the  $R_{ITH}$  and the bandwidth of the loop increases with decreasing  $C_{ITH1}$ . If  $R_{ITH}$  is increased by the same factor that  $C_{ITH1}$  is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor,  $C_{FF}$ , can be added to improve the high frequency response, as used in the typical application at the last page of this data sheet. Feedforward capacitor  $C_{FF}$  provides phase lead by creating a high frequency zero with  $R_{FB2}$  which improves the phase margin.

A more severe transient can be caused by switching in loads with large supply bypass capacitors. The discharged bypass capacitors of the load are effectively put in parallel with the converter's  $C_{OUT}$ , causing a rapid drop in  $V_{OUT}$ . No regulator can deliver current quick enough to prevent this sudden step change in output voltage, if the switch connecting the  $C_{OUT}$  to the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. Hot Swap™ controllers are designed specifically for this purpose and usually incorporate current limiting, short-circuit protection and soft starting.

### Load-Release Transient Detection

As the output voltage requirement of step-down switching regulators becomes lower,  $V_{IN}$  to  $V_{OUT}$  step-down ratio increases, and load transients become faster, a major challenge is to limit the overshoot in  $V_{OUT}$  during a fast load current drop, or “load-release” transient.

Inductor current slew rate  $di_L/dt = V_L/L$  is proportional to voltage across the inductor  $V_L = V_{SW} - V_{OUT}$ . When the top MOSFET is turned on,  $V_L = V_{IN} - V_{OUT}$ , inductor current ramps up. When bottom MOSFET turns on,  $V_L = V_{SW} - V_{OUT} = -V_{OUT}$ , inductor current ramps down. At very low  $V_{OUT}$ , the low differential voltage,  $V_L$ , across the inductor during the ramp down makes the slew rate of the inductor current much slower than needed to follow the load current change. The excess inductor current charges up the output capacitor, which causes overshoot at  $V_{OUT}$ .

If the bottom MOSFET could be turned off during the load-release transient, the inductor current would flow through the body diode of the bottom MOSFET, and the equation can be modified to include the bottom MOSFET body diode drop to become  $V_L = -(V_{OUT} + V_{BD})$ . Obviously the benefit increases as the output voltage gets lower, since  $V_{BD}$  would increase the sum significantly, compared to a single  $V_{OUT}$  only.

The load-release overshoot at  $V_{OUT}$  causes the error amplifier output, ITH, to drop quickly. ITH voltage is proportional to the inductor current setpoint. A load transient will result in a quick change of this load current setpoint, i.e., a negative spike of the first derivative of the ITH voltage.

The LTC3838-2 uses a detect transient (DTR) pin to monitor the first derivative of the ITH voltage, and detect the load-release transient. Referring to the Functional Diagram, the DTR pin is the input of a DTR comparator, and the internal reference voltage for the DTR comparator is half of  $INTV_{CC}$ . To use this pin for transient detection, ITH compensation needs an additional  $R_{ITH}$  resistor tied to  $INTV_{CC}$ , and connects the junction point of ITH compensation components  $C_{ITH1}$ ,  $R_{ITH1}$  and  $R_{ITH2}$  to the DTR pin as shown in the Functional Diagram. The DTR pin is now proportional to the first derivative of the inductor current setpoint, through the highpass filter of  $C_{ITH1}$  and  $(R_{ITH1}/R_{ITH2})$ .

The two  $R_{ITH}$  resistors establish a voltage divider from  $INTV_{CC}$  to SGND, and bias the DC voltage on DTR pin (at steady-state load or ITH voltage) slightly above half of  $INTV_{CC}$ . Compensation performance will be identical by

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using the same  $C_{ITH1}$  and make  $R_{ITH1}/R_{ITH2}$  equal the  $R_{ITH}$  as used in conventional single resistor OPTI-LOOP compensation. This will also provide the R-C time constant needed for the DTR duration. The DTR sensitivity can be adjusted by the DC bias voltage difference between DTR and half  $INTV_{CC}$ . This difference could be set as low as 200mV, as long as the ITH ripple voltage with DC load current does not trigger the DTR.

Note the internal 2.5µA pull-up current from the DTR pin will generate an additional offset on top of the resistor divider itself, making the total difference between the DC bias voltage on the DTR pin and half  $INTV_{CC}$ :

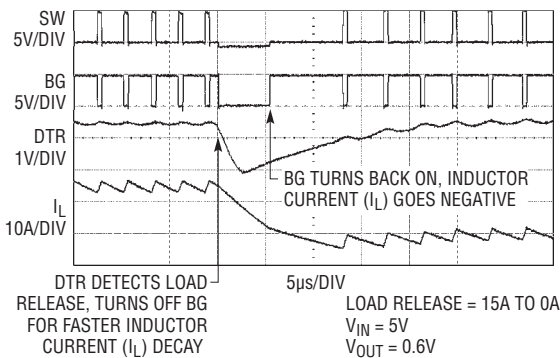
$$V_{DTR} - 0.5V_{INTV_{CC}} = \left[ \frac{R_{ITH1}}{(R_{ITH1} + R_{ITH2})} - 0.5 \right] \cdot 5.3V + 2.5\mu A \cdot (R_{ITH1} // R_{ITH2})$$

As illustrated in Figure 12, when load current suddenly drops,  $V_{OUT}$  overshoots, and ITH drops quickly. The voltage on the DTR pin will also drop quickly, since it is coupled to the ITH pin through a capacitor. If the load transient is fast enough that the DTR voltage drops below half of  $INTV_{CC}$ , a load release event is detected. The bottom gate (BG) will be turned off, so that the inductor current flows through the body diode in the bottom MOSFET. This allows the SW node to drop below PGND by a voltage of a forward-conducted silicon diode. This creates a more negative differential voltage ( $V_{SW} - V_{OUT}$ ) across the inductor, allowing the inductor current to drop at a faster rate to zero, therefore creating less overshoot on  $V_{OUT}$ .

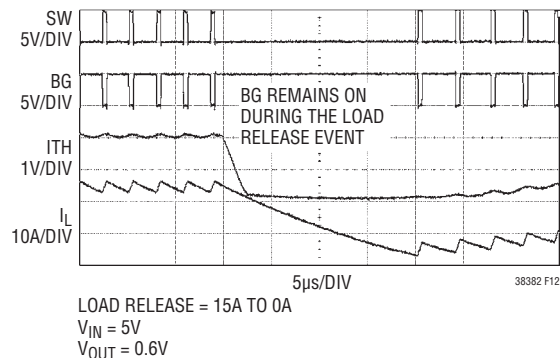
The DTR comparator output is overridden by reverse inductor current detection ( $I_{REV}$ ) and overvoltage (OV) condition. This means BG will be turned off when  $SENSE^+$  is higher than  $SENSE^-$  (i.e., inductor current is positive), as long as the OV condition is not present. When inductor current drops to zero and starts to reverse, BG will turn back on in forced continuous mode (e.g., the MODE/PLLIN pin tied to  $INTV_{CC}$ , or an input clock is present), even if DTR is still below half  $INTV_{CC}$ . This is to allow the inductor current to go negative to quickly pull down the  $V_{OUT}$  overshoot. Of course, if the MODE/PLLIN pin is set to discontinuous mode (i.e., tied to SGND), BG will stay off as inductor current reverse, as it would with the DTR feature disabled.

Also, if  $V_{OUT}$  gets higher than the OV window (7.5% typical), the DTR function is defeated and BG will turn on regardless. Therefore, in order for the DTR feature to reduce  $V_{OUT}$  overshoot effectively, sufficient output capacitance needs to be used in the application so that OV is not triggered with the amount of load step desired to have its overshoot suppressed.

Experimenting with a 0.6V output application (modified from the design example circuit by setting  $V_{OUT}$  to 0.6V and ITH compensation adjusted accordingly) shows this detect transient feature significantly reduces the overshoot peak voltage, as well as time to resume regulation during load release steps (see application examples in Typical Performance Characteristics).



(12a) DTR Enabled



(12b) DTR Disabled

Figure 12. Comparison of  $V_{OUT}$  Overshoot with Detect Transient (DTR) Feature Enabled and Disabled

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Note that it is expected that this DTR feature will cause additional loss on the bottom MOSFET, due to its body diode conduction. The bottom MOSFET temperature may be higher with a load of frequent and large load steps. This is an important design consideration. Experiments on the demo board show a 20°C increase when a continuous 100% to 50% load step pulse train with 50% duty cycle and 100kHz frequency is applied to the output.

If not needed, this DTR feature can be disabled by tying the DTR pin to INTV<sub>CC</sub>, or simply leave the DTR pin open so that an internal 2.5µA current source will pull itself up to INTV<sub>CC</sub>.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percentage efficiency can be expressed as:

$$\% \text{Efficiency} = 100\% - (L1\% + L2\% + L3\% + \dots)$$

where L1%, L2%, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce power losses, several main sources usually account for most of the losses:

1.  $I^2R$  loss. These arise from the DC resistances of the MOSFETs, inductor, current sense resistor and is the majority of power loss at high output currents. In continuous mode the average output current flows through the inductor L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same  $R_{DS(ON)}$ , then the resistance of one MOSFET can simply be summed with the inductor's DC resistances (DCR) and the board traces to obtain the  $I^2R$  loss. For example, if each  $R_{DS(ON)} = 8\text{m}\Omega$ ,  $R_L = 5\text{m}\Omega$ , and  $R_{SENSE} = 2\text{m}\Omega$  the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A. This results in loss from 0.3% to 3% a 5V output, or 1% to 10% for a 1.5V output. Efficiency varies as the inverse square of  $V_{OUT}$  for the same external components and output power level. The combined effects of lower output voltages and higher currents load demands greater importance of this loss term in the switching regulator system.
2. Transition loss. This loss mostly arises from the brief amount of time the top MOSFET spends in the saturation (Miller) region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors, and can be significant at higher input voltages or higher switching frequencies.
3. DRV<sub>CC</sub> current. This is the sum of the MOSFET driver and INTV<sub>CC</sub> control currents. The MOSFET driver currents result from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from DRV<sub>CC</sub> to ground. The resulting dQ/dt is a current out of DRV<sub>CC</sub> that is typically much larger than the controller I<sub>Q</sub> current. In continuous mode,
 
$$I_{\text{GATECHG}} = f \cdot (Q_{g(\text{TOP})} + Q_{g(\text{BOT})}),$$
 where  $Q_{g(\text{TOP})}$  and  $Q_{g(\text{BOT})}$  are the gate charges of the top and bottom MOSFETs, respectively.
 

Supplying DRV<sub>CC</sub> power through EXT<sub>V</sub><sub>CC</sub> could increase efficiency by several percent, especially for high  $V_{IN}$  applications. Connecting EXT<sub>V</sub><sub>CC</sub> to an output-derived source will scale the  $V_{IN}$  current required for the driver and controller circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of DRV<sub>CC</sub> current results in approximately 2.5mA of  $V_{IN}$  current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from  $V_{IN}$ ) to only a few percent.
4. C<sub>IN</sub> loss. The input capacitor filters large square-wave input current drawn by the regulator into an averaged DC current from the supply. The capacitor itself has a zero average DC current, but square-wave-like AC current flows through it. Therefore the input capacitor must have a very low ESR to minimize the RMS current loss on ESR. It must also have sufficient capacitance to filter out the AC component of the input current to prevent additional RMS losses in upstream cabling, fuses or batteries. The LTC3838-2's 2-phase architecture improves the ESR loss.

## APPLICATIONS INFORMATION

“Hidden” copper trace, fuse and battery resistance, even at DC current, can cause a significant amount of efficiency degradation, so it is important to consider them during the design phase. Other losses, which include the  $C_{OUT}$  ESR loss, bottom MOSFET’s body diode reverse-recovery loss, and inductor core loss generally account for less than 2% additional loss.

Power losses in the switching regulator will reflect as a higher than ideal duty cycle, or a longer on-time for a constant frequency. This efficiency accounted on-time can be calculated as:

$$t_{ON} \approx t_{ON(IDEAL)} / \text{Efficiency}$$

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased.

### Design Example

Consider a channel of step-down converter from  $V_{IN} = 4.5V$  to  $26V$  to  $V_{OUT} = 1.2V$ , with  $I_{OUT(MAX)} = 15A$ , and  $f = 350kHz$  (see Figure 13, channel 1).

The regulated output voltage of channel 1 is determined by:

$$V_{OUT1} = 0.6V \cdot \left( 1 + \frac{R_{FB2}}{R_{FB1}} \right)$$

Using a 10k resistor for  $R_{FB1}$ ,  $R_{FB2}$  is also 10k.

Channel 2 uses an external reference and requires an additional resistor to the remote ground of the external reference (See Output Voltage Programming section). The value of the additional resistor is equal to the parallel of the two feedback resistors. If such an exact resistor value is not available, simply use two additional resistors in parallel for the best accuracy.

The frequency is programmed by:

$$R_T [k\Omega] = \frac{41550}{f [kHz]} - 2.2 = \frac{41550}{350} - 2.2 \approx 116.5$$

Use the nearest 1% resistor standard value of 115k.

The minimum on-time occurs for maximum  $V_{IN}$ . Using the  $t_{ON(MIN)}$  curves in the Typical Performance Characteristics as references, make sure that the  $t_{ON(MIN)}$  at maximum  $V_{IN}$  is greater than that the LTC3838-2 can achieve, and allow sufficient margin to account for the extension of effective on-time at light load due to the dead times ( $t_{D(TG/BG)} + t_{D(TG/BG)}$  in the Electrical Characteristics). The minimum on-time for this application is:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot f} = \frac{1.2V}{24V \cdot 350kHz} = 143ns$$

Set the inductor value to give 40% ripple current at maximum  $V_{IN}$  using the adjusted operating frequency:

$$L = \left( \frac{1.2V}{350kHz \cdot 40\% \cdot 15A} \right) \left( 1 - \frac{1.2V}{24V} \right) = 0.54\mu H$$

Select 0.56 $\mu H$  which is the nearest standard value.

The resulting maximum ripple current is:

$$\Delta I_L = \left( \frac{1.2V}{350kHz \cdot 0.56\mu H} \right) \left( 1 - \frac{1.2V}{24V} \right) = 5.8A$$

Often in a high current application, DCR current sensing is preferred over  $R_{SENSE}$  in order to maximize efficiency. In order to determine the DCR filter values, first the inductor manufacturer has to be chosen. For this design, the Vishay IHL-4040DZ-01 model is chosen with a value of 0.56 $\mu H$  and a  $DCR_{MAX} = 1.8m\Omega$ . This implies that:

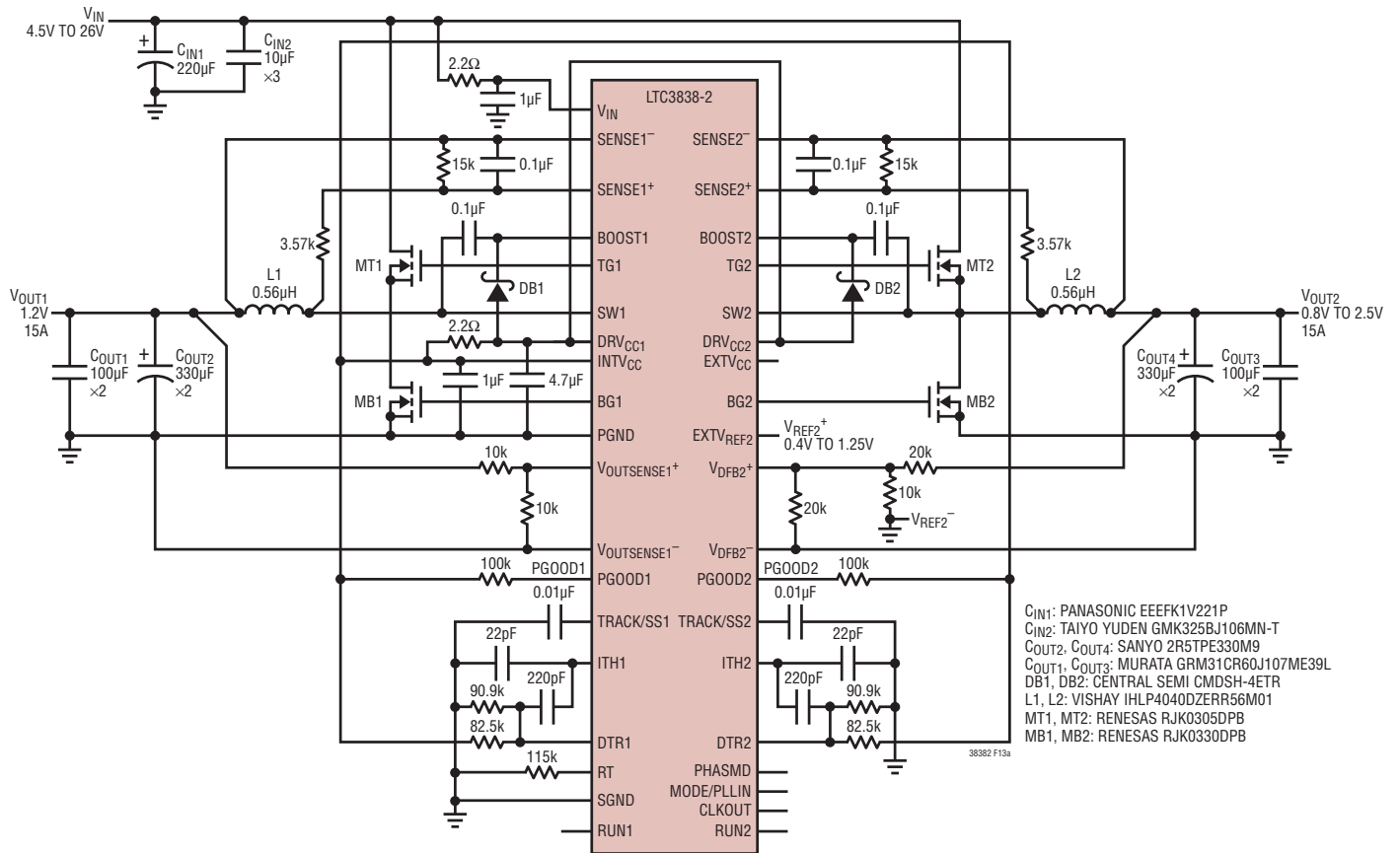
$$V_{SENSE(MAX)} = 1.8m\Omega \cdot [1 + (100^\circ C - 25^\circ C) \cdot 0.4\%/^\circ C] \cdot (15A - 5.8A/2) = 28mV$$

The maximum sense voltage,  $V_{SENSE(MAX)}$ , is within the range that LTC3838-2 can handle without any additional scaling. Therefore, the DCR filter can use a simple RC filter across the inductor. If the C is chosen to be 0.1 $\mu F$ , then the R can be calculated as:

$$R_{DCR} = \frac{L}{DCR \cdot C_{DCR}} = \frac{0.56\mu H}{1.8m\Omega \cdot 0.1\mu F} = 3.1k\Omega$$



# APPLICATIONS INFORMATION



C<sub>IN1</sub>: PANASONIC EEEFK1V221P  
 C<sub>IN2</sub>: TAIYO YUDEN GMK325BJ106MN-T  
 C<sub>OUT2</sub>, C<sub>OUT4</sub>: SANYO 2R5TPE330M9  
 C<sub>OUT1</sub>, C<sub>OUT3</sub>: MURATA GRM31CR60J107ME39L  
 DB1, DB2: CENTRAL SEMI CMDSH-4ETR  
 L1, L2: VISHAY IHLP4040DZER56M01  
 MT1, MT2: RENESAS RJK0305DPB  
 MB1, MB2: RENESAS RJK0330DPB

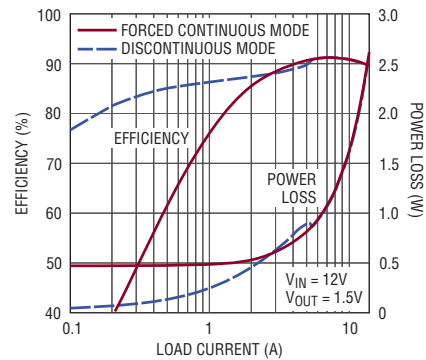
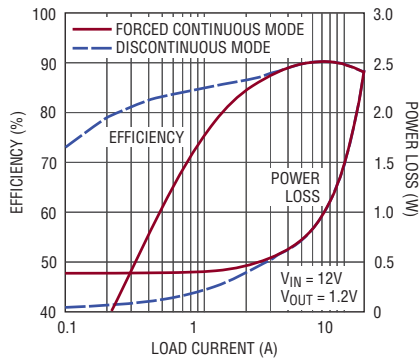


Figure 13. Design Example: 4.5V to 26V Input, 1.2V/15A and 0.8V to 2.5V/15A (V<sub>OUT2</sub>: EXT<sub>REF2</sub> = 2:1) Dual Outputs, 350kHz, DCR Sense, DTR Enabled, Step-Down Converter

## APPLICATIONS INFORMATION

Use an additional resistor in the DCR filter, as discussed in DCR Inductor Current Sensing, to scale the  $V_{\text{SENSE(MAX)}}$  down by a comfortable margin below the lower limit of the LTC3838-2's own  $V_{\text{SENSE(MAX)}}$  specification, so that the maximum output current can be guaranteed.

In this design example, a 3.57k and 15k resistor divider is used. The previously calculated  $V_{\text{SENSE(MAX)}}$  is scaled down from 28mV to 22.6mV, which is close to the lower limit of LTC3838-2's  $V_{\text{SENSE(MAX)}}$  specification. Note the equivalent  $R_{\text{DCR}} = 3.57\text{k}/15\text{k} = 2.9\text{k}$ , slightly lower than the 3.1k calculated above for a matched  $R_{\text{DCR}}-C_{\text{DCR}}$  and L-DCR network. The resulted mismatch allows for a slightly higher ripple in  $V_{\text{SENSE}}$ .

Remember to check the maximum possible peak inductor current, considering the upper spec limit of  $V_{\text{SENSE(MAX)}}$  and the  $\text{DCR}_{\text{(MIN)}}$  at lowest operating temperature, as well as the maximum  $\Delta I_L$ , is not going to saturate the inductor or exceed the rating of power MOSFETs:

$$I_{\text{L(PEAK)}} = \frac{V_{\text{SENSE(MAX)(Upper Spec Limit)}}}{\text{DCR}_{\text{MIN}} [1 + (T_{\text{MIN}} - 25^\circ\text{C}) \cdot 0.4\% / ^\circ\text{C}]} + \Delta I_{\text{L(MAX)}}$$

For the external N-channel MOSFETs, Renesas RJK0305DBP ( $R_{\text{DS(ON)}} = 13\text{m}\Omega$  max,  $C_{\text{MILLER}} = 150\text{pF}$ ,  $V_{\text{GS}} = 4.5\text{V}$ ,  $\theta_{\text{JA}} = 40^\circ\text{C/W}$ ,  $T_{\text{J(MAX)}} = 150^\circ\text{C}$ ) is chosen for the top MOSFET (main switch). RJK-0330DBP ( $R_{\text{DS(ON)}} = 3.9\text{m}\Omega$  max,  $V_{\text{GS}} = 4.5\text{V}$ ,  $\theta_{\text{JA}} = 40^\circ\text{C/W}$ ,  $T_{\text{J(MAX)}} = 150^\circ\text{C}$ ) is chosen for the bottom MOSFET (synchronous switch). The power dissipation for each MOSFET can be calculated for  $V_{\text{IN}} = 24\text{V}$  and typical  $T_{\text{J}} = 125^\circ\text{C}$ :

$$\begin{aligned} P_{\text{TOP}} &= \left(\frac{1.2\text{V}}{24\text{V}}\right) (15\text{A})^2 (13\text{m}\Omega) [1 + 0.4\% (125^\circ\text{C} - 25^\circ\text{C})] \\ &\quad + (24\text{V})^2 \left(\frac{15\text{A}}{2}\right) (150\text{pF}) \left[\frac{2.5\Omega}{5.3\text{V} - 3\text{V}} + \frac{1.2\Omega}{3\text{V}}\right] (350\text{kHz}) \\ &= 0.54\text{W} \\ P_{\text{BOT}} &= \left(\frac{24\text{V} - 1.2\text{V}}{24\text{V}}\right) (15\text{A})^2 (3.9\text{m}\Omega) [1 + 0.4\% (125^\circ\text{C} - 25^\circ\text{C})] \\ &= 1.2\text{W} \end{aligned}$$

The resulted junction temperatures at an ambient temperature  $T_{\text{A}} = 75^\circ\text{C}$  are:

$$T_{\text{J(TOP)}} = 75^\circ\text{C} + (0.54\text{W})(40^\circ\text{C/W}) = 97^\circ\text{C}$$

$$T_{\text{J(BOT)}} = 75^\circ\text{C} + (1.2\text{W})(40^\circ\text{C/W}) = 123^\circ\text{C}$$

These numbers show that careful attention should be paid to proper heat sinking when operating at higher ambient temperatures.

Select the  $C_{\text{IN}}$  capacitors to give ample capacitance and RMS ripple current rating. Consider worst-case duty cycles per Figure 6: If operated at steady-state with SW nodes fully interleaved, the two channels would generate not more than 7.5A RMS at full load. In this design example,  $3 \times 10\mu\text{F}$  35V X5R ceramic capacitors are put in parallel to take the RMS ripple current, with a 220 $\mu\text{F}$  aluminum-electrolytic bulk capacitor for stability. For 10 $\mu\text{F}$  1210 X5R ceramic capacitors, try to keep the ripple current less than 3A RMS through each device. The bulk capacitor is chosen for RMS rating per simulation with the circuit model provided.

The output capacitor  $C_{\text{OUT}}$  is chosen for a low ESR of 4.5m $\Omega$  to minimize output voltage changes due to inductor ripple current and load steps. The output voltage ripple is given as:

$$\Delta V_{\text{OUT(RIPPLE)}} = \Delta I_{\text{L(MAX)}} \cdot \text{ESR} = 5.85\text{A} \cdot 4.5\text{m}\Omega = 26\text{mV}$$

However, a 10A load step will cause an output change of up to:

$$\Delta V_{\text{OUT(STEP)}} = \Delta I_{\text{LOAD}} \cdot \text{ESR} = 10\text{A} \cdot 4.5\text{m}\Omega = 45\text{mV}$$

Optional  $2 \times 100\mu\text{F}$  ceramic output capacitors are included to minimize the effect of ESR and ESL in the output ripple and to improve load step response.

The ITH compensation resistor  $R_{\text{ITH}}$  of 40k and a  $C_{\text{ITH}}$  of 220pF are chosen empirically for fast transient response, and an additional  $C_{\text{ITH2}} = 22\text{pF}$  is added directly from ITH pin to SGND, to roll off the system gain at switching frequency and attenuate high frequency noise. For less aggressive transient response but more stability, lower-valued  $R_{\text{ITH}}$  and higher-valued  $C_{\text{ITH}}$  and  $C_{\text{ITH2}}$  can be used (such as the various combinations used in Figures 16, 17, 18, 19, 20), which typically results in lower bandwidth but more phase margin.

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To set up the detect transient (DTR) feature, pick resistors for an equivalent  $R_{ITH} = R_{ITH1} // R_{ITH2}$  close to 40k. Here, 1% resistors  $R_{ITH1} = 90.9k$  (low side) and  $R_{ITH2} = 82.5k$  (high side) are used, which yields an equivalent  $R_{ITH}$  of 43.2k, and a DC-bias threshold of 236mV typical above one-half of  $INTV_{CC}$  (including the 2.5 $\mu$ A pull-up current from the DTR pin, see the Load-Release Transient Detection section). Note that even though the accuracy of the equivalent compensation resistance  $R_{ITH}$  is not as important, always use 1% or better resistors for the resistor divider from  $INTV_{CC}$  to SGND to guarantee the relative accuracy of this DC-bias threshold. To disable the DTR feature, simply use a single  $R_{ITH}$  resistor to SGND, and tie the DTR pin to  $INTV_{CC}$ .

If channel 2 uses an external reference voltage with a ratio of  $V_{OUT2}: V_{EXTVREF2} = 2:1$ , as in this design example, it would have the same ratio and overall system gain as channel 1 ( $V_{OUT1}: V_{INTVREF} = 1.2V: 0.6V = 2:1$ ), therefore the same values (as channel 1) of compensation components can be used on ITH2 pin. If another ratio is needed, the ITH compensation may need to be adjusted. Figure 17 shows an  $R_{SENSE}$  and DTR-disabled version of this design with a channel 2 that has  $V_{OUT2}: V_{EXTVREF2} = 1:1$ . Note that as  $EXTV_{REF2}$  is getting closer to its higher limit, the lower end of the  $V_{IN}$  range may require a higher value to guarantee the  $INTV_{CC}$  required at the  $EXTV_{REF2}$  applied (see the Electrical Characteristics section) and assure TRACK/SS2 settles well above  $EXTV_{REF2}$  when no external pull-up is used.

### PCB Layout Checklist

The printed circuit board layout is illustrated graphically in Figure 14. Figure 15 illustrates the current waveforms present in the various branches of 2-phase synchronous regulators operating in continuous mode. Use the following checklist to ensure proper operation:

- A multilayer printed circuit board with dedicated ground planes is generally preferred to reduce noise coupling and improve heat sinking. The ground plane layer should be immediately next to the routing layer for the power components, e.g., MOSFETs, inductors, sense resistors, input and output capacitors etc.
- Keep SGND and PGND separate. Upon finishing the layout, connect SGND and PGND together with a single PCB trace underneath the IC from the SGND pin through the exposed PGND pad to the PGND pin.
- All power train components should be referenced to PGND; all components connected to noise-sensitive pins, e.g., ITH, RT, TRACK/SS, etc., should return to the SGND pin. Keep PGND ample, but SGND area compact. Use a modified “star ground” technique: a low impedance, large copper area central PCB point on the same side of the as the input and output capacitors.
- Place power components, such as  $C_{IN}$ ,  $C_{OUT}$ , MOSFETs,  $D_B$  and inductors, in one compact area. Use wide but shortest possible traces for high current paths (e.g.,  $V_{IN}$ ,  $V_{OUT}$ , PGND etc.) to this area to minimize copper loss.
- Keep the switch nodes (SW1,2), top gates (TG1,2) and boost nodes (BOOST1,2) away from noise-sensitive small-signal nodes, especially from the opposite channel’s voltage and current sensing feedback pins. These nodes have very large and fast moving signals and therefore should be kept on the “output side” of the LTC3838-2 (power-related pins are toward the right hand side of the IC), and occupy minimum PC trace area. Use compact switch node (SW) planes to improve cooling of the MOSFETs and to keep EMI down. If DCR sensing is used, place the top filter resistor (R1 only in Figure 5) close to the switch node.

## APPLICATIONS INFORMATION

- The top N-channel MOSFETs of the two channels have to be located within a short distance from (preferably <1cm) each other with a common drain connection at  $C_{IN}$ . Do not attempt to split the input decoupling for the two channels as it can result in a large resonant loop.
- Connect the input capacitor(s),  $C_{IN}$ , close to the power MOSFETs. This capacitor provides the MOSFET transient spike current. Connect the drain of the top MOSFET as close as possible to the (+) plate of the ceramic portion of input capacitors  $C_{IN}$ . Connect the source of the bottom MOSFET as close as possible to the (-) terminal of the same ceramic  $C_{IN}$  capacitor(s). These ceramic capacitor(s) bypass the high di/dt current locally, and both top and bottom MOSFET should have short PCB trace lengths to minimize high frequency EMI and prevent MOSFET voltage stress from inductive ringing.
- The path formed by the top and bottom N-channel MOSFETs, and the  $C_{IN}$  capacitors should have short leads and PCB trace. The (-) terminal of output capacitors should be connected close to the (-) terminal of  $C_{IN}$ , but away from the loop described above. This is to achieve an effect of Kelvin (4-wire) connection to the input ground so that the “chopped” switching current will not flow through the path between the input ground and the output ground, and cause common mode output voltage ripple.
- Several smaller sized ceramic output capacitors,  $C_{OUT}$ , can be placed close to the sense resistors and before the rest bulk output capacitors.
- The filter capacitor between the  $SENSE^+$  and  $SENSE^-$  pins should always be as close as possible to these pins. Ensure accurate current sensing with Kelvin (4-wire) connections to the soldering pads from underneath the sense resistors or inductor. A pair of sense traces should be routed together with minimum spacing.  $R_{SENSE}$ , if used, should be connected to the inductor on the noiseless output side, and its filter resistors close to the  $SENSE^+/SENSE^-$  pins. For DCR sensing, however, filter resistor should be placed close to the inductor, and away from the  $SENSE^+/SENSE^-$  pins, as its terminal is the SW node.
- Keep small-signal components connected noise-sensitive pins (give priority to  $SENSE^+/SENSE^-$ ,  $V_{OUTSENSE1^+}/V_{OUTSENSE1^-}$ ,  $V_{DFB2^+}/V_{DFB2^-}$ , RT, ITH, etc.) on the left hand side of the IC as close to their respective pins as possible. This minimizes the possibility of noise coupling into these pins. If the LTC3838-2 can be placed on the bottom side of a multilayer board, use ground planes to isolate from the major power components on the top side of the board, and prevent noise coupling to noise sensitive components on the bottom side.
- Place the resistor feedback dividers close to the  $V_{OUTSENSE1^+}$  and  $V_{OUTSENSE1^-}$  pins for channel 1, or the  $V_{DFB2^+}$  and  $V_{DFB2^-}$  pins for channel 2, so that the feedback voltage tapped from the resistor divider will not be disturbed by noise sources. Route remote sense PCB traces (use a pair of wires closely together for differential sensing) directly to the terminals of output capacitors for best output regulation.
- Place decoupling capacitors  $C_{ITH2}$  next to the ITH and SGND pins with short, direct trace connections.
- Use sufficient isolation when routing a clock signal into the MODE/PLLIN pin or out of the CLKOUT pin, so that the clock does not couple into sensitive pins.
- Place the ceramic decoupling capacitor  $C_{INTVCC}$  between the INTVCC pin and SGND and as close as possible to the IC.
- Place the ceramic decoupling capacitor  $C_{DRVCC}$  close to the IC, between the combined  $DRV_{CC1,2}$  pins and PGND.
- Filter the  $V_{IN}$  input to the LTC3838-2 with an RC filter. Place the filter capacitor close to the  $V_{IN}$  pin.
- If vias have to be used, use immediate vias to connect components to the SGND and PGND planes of LTC3838-2. Use multiple large vias for power components.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to DC rails only, e.g., PGND.

## APPLICATIONS INFORMATION

### PCB Layout Debugging

Only after each controller is checked for its individual performance should both controllers be turned on at the same time. It is helpful to use a current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator output CLKOUT, or external clock if used. Probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application.

The frequency of operation should be maintained over the input voltage range. The phase should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the phase of SW node pulse can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PCB layout if regulator bandwidth optimization is not required.

Pay special attention to the region of operation when one controller channel is turning on (right after its current comparator trip point) while the other channel is turning off its top MOSFET at the end of its on-time. This may cause minor phase-lock jitter at either channel due to noise coupling.

Reduce  $V_{IN}$  from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering  $V_{IN}$  while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins.

The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between  $C_{IN}$ , top and bottom MOSFET components to the sensitive current and voltage sensing traces.

In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

### High Switching Frequency Operation

At high switching frequencies there may be an increased sensitivity to noise. Special care may need to be taken to prevent cycle-by-cycle instability and/or phase-lock jitter. First, carefully follow the recommended layout techniques to reduce coupling from the high switching voltage/current traces. Additionally, use low ESR and low impedance X5R or X7R ceramic input capacitors: up to  $5\mu\text{F}$  per Ampere of load current may be needed.

APPLICATIONS INFORMATION

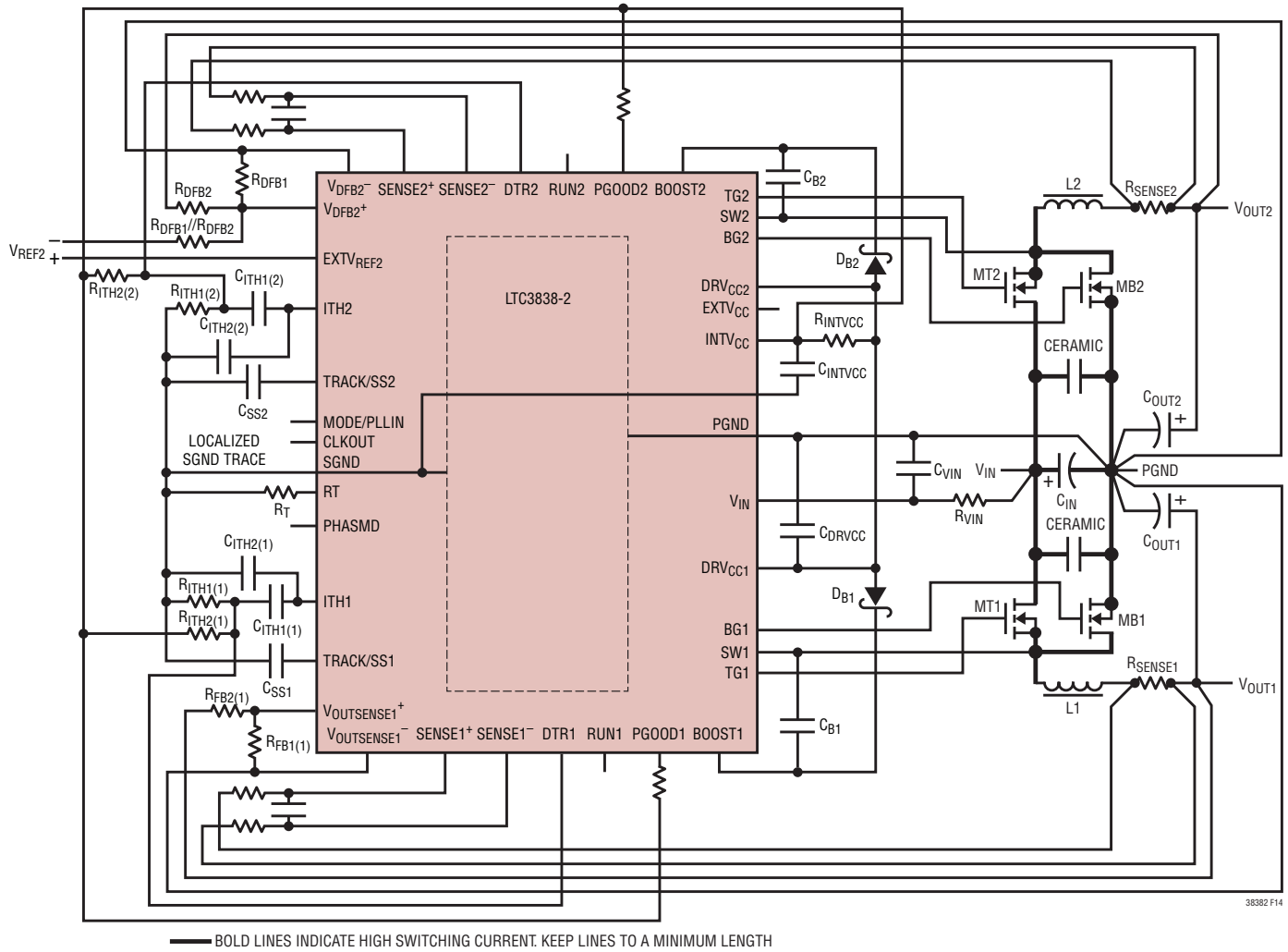


Figure 14. Recommended PCB Layout Diagram

APPLICATIONS INFORMATION

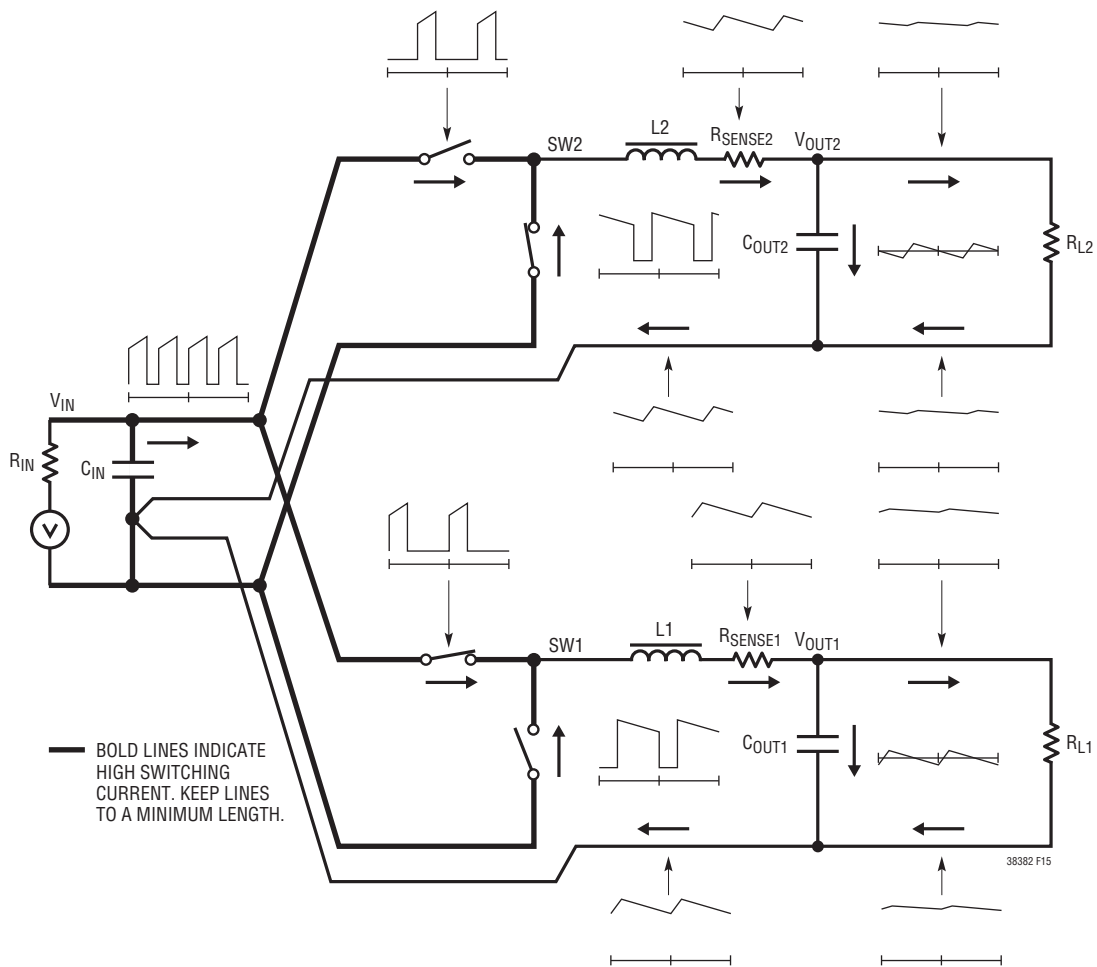
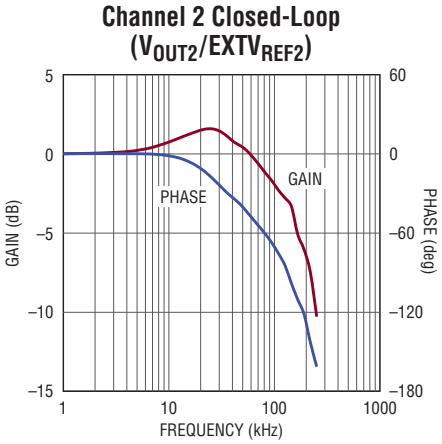
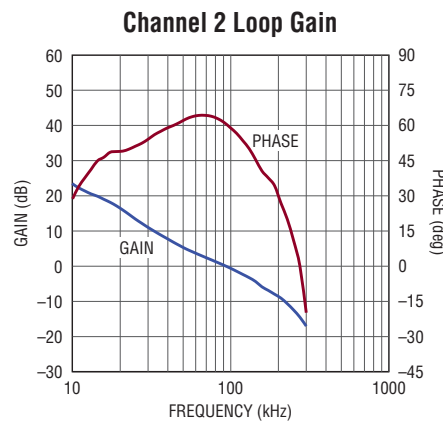
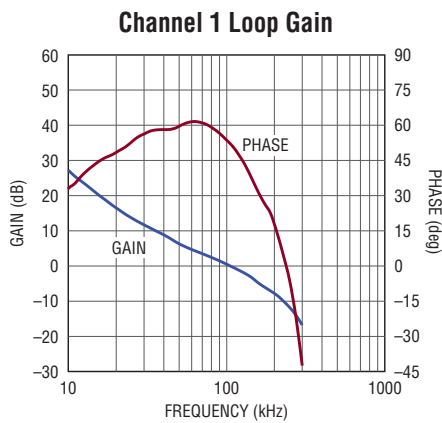
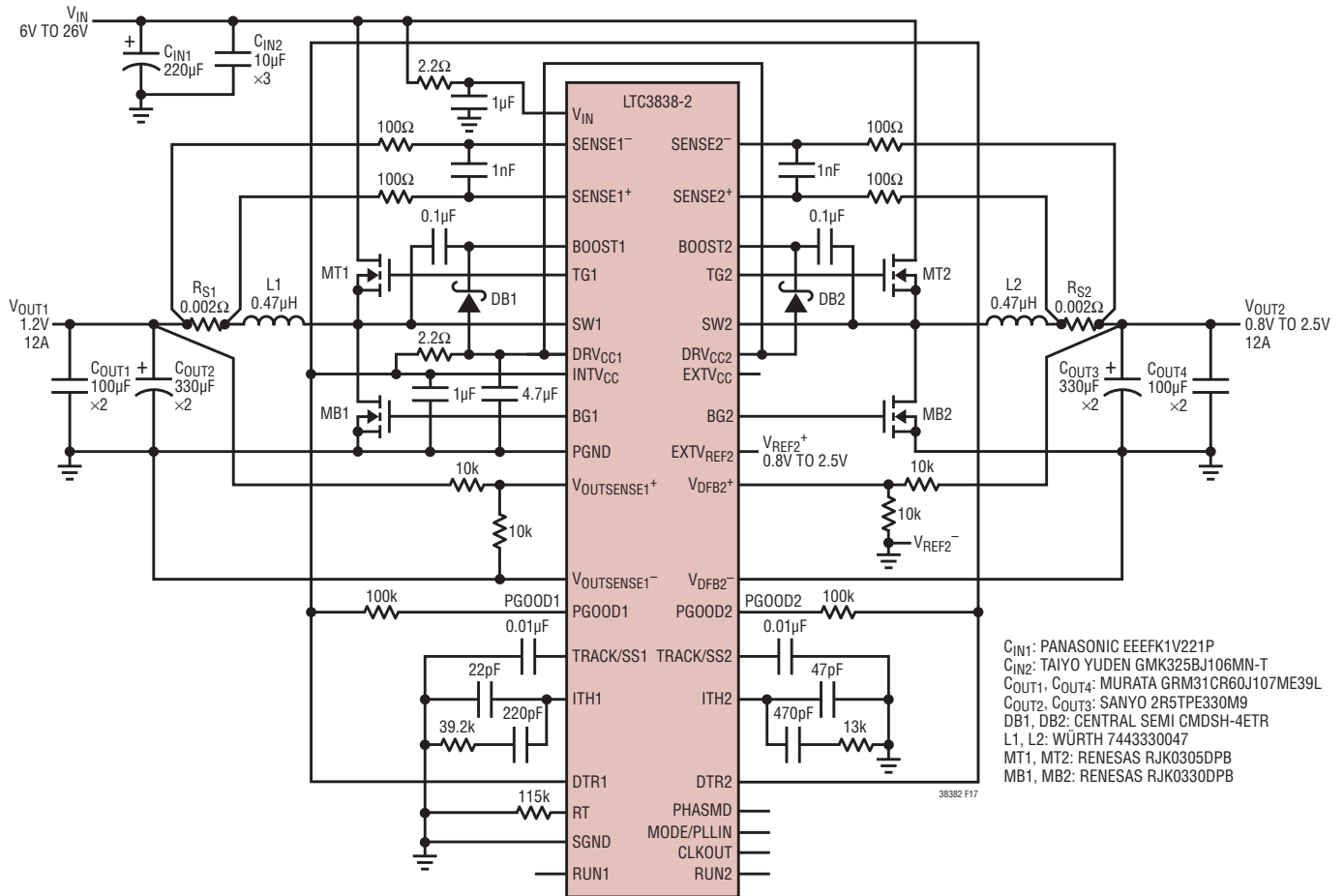


Figure 15. Branch Current Waveforms





TYPICAL APPLICATIONS



Bode plots taken with OMICRON Lab Bode 100 Vector Network Analyzer.

Figure 17. 6V to 26V Input, 1.2V/15A and 0.8V to 2.5V/15A ( $V_{OUT2}: EXT_{REF2} = 1:1$ ) Dual Output, 350kHz,  $R_{SENSE}$ , Step-Down Converter

## TYPICAL APPLICATIONS

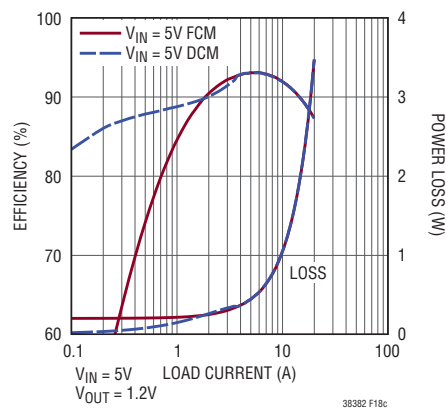
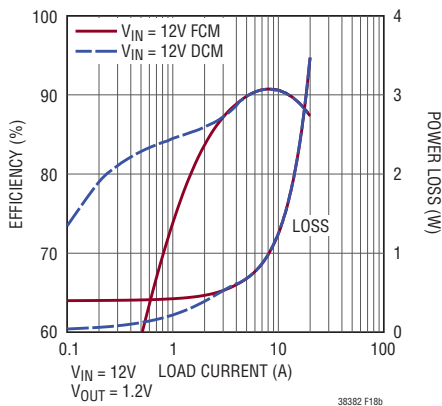
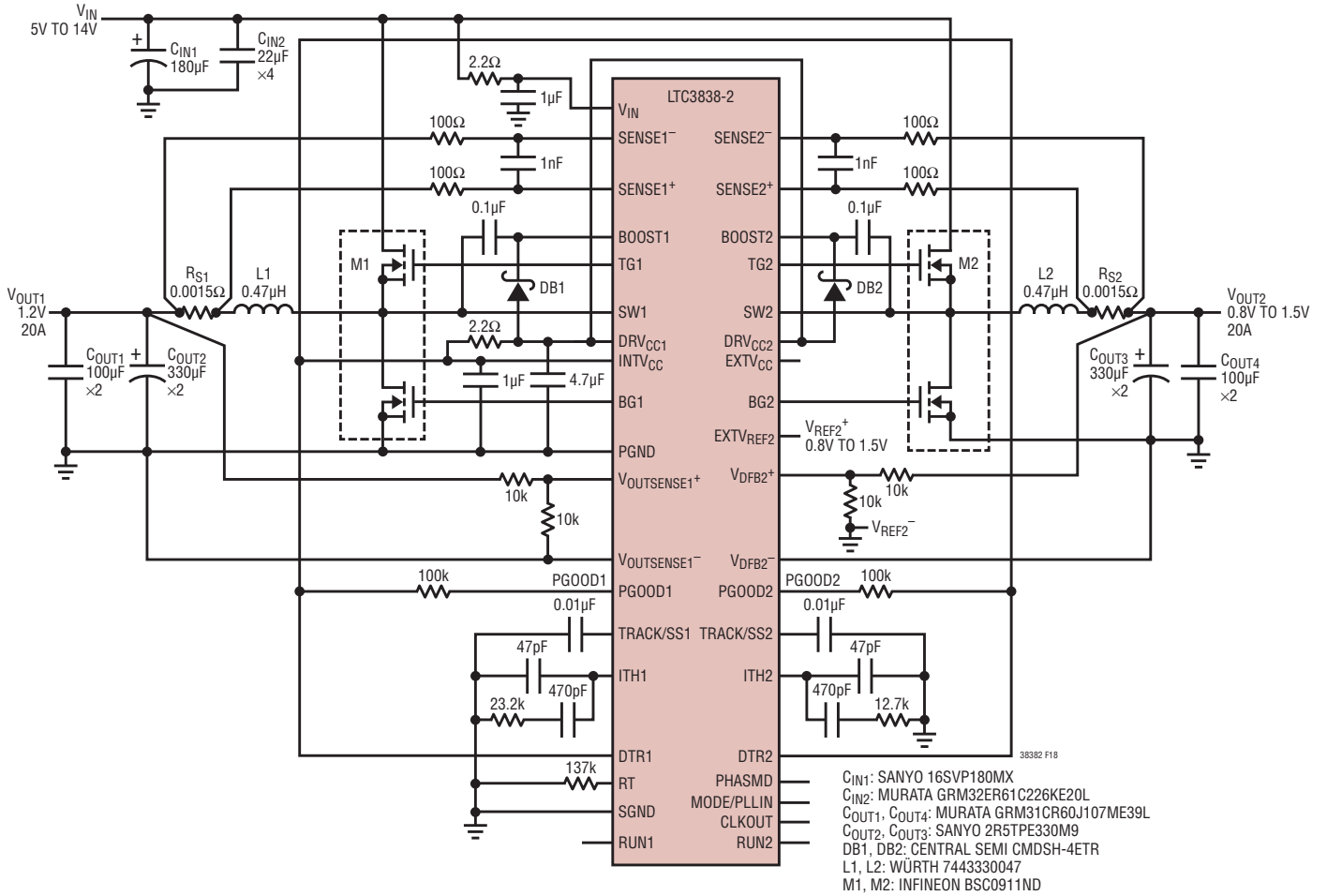
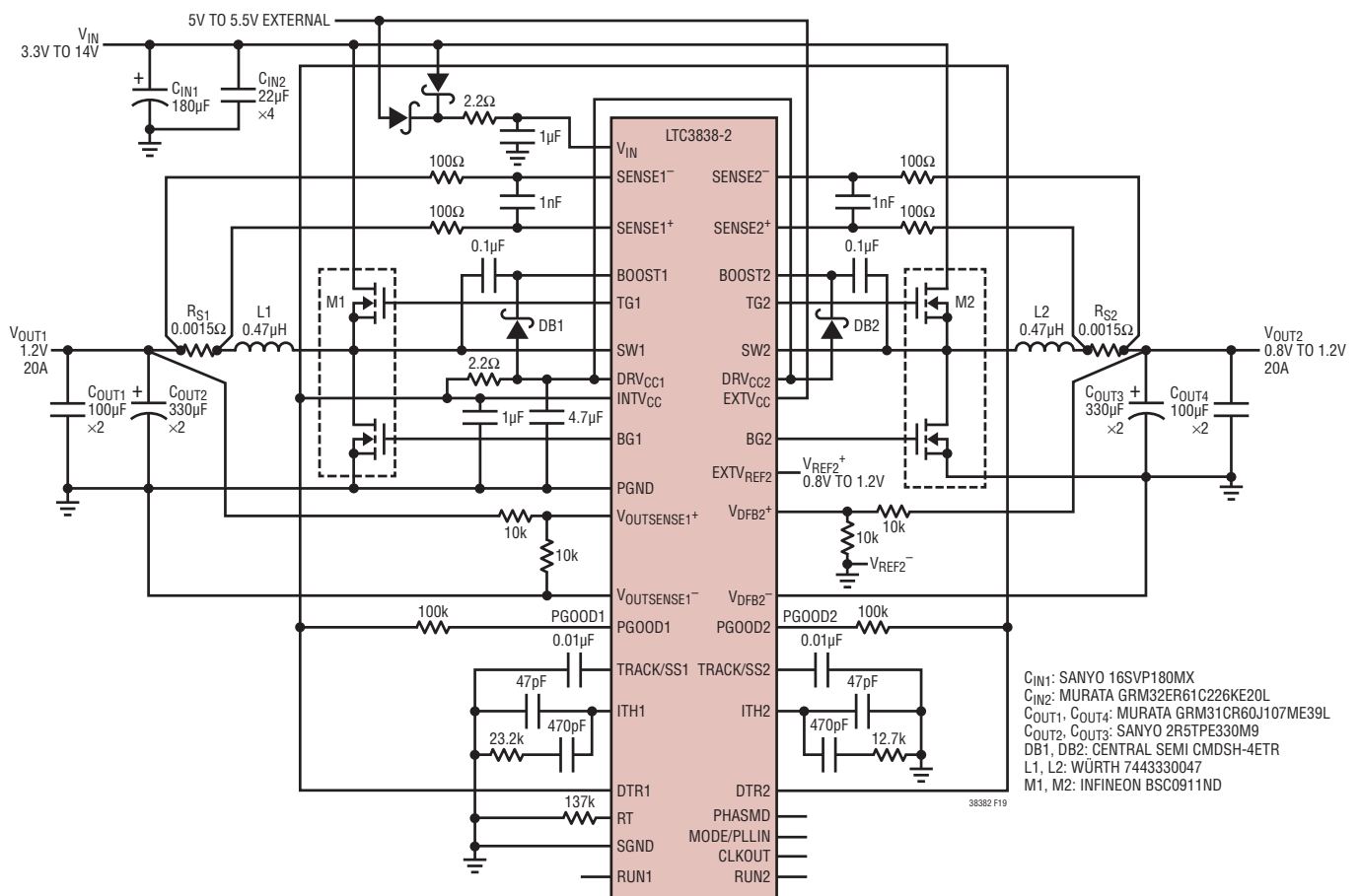


Figure 18. 5V to 14V Input, 1.2V/20A and 0.8V to 1.5V/20A ( $V_{OUT2}: EXT_{VREF2} = 1:1$ ) Dual Output, 300kHz,  $R_{SENSE}$ , Step-Down Converter

## TYPICAL APPLICATIONS

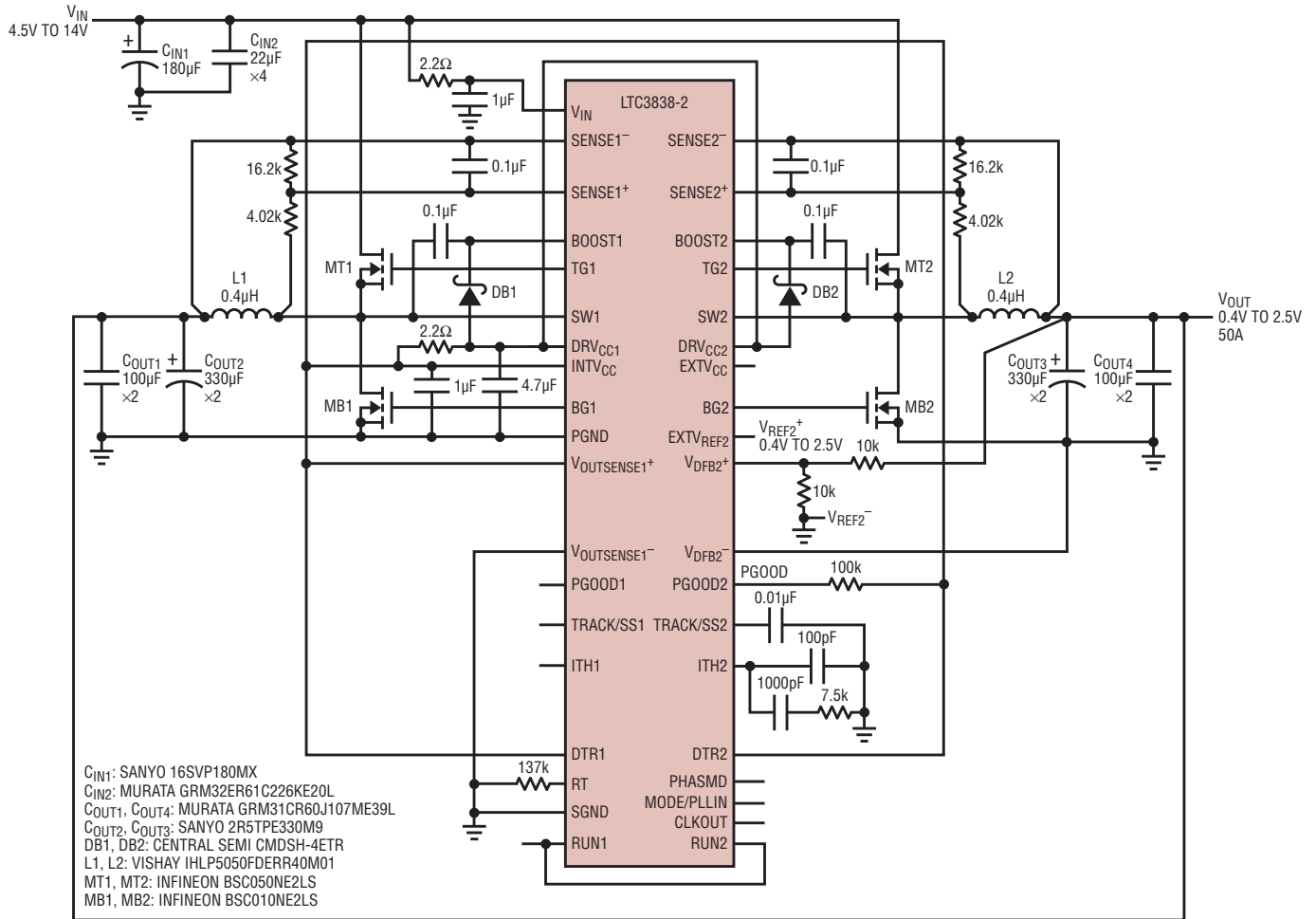


**Note:** When operating with the power  $V_{IN}$  supply below 5.5V, this application requires the 5V to 5.5V external supply to be present at  $EXTV_{CC}$  in order to maintain  $DRV_{CC}$ ,  $INTV_{CC}$  and  $V_{IN}$  pin voltages needed for the IC to function properly. The  $EXTV_{CC}$  supply is optional when the power  $V_{IN}$  supply is at or above 5.5V.

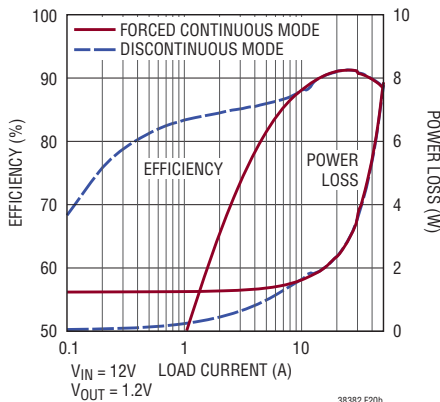
Power input voltage range of this application cannot be generalized for other frequency and/or output voltage. Each application that needs a power input voltage different from the  $V_{IN}$  pin voltage shall be tested individually for margin of range in which the switching nodes (SW1, SW2) phase-lock to the clock output (CLKOUT)

**Figure 19. 3.3V to 14V Power Input, 1.2V/20A and 0.8V to 1.2V/20A ( $V_{OUT2}$ :  $EXTV_{REF2}$  = 1:1) Dual Output, 300kHz,  $R_{SENSE}$ , Step-Down Converter (with Externally-Available 5V to 5.5V Supply)**

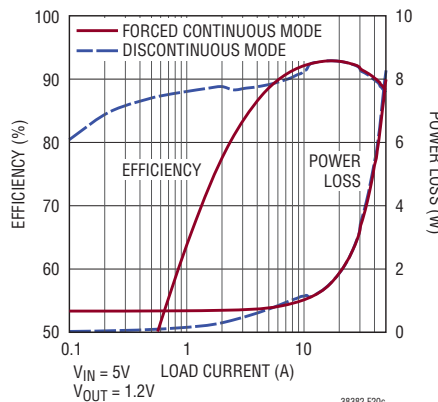
## TYPICAL APPLICATIONS



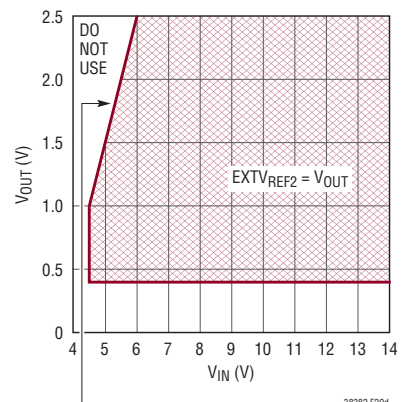
38382 F20a



38382 F20b



38382 F20c



38382 F20d

**Figure 20. 4.5V to 14V Input, 0.4V to 2.5V/50A ( $V_{OUT} : EXTV_{REF2} = 1:1$ ) 2-Phase Single Output, 300kHz, DCR Sense, Step-Down Converter**

# TYPICAL APPLICATIONS

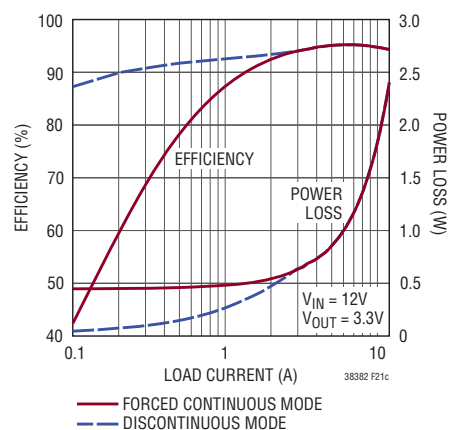
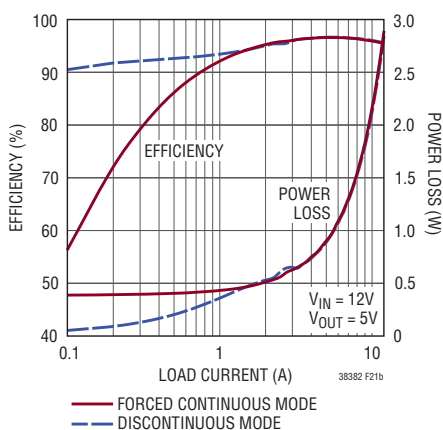
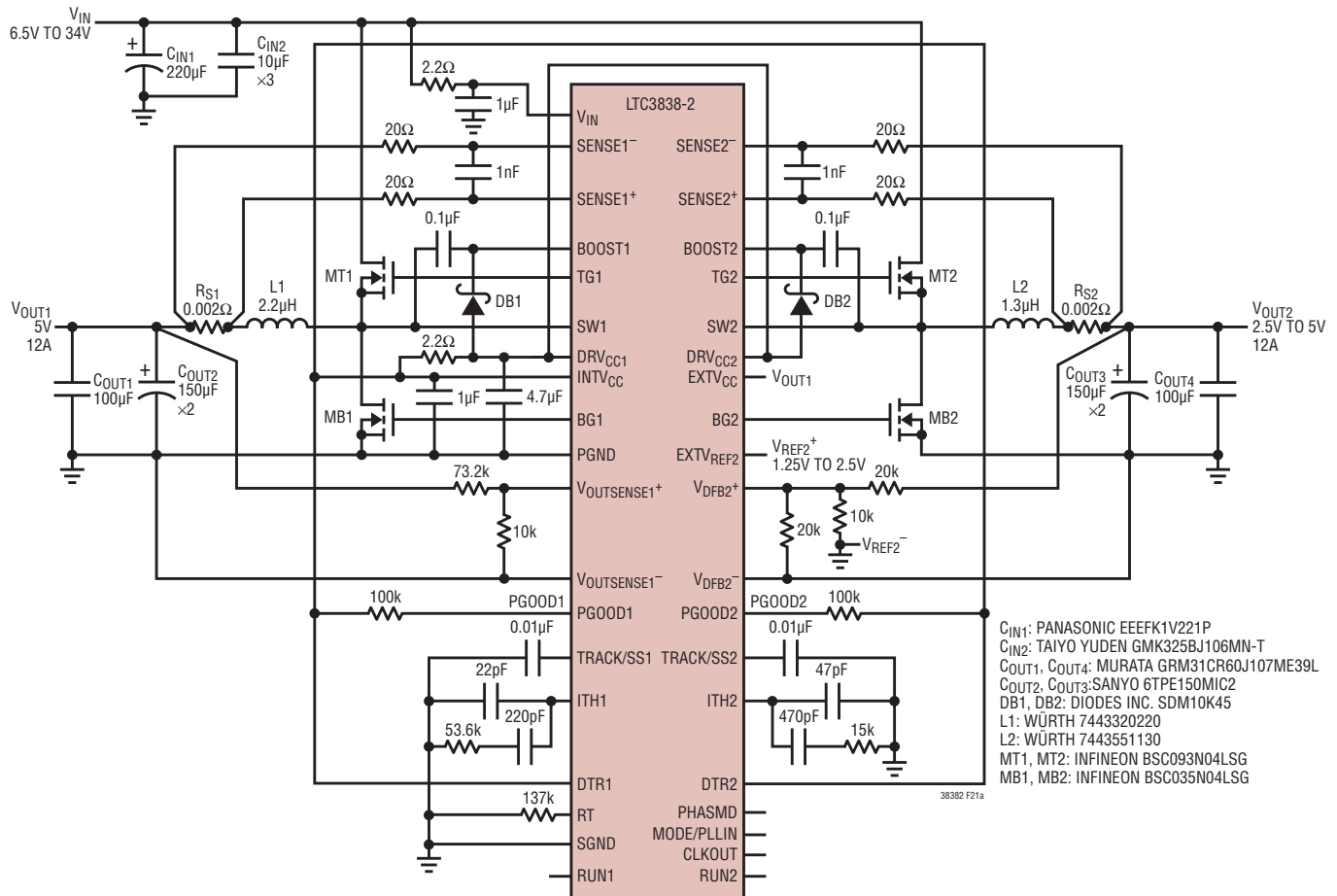
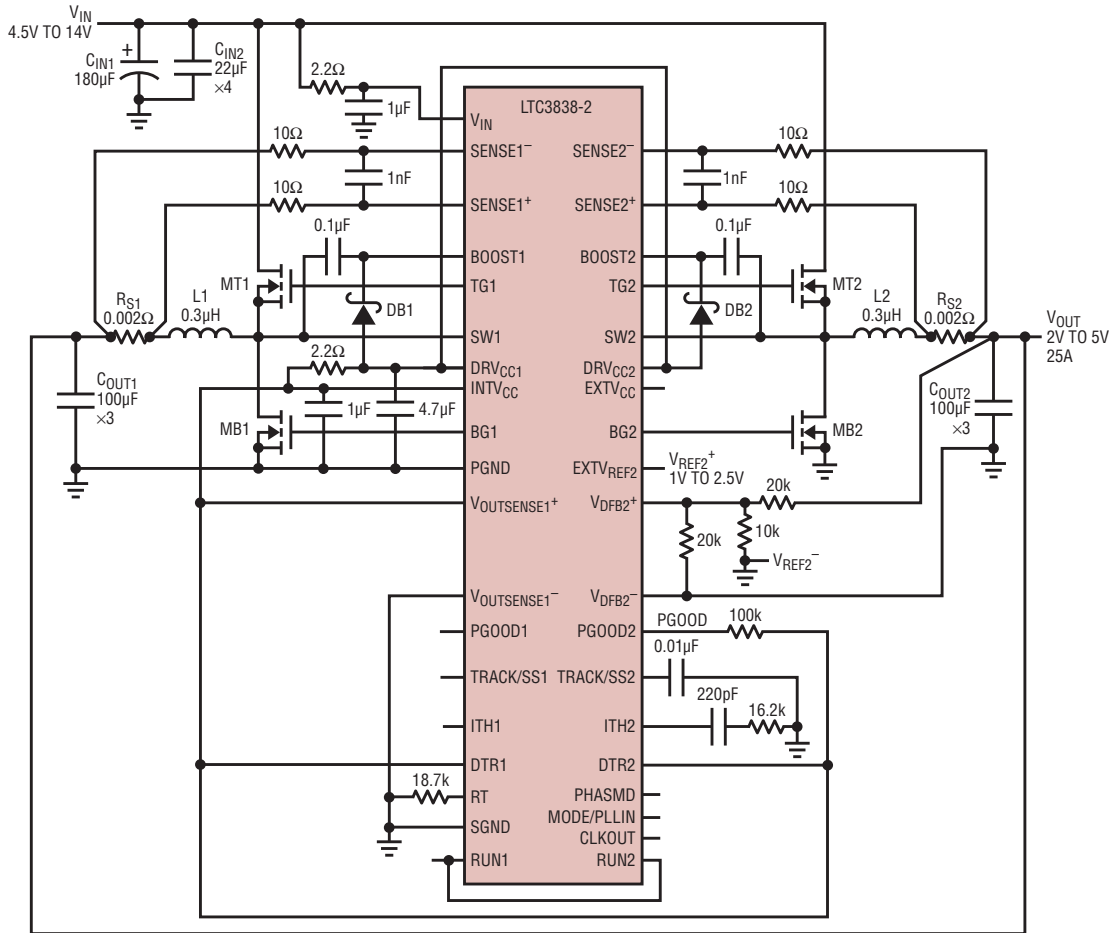


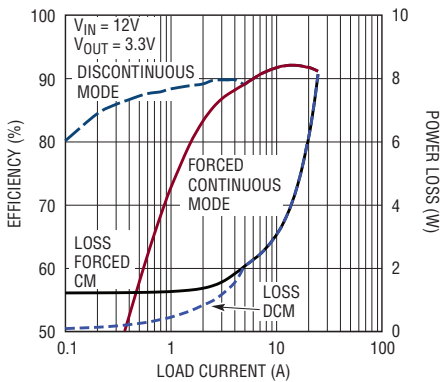
Figure 21. 6.5V to 34V Input, 5V/12A and 2.5V to 5V/12A ( $V_{OUT2}: EXT_{REF2} = 2:1$ )/12A Dual Output, 300kHz,  $R_{SENSE}$ , 5V Output Tied to  $EXT_{VCC}$ , Step-Down Converter

## TYPICAL APPLICATIONS

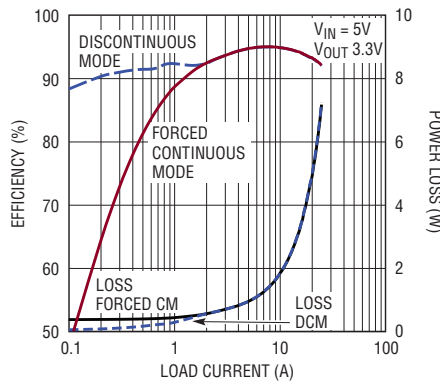


CIN1: SANYO 16SVP180MX  
 CIN2: MURATA GRM32ER61C226KE20L  
 COUT1, COUT2: MURATA GRM31CR60J107ME39L  
 DB1, DB2: CENTRAL CMDSH-3  
 MT1, MT2: INFINEON BSC050NE2LS  
 MB1, MB2: INFINEON BSC032NE2LS  
 L1, L2: WÜRTH 7443340030/WÜRTH 7443340047

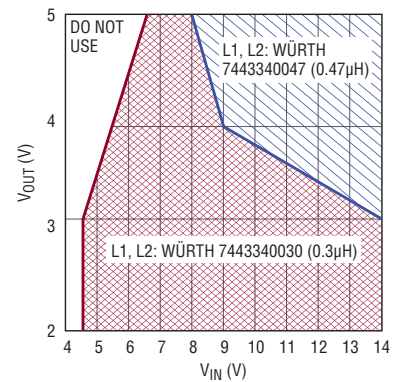
38382 F22a



38382 F22b



38382 F22c



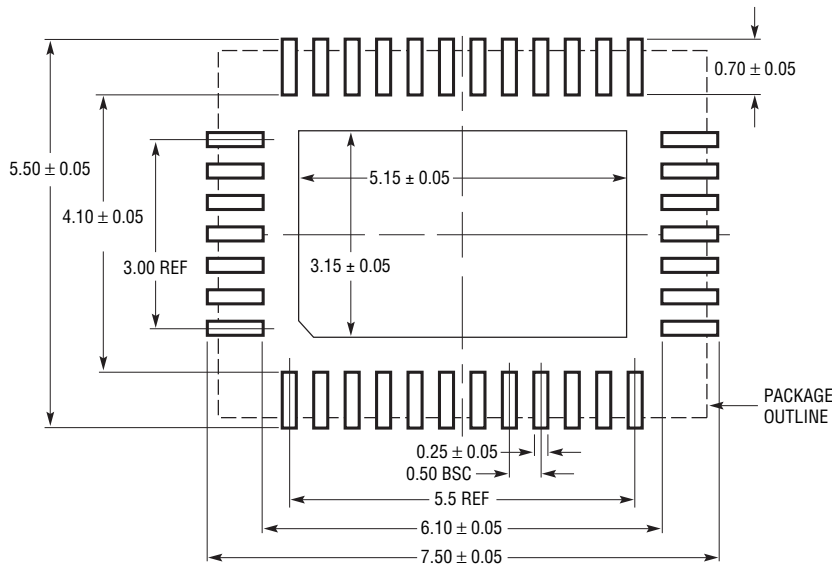
38382 F22d

Figure 22. 4.5V to 14V Input, 2V to 5V/25A ( $V_{OUT2}$ :  $EXTV_{REF2} = 2:1$ ) Output, 2MHz,  $R_{SENSE}$ , Step-Down Converter

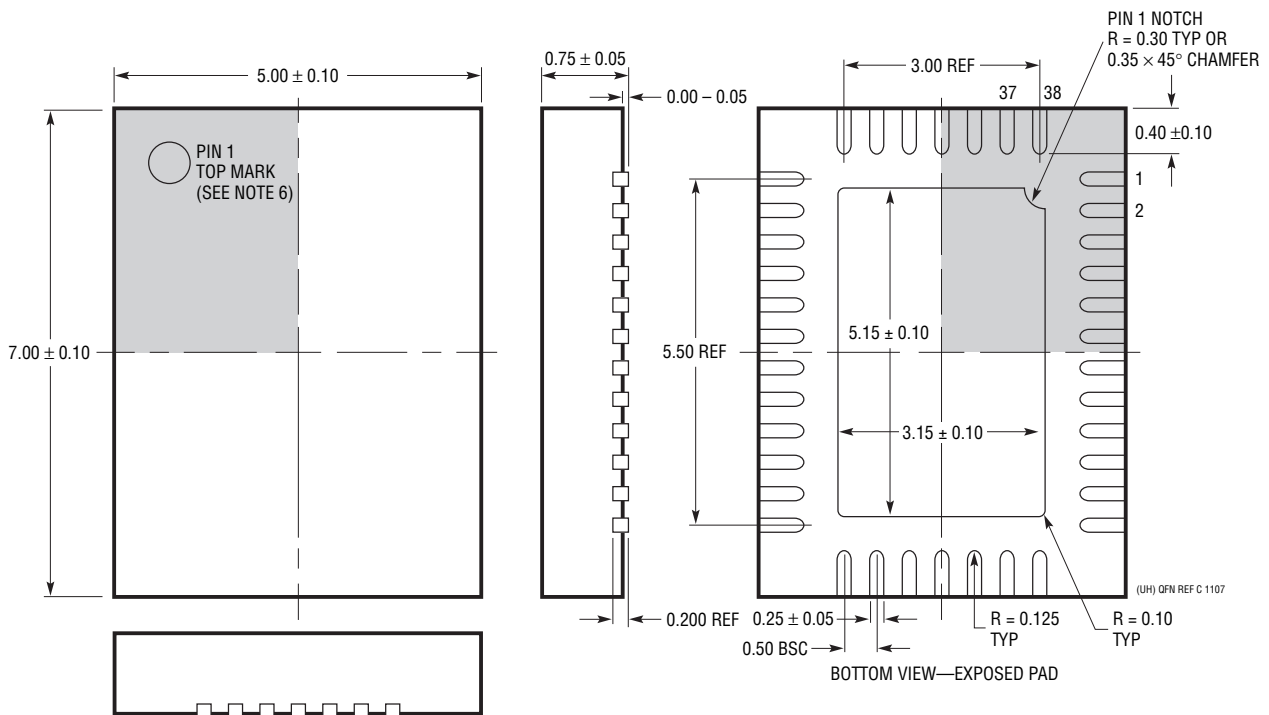
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**UHF Package**  
**38-Lead Plastic QFN (5mm × 7mm)**  
 (Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



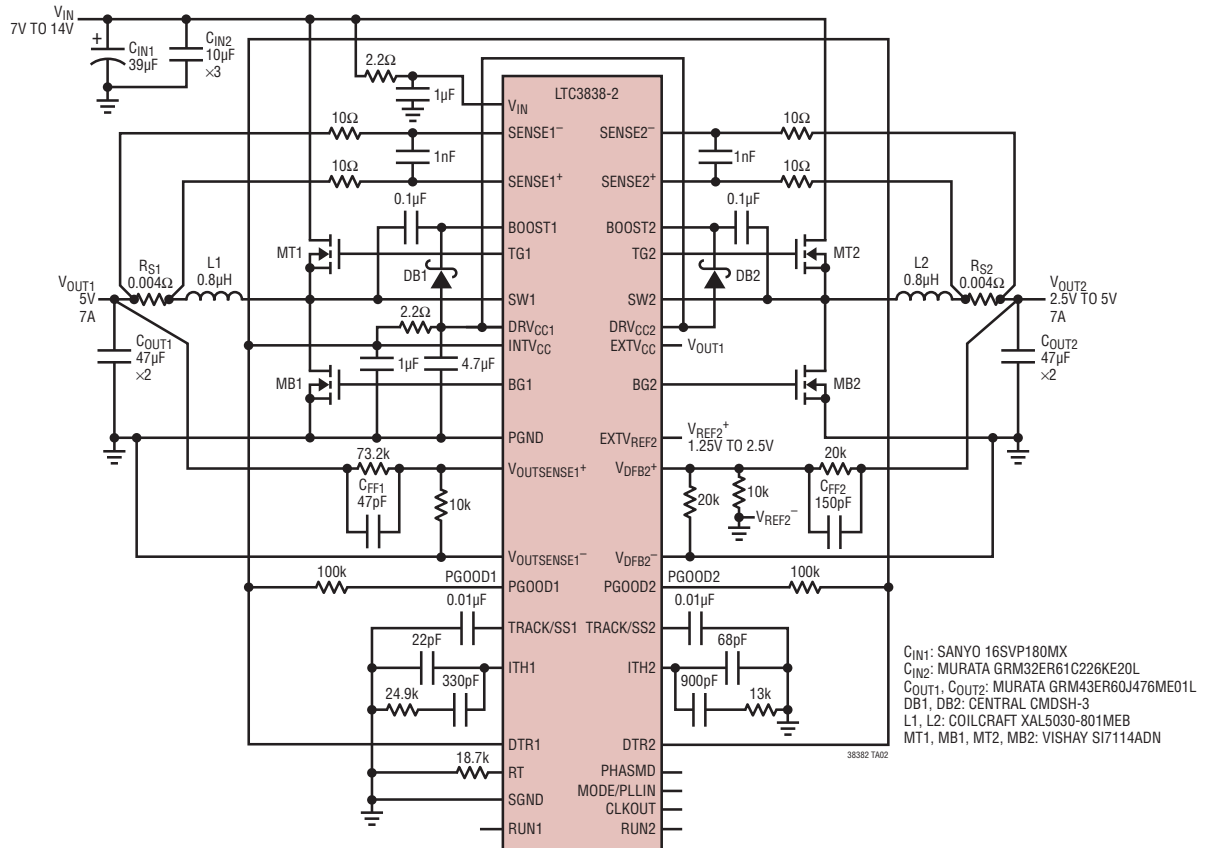
- NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# LTC3838-2

## TYPICAL APPLICATION

7V to 14V Input, 5V/5A and 2.5V to 5V/5A ( $V_{OUT2}: EXT_{VREF2} = 2:1$ )/5A Dual Output, 2MHz,  $R_{SENSE}$ , Step-Down Converter with  $EXT_{VCC}$  Tied to 5V Output



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3833	Fast Controlled On-Time, High Frequency Synchronous Step-Down Controller with Diff Amp	200kHz to 2MHz Operating Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 3mm x 4mm QFN-20, TSSOP-20
LTC3838/LTC3838-1	Dual or Single Output, 2-Channel Fast Controlled On-Time Synchronous Step-Down DC/DC Controller with Diff Amp(s)	200kHz to 2MHz Operating Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 5mm x 7mm QFN-38, TSSOP-38
LTC3839	Single-Output 2-Channel Fast Controlled On-Time Synchronous Step-Down Controller with Diff Amp	200kHz to 2MHz Operating Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 5mm x 5mm QFN-32
LTC3880/LTC3880-1	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	$I^2C$ /PMBus Interface with EEPROM and 16-Bit ADC, $V_{IN}$ Up to 24V, $0.5V \leq V_{OUT} \leq 5.5V$ , Analog Control Loop
LTC3869/LTC3869-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, with Accurate Current Sharing	PLL Fixed 250kHz to 750kHz Frequency, $4V \leq V_{IN} \leq 38V$ , $V_{OUT3}$ Up to 12.5V
LTC3855	Dual Output, 2-phase, Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	PLL Fixed Frequency 250kHz to 770kHz, $4.5V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 12V$
LTC3856	Single Output 2-Channel Synchronous Step-Down DC/DC Controller with Diff Amp and Up to 12-Phase Operation	PLL Fixed 250kHz to 770kHz Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 5V$
LTC3861/LTC3861-1	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and Three-State Output Drive	Operates with Power Blocks, DRMos Devices or External Drivers/MOSFETs, $3V \leq V_{IN} \leq 24V$ , $t_{ON(MIN)} = 20ns$
LTC3850/LTC3850-1 LTC3850-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, $R_{SENSE}$ or DCR Current Sensing	PLL Fixed 250kHz to 780kHz Frequency, $4V \leq V_{IN} \leq 30V$ , $0.8V \leq V_{OUT} \leq 5.25V$

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