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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74HC113

Dual J-K Flip-Flops (with Preset)



ADE-205-436 (Z)

1st. Edition

Sep. 2000

Description

This flip-flop is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, clock, and preset inputs and Q and \bar{Q} outputs. Preset is independent of the clock and accomplished by a low level on the input.

Features

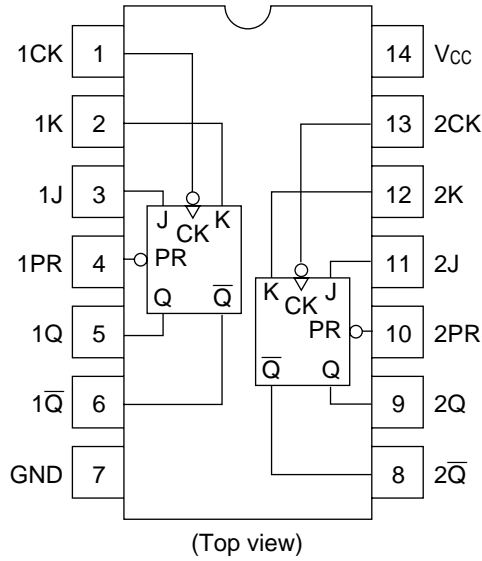
- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

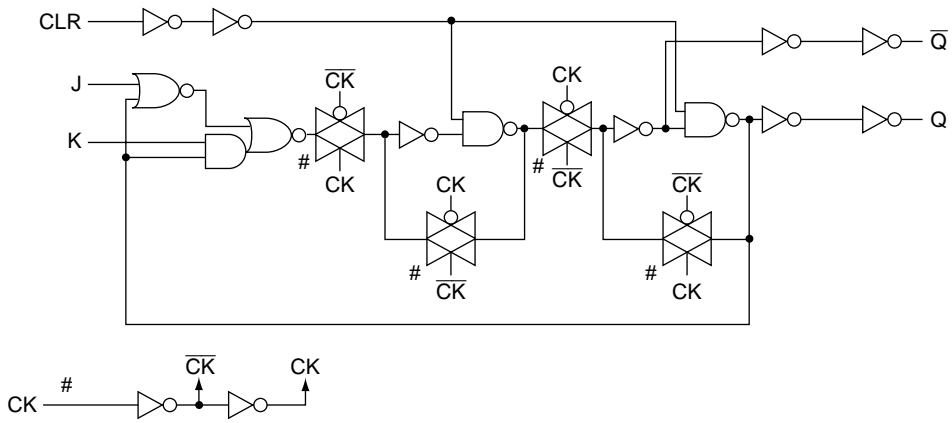
Inputs				Output	
Preset	Clock	J	K	Q	\bar{Q}
L	X	X	X	H	L
H		L	L	No change	
H		L	H	L	H
H		H	L	H	L
H		H	H	Toggle	
H	H	X	X	No change	
H	L	X	X	No change	
H		X	X	No change	

HD74HC113

Pin Arrangement



Logic Diagram (1/2)



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min			Max	
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

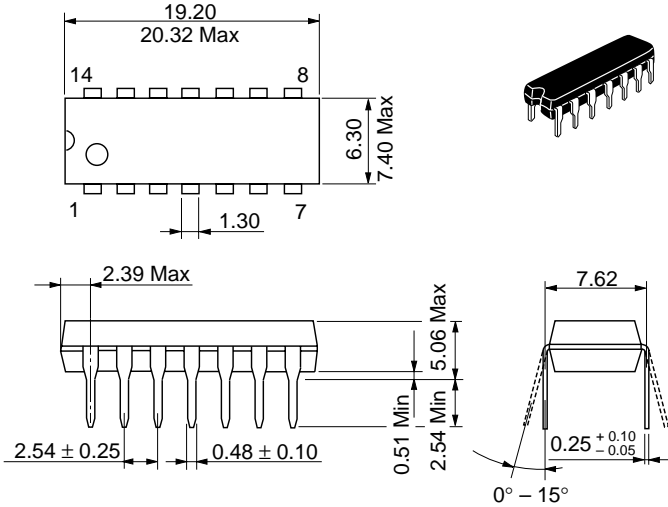
HD74HC113

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz		
		4.5	—	—	30	—	24			
		6.0	—	—	35	—	28			
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	Clock to Q or \bar{Q}	
		4.5	—	18	30	—	38			
	t_{PHL}	2.0	—	—	26	—	33		Preset to Q or \bar{Q}	
		4.5	—	17	28	—	35			
			6.0	—	—	24	—	30		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, Preset	
		4.5	16	8	—	20	—			
		6.0	14	—	—	17	—			
Setup time	t_{su}	2.0	100	—	—	125	—	ns	J or K to Clock	
		4.5	20	4	—	25	—			
		6.0	17	—	—	21	—			
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to J or K	
		4.5	5	-2	—	5	—			
		6.0	5	—	—	5	—			
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	Preset to Clock	
		4.5	20	-2	—	25	—			
		6.0	17	—	—	21	—			
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns		
		4.5	—	5	15	—	19			
	t_{THL}	6.0	—	—	13	—	16			
Input capacitance	C_{in}	—	—	5	10	—	10	pF		

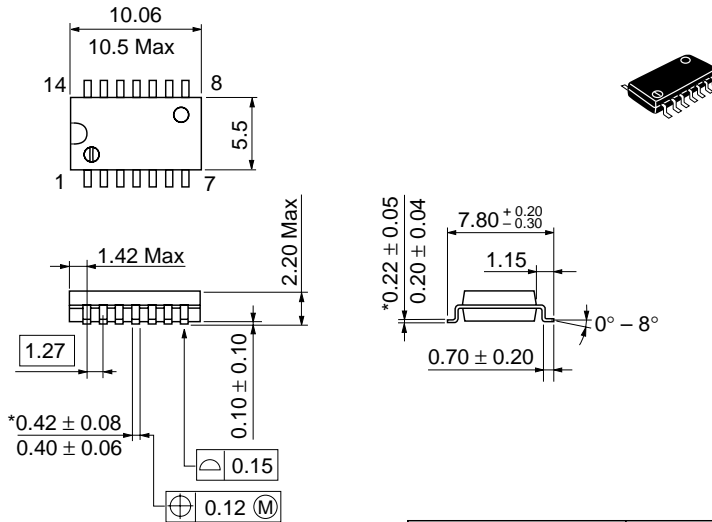
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

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