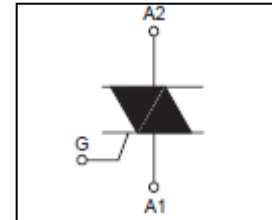


**Sensitive Gate
Bi-Directional Triode Thyristor**

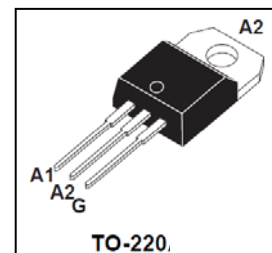
Features

- Repetitive Peak off-State Voltage: 600V
- R.M.S On-State Current($I_{T(RMS)}$)=12A
- Low on-state voltage: $V_{TM}=1.55V(\text{Max.})@ I_T=17A$
- High Commutation dV/dt .



General Description

General purpose swithing and phase control applications. These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.



Absolute Maximum Ratings ($T_J=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DRM}/V_{PRM}	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	600	V
$I_{T(RMS)}$	Forward Current RMS (All Conduction Angles, $T_J=58^{\circ}C$)	12	A
I_{TSM}	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	120/126	A
I^2t	Circuit Fusing Considerations ($t_p= 10\text{ ms}$)	100	A^2s
P_{GM}	Peak Gate Power — Forward, ($T_J = 58^{\circ}C$, Pulse with $\leq 1.0\mu s$)	5	W
$P_{G(AV)}$	Average Gate Power — Forward, (Over any 20ms period)	1	W
di/dt	Critical rate of rise of on-state current $I_{TM} = 20A; I_G = 200mA; di_G/dt = 200mA/\mu s$ $T_J=125^{\circ}C$	50	$A/\mu s$
I_{FGM}	Peak Gate Current — Forward, $T_J = 125^{\circ}C$ (20 μs , 120 PPS)	4	A
V_{RGM}	Peak Gate Voltage — Reverse, $T_J= 125^{\circ}C$ (20 μs , 120 PPS)	10	V
T_J	Junction Temperature	-40~125	$^{\circ}C$
T_{stg}	Storage Temperature	-40~150	$^{\circ}C$

Note1: Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may swiTh to the on-state. The rate of rise of current should not exceed 15A/ μs .

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	1.4	$^{\circ}C/W$
R_{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	60	$^{\circ}C/W$

WTPB12A60CW

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Characteristics	Min	Typ.	Max	Unit	
I _{DRM} /I _{RRM}	Peak Forward or Reverse Blocking Current (V _{DRM} =V _{RRM} .)	T _J =25°C	-	-	5	μA
		T _J =125°C	-	-	1	mA
V _{TM}	Forward "On" Voltage (Note2) (I _{TM} = 17A tp=380μs)	-	-	1.55	V	
I _{GT}	Gate Trigger Current (Continuous dc) (V _D = 12 Vdc, R _L = 33 Ω)	T2+G+	-	-	30	mA
		T2+G-	-	-	30	
		T2-G-	-	-	30	
V _{GT}	Gate Trigger Voltage (Continuous dc) (V _D =12 Vdc, R _L = 33 Ω)	T2+G+	-	-	1.2	V
		T2+G-	-	-	1.2	
		T2-G-	-	-	1.2	
V _{GD}	Gate threshold voltage(V _D = V _{DRM} ,R _L = 3.3 KΩ,T _J =125°C,)	0.2	-	-	V	
dV/dt	Critical rate of rise of commutation Voltage (V _D =0.67V _{DRM})	40	-	-	V/μs	
I _H	Holding Current (I _T = 500 mA) (Note 3)	-	-	25	mA	
I _L	Latching current (V _D =12 Vdc,I _{GT} =0.1A)	T2+G+	-	-	40	mA
		T2+G-	-	-	70	
		T2-G-	-	-	40	
R _d	Dynamic resistance	-	-	35	mΩ	

Note 2. Forward current applied for 1 ms maximum duration, duty cycle

Note 3. For both polarities of A2 to A1

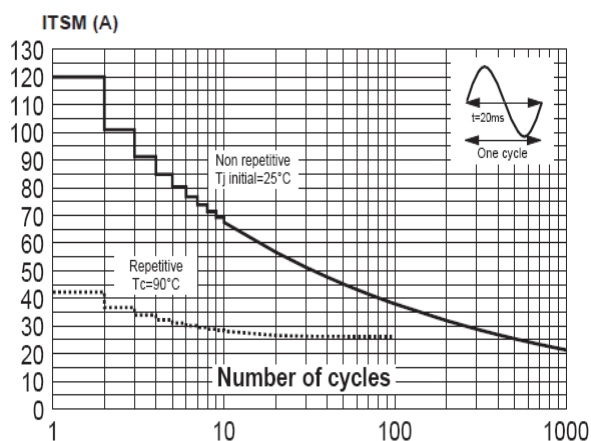


Fig.1 Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

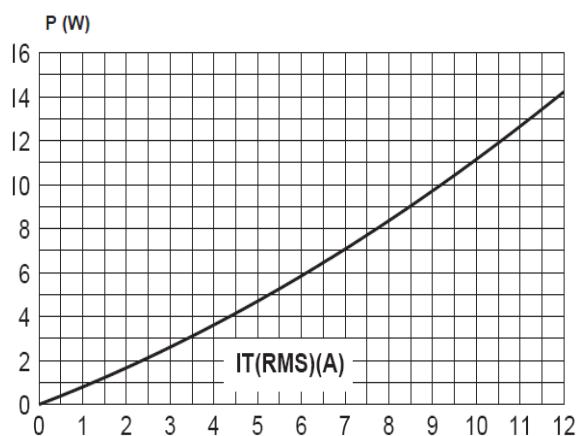


Fig.2 Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where $\alpha =$ conduction angle.

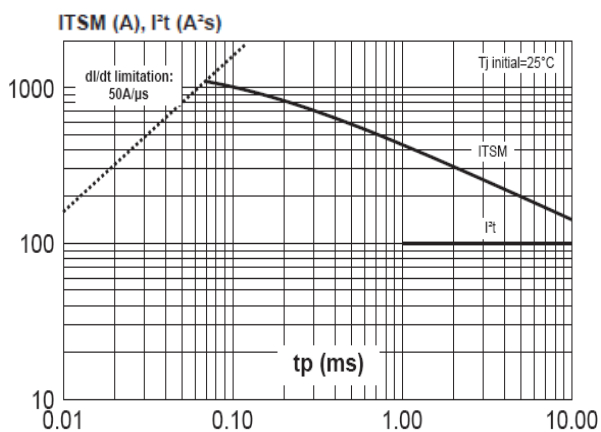


Fig.3 Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms, and corresponding value of I^2t .

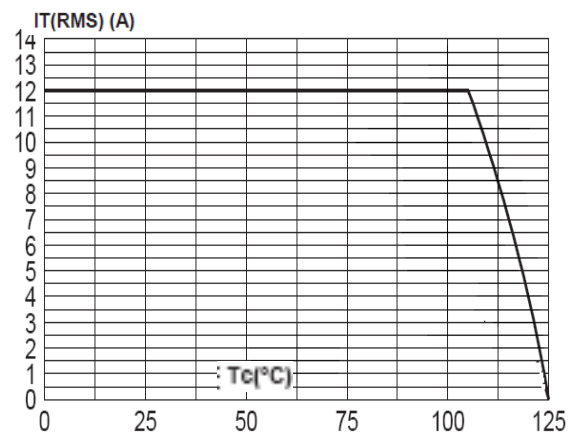


Fig.4 Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead} .

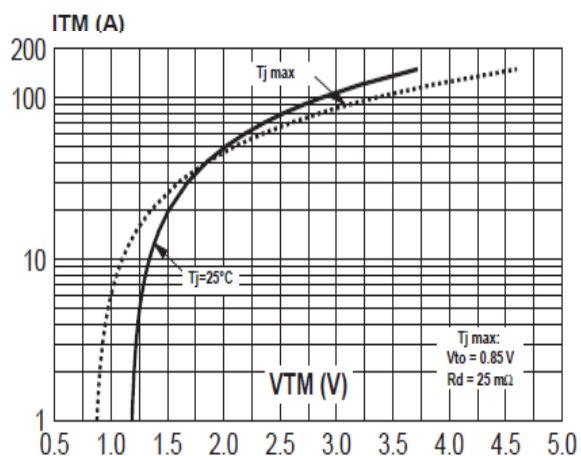


Fig.5 Typical and maximum on-state characteristic.

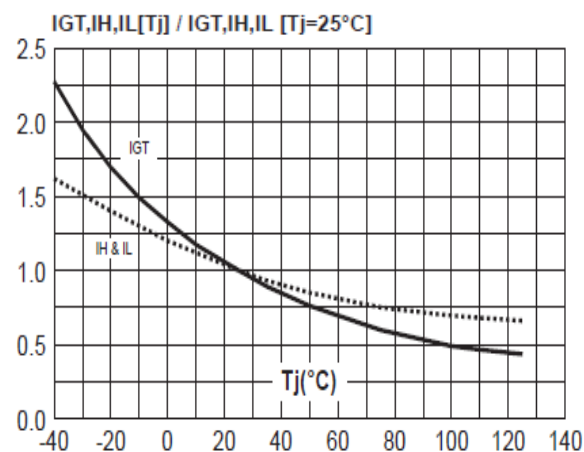


Fig.6 Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

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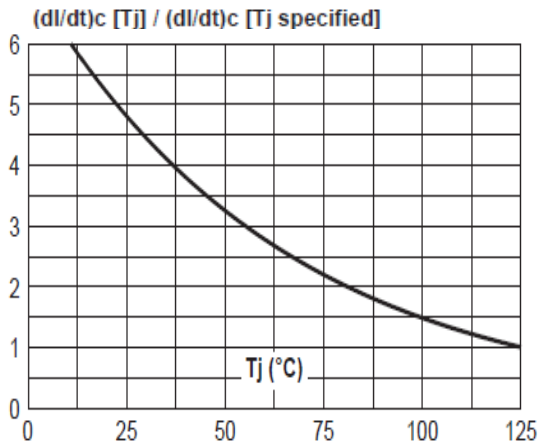


Fig.7 Relative variation of critical rate of decrease of main current versus junction temperature.

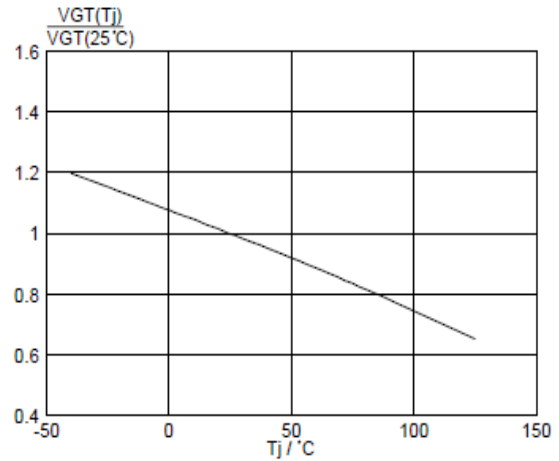


Fig.8 Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

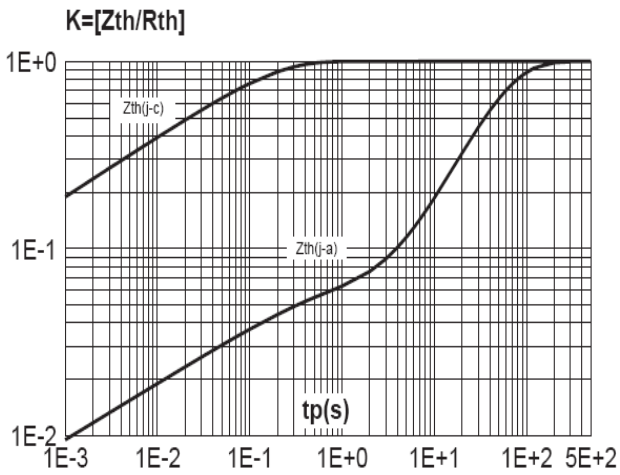


Fig.9 Transient thermal impedance $Z_{th-j-mb}$, versus pulse width t_p .

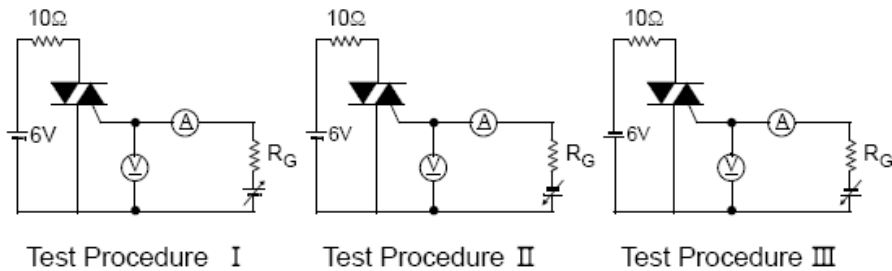


Fig.10 Gate Trigger Characteristics Test Circuit

TO-220 Package Dimension

