

**TOSHIBA**

TOSHIBA Original CMOS 8-Bit Microcontroller

**TLCS-870 Series**

**TMP87PS68DFG**

Not Recommended  
for New Design

**TOSHIBA CORPORATION**

Semiconductor Company

## Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

Example: TMPxxxxxF      TMPxxxxxFG

All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

Example: LQFP100-P-1414-0.50C      LQFP100-P-1414-0.50F

All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number
2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PS68DF	LQFP80-P-1212-0.50A	TMP87PS68DFG	LQFP80-P-1212-0.50F	—

\*: For the dimensions of the new package, see the attached Package Dimensions diagram.

### 3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

### 4. RESTRICTIONS ON PRODUCT USE

The following replaces the “RESTRICTIONS ON PRODUCT USE” on page 1 of body text.

#### RESTRICTIONS ON PRODUCT USE

20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

### 5. Publication date of the datasheet

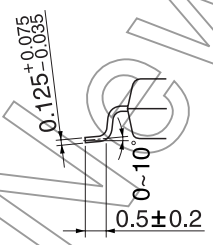
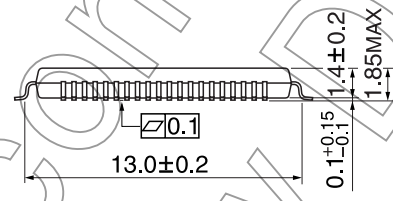
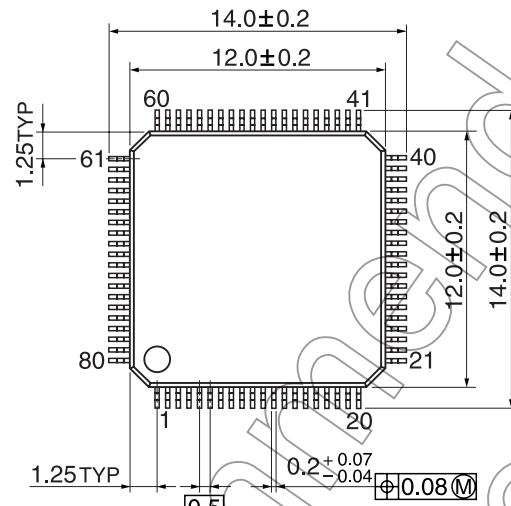
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

LQFP80-P-1212-0.50F

Unit: mm



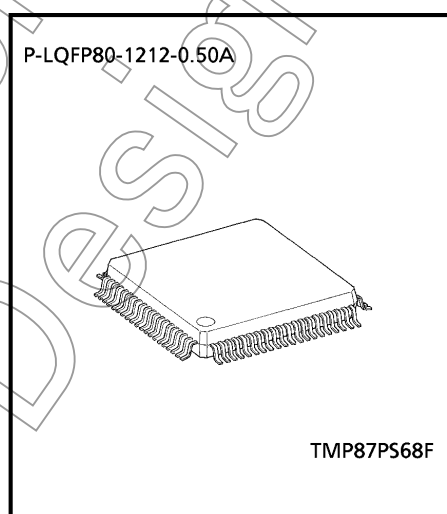
Not Recommended for New Design

## CMOS 8-Bit Microcontroller

**TMP87PS68DF**

The 87PS68 is a One-Time PROM microcontroller with low-power 480 K bits electrically programmable read only memory for the 87CS68 system evaluation. The 87PS68 is pin compatible with the 87CS68. The operations possible with the 87CS68 can be performed by writing programs to PROM. The 87PS68 can write and verify in the same way as the TC571000D using an adaptor socket BM11105 and an EPROM programmer.

Part No.	OTP	RAM	Package	OTP Adapter
TMP87PS68F	61184 bytes (60 Kbyte-256 byte)	2 K x 8-bit	P-LQFP80-1212-0.50A	BM11105

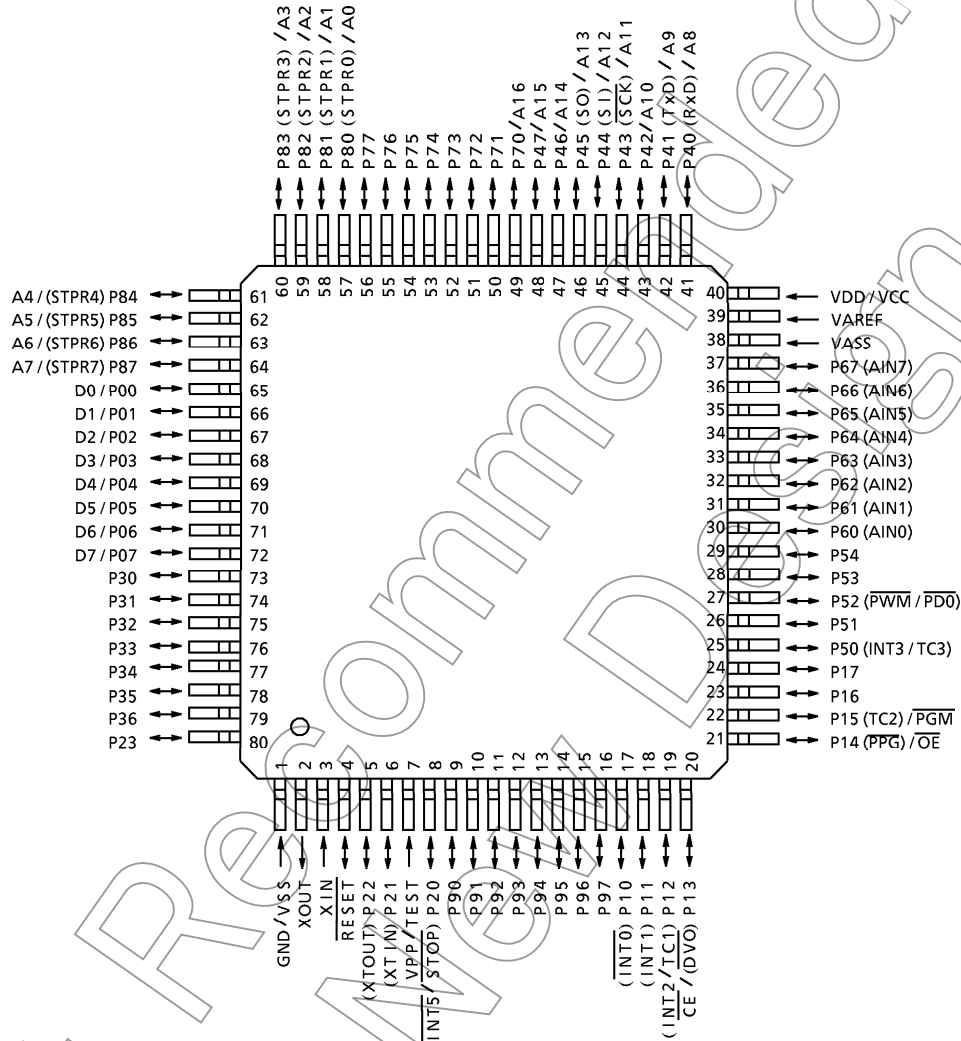


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Pin Assignments (Top View)

P-LQFP80-1212-0.50A



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**Pin Function**

The 87PS68 has two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87PS68 is pin compatible with the 87CS68 (fix the TEST pin at low level.)

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16	Input	PROM address inputs	P70
A15 to A8			P47 to P40
A7 to A0			P87 to P80
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
$\overline{PGM}$		Program mode signal input	P15
VPP	Power supply	+ 12.75 V / 5 V (Program supply voltage)	TEST
VCC		+ 6.25 V / 5 V	VDD
GND		0 V	VSS
P36 to P30	I/O	Pull-up with resistance for input processing.	
P54 to P50			
P67 to P60			
P77 to P72			
P11	I/O	PROM mode setting pin. Be fixed at high level.	
P21			
P71			
P17, P16, P12, P10, P22, P20			
RESET	I/O	PROM mode setting pin. Be fixed at low level.	
XIN			
XOUT	Output	Connect an 8MHz oscillator to stabilize the internal state.	
VAREF	Power supply		
VASS			

**Operational Description**

The following explains the 87PS68 hardware configuration and operation. The configuration and functions of the 87PS68 are the same as 87CS68, except in that a one-time PROM is used instead of an on-chip mask ROM.

The 87PS68 is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

**1. Operating Mode**

The 87PS68 has two modes: MCU and PROM.

**1.1 MCU Mode**

The MCU mode is activated by fixing the TEST / VPP pin at low level.

In the MCU mode, operation is the same as with the 87CS68 (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

**1.1.1 Program Memory**

The 87PS68 has a 60K × 8-bit (addresses 1100<sub>H</sub>-FFFF<sub>H</sub> in the MCU mode, addresses 11100<sub>H</sub>-1FFFF<sub>H</sub> in the PROM mode) of program memory (OTP).

When the 87PS68 is used as a system evaluation of the 87CS68, the data is written to the program storage area shown in Figure 1-1.

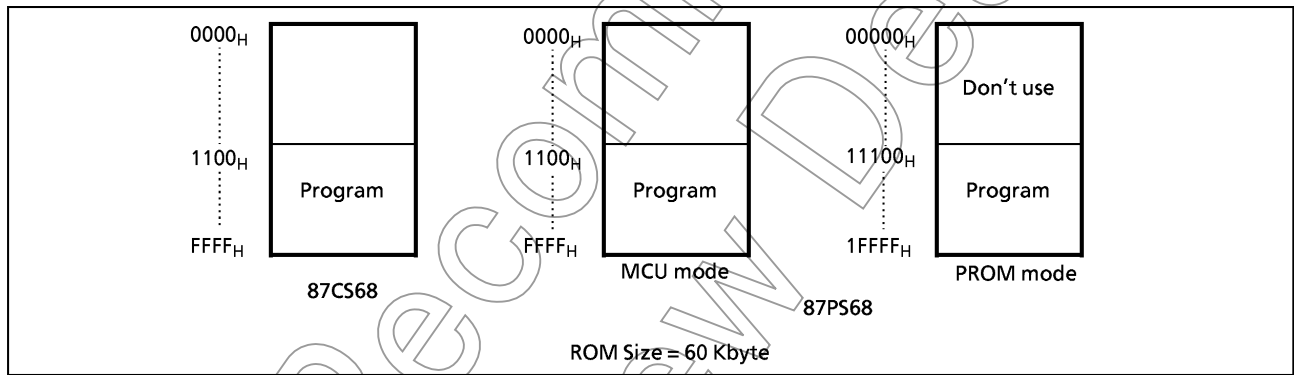


Figure 1.1 Program Memory Area

*Note : Either write the data FF<sub>H</sub> to the unused area or set the PROM programmer to access only the program storage area.*



### 1.1.2 Data Memory

The 87PS68 has an on-chip  $2K \times 8$ -bit data memory (static RAM).

### 1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the 87PS68 are the same as 87CS68 except that the TEST pin has no built-in pull-down resistance.

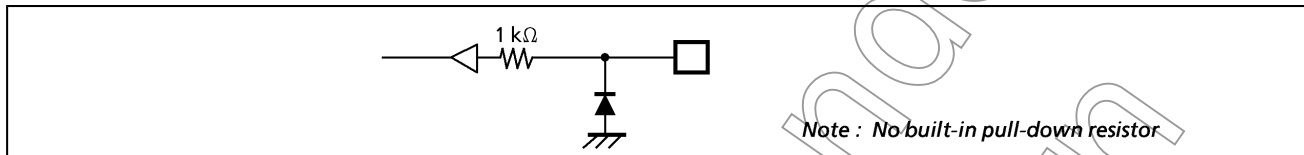


Figure 1-2. TEST pin

(2) I/O ports

The I/O circuits of 87PS68 I/O ports are the same I/O circuitries of the 87CS68.

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1.2 PROM Mode

The PROM mode is activated by setting the TEST,  $\overline{\text{RESET}}$  pin and the ports P17 to P10, P22 to P20 and P71, as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

*Note :* The high-speed programming mode can be used for program operation.  
 The 87PS68 is not supported an electric signature mode, so the ROM type must be set to TC571000D. (The settings may differ depending on the type of PROM programmer is use. Refer to the PROM programmer operation manual.

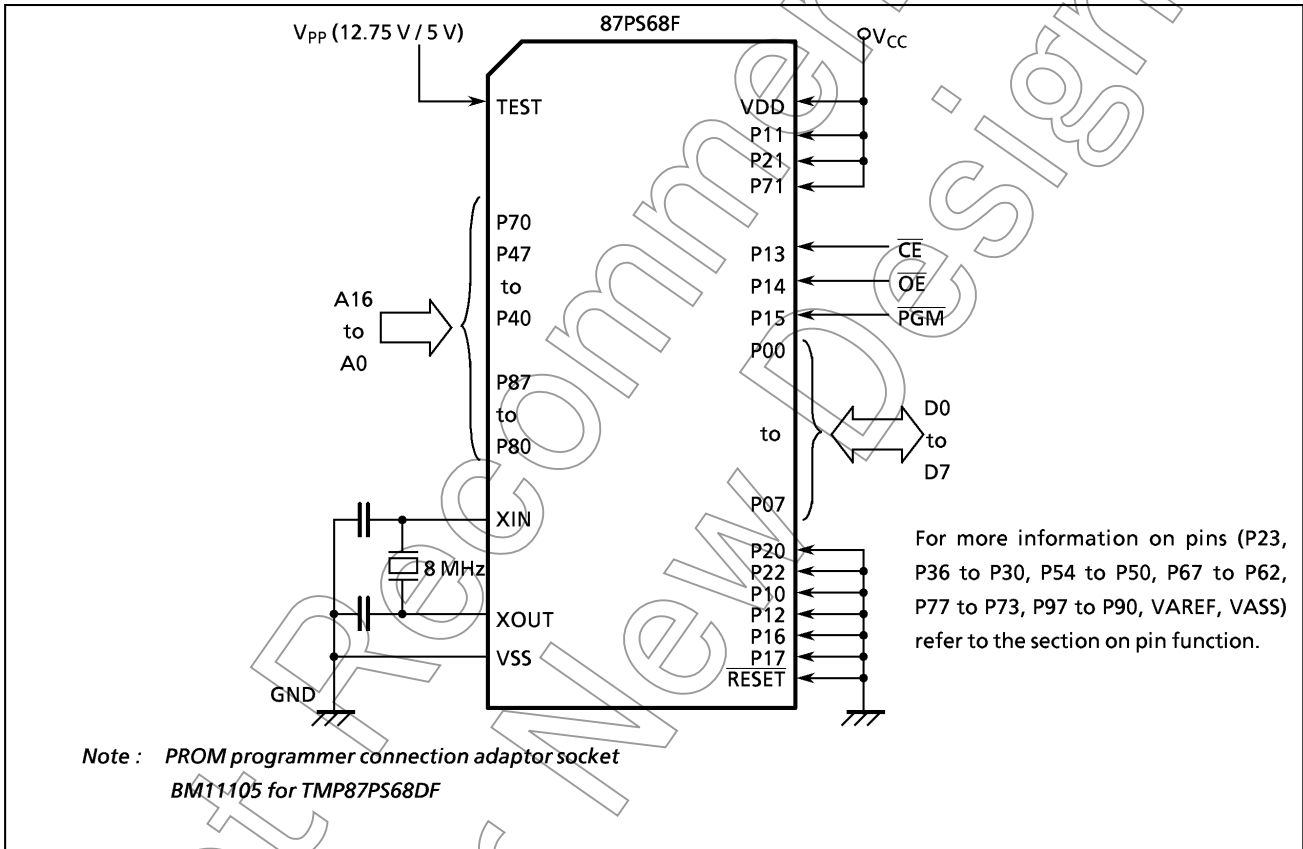


Figure 1-3. Setting for PROM Mode

**1.2.1 Programming Flowchart (High-speed Programming Mode)**

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the VPP pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the PGM input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

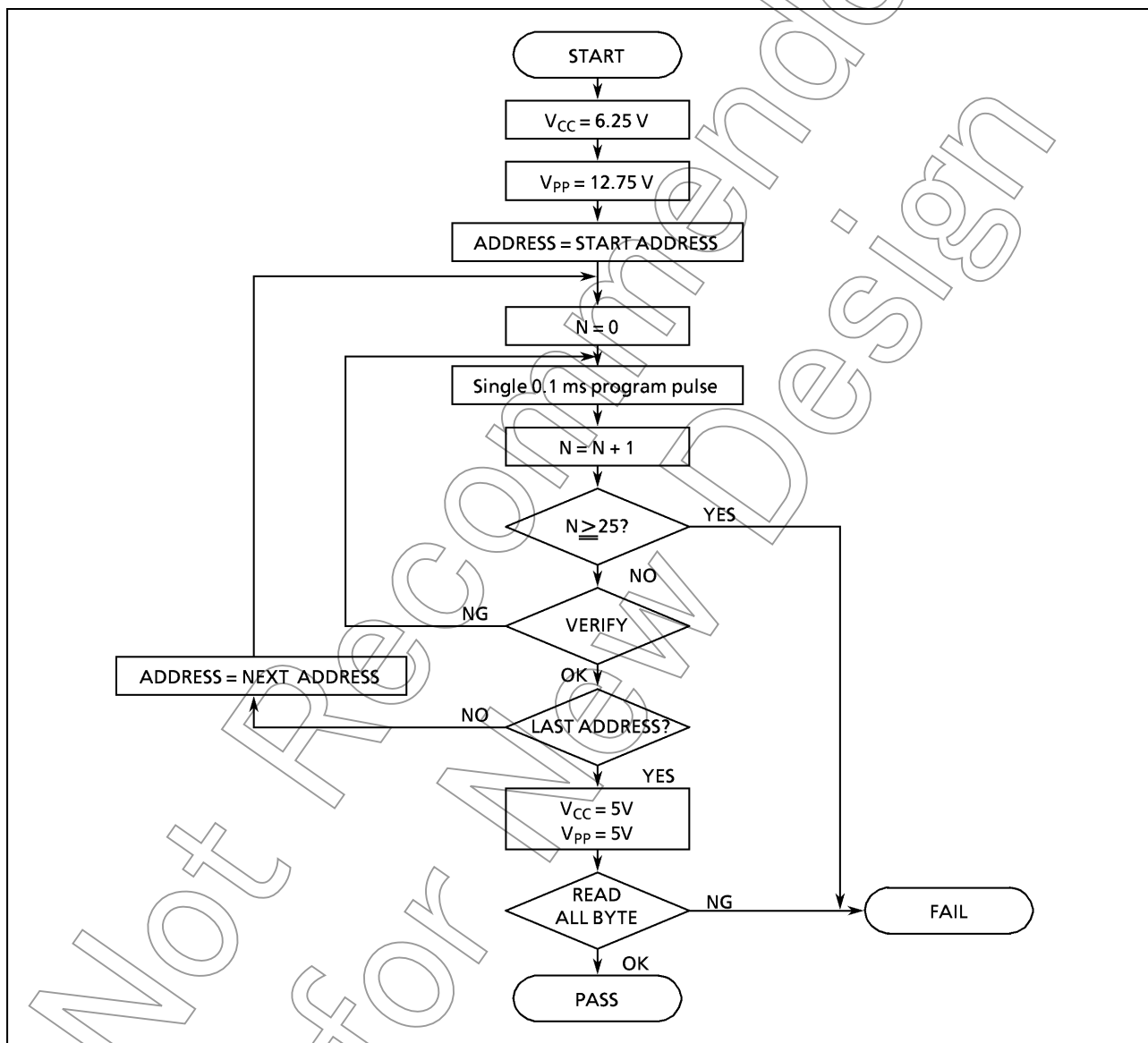


Figure 1-4. Flow Chart of High-speed Programming

## 1.2.2 Writing Method for General-purpose PROM Program

- (1) Adapters  
BM11105 : TMP87PS68DF
- (2) Adapter setting  
Switch (SW1) is set to side N.
- (3) PROM programmer specifying
  - i) PROM type is specified to TC571000D.  
Writing voltage: 12.75 V (high-speed program mode)
  - ii) Data transfer (copy) (note 1)  
In the TMP87PS68, EPROM is within the addresses 11100<sub>H</sub> to 1FFFF<sub>H</sub>. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.  
  
Ex. In the block transfer (copy) mode, executed as below.  
ROM capacity of 60KB : transferred addresses 01100<sub>H</sub> to 0FFFF<sub>H</sub> to addresses 11100 to 1FFFF<sub>H</sub>
  - iii) Writing address is specified. (note 1)  
Start address : 11100<sub>H</sub>  
End address : 1FFFF<sub>H</sub>
- (4) Writing  
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

*Note 1 : The specifying method is referred to the PROM programmer description. Either write the data FF<sub>H</sub> to the unused area or set the PROM programmer to access only the program storage area.*

*Note 2 : When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.*

*Note 3 : The TMP87PS68 does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.*

Input / Output Circuitry

(1) Control pins

The input / output circuitries of the 87PS68 control pins are shown below.

Control Pin	I/O	Input / Output Circuitry and Code	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency)  $R_f = 1.2\text{ M}\Omega$ (typ.) $R_o = 1.5\text{ k}\Omega$ (typ.)
XTIN (P21) XTOUT (P22)	Input Output	NM1 Refer to port P2 NM2 	Resonator connecting pins (low-frequency)  $R_f = 6\text{ M}\Omega$ (typ.) $R_o = 220\text{ k}\Omega$ (typ.)  In only dual-clock mode
RESET	I/O		Sink open drain output Hysteresis input Pull-up resistor  $R_{IN} = 220\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)
STOP/INT5 (P20)	Input		Hysteresis input  $R = 1\text{ k}\Omega$ (typ.)
TEST	Input		$R = 1\text{ k}\Omega$ (typ.)

Note1 : The TEST pin of the 87PS68 does not have a pull-down resistor. Be sure to fix the TEST pin to low in MCU mode.

Note2 : The 87PS68 is placed in the single-clock mode during reset. (NM1)

(2) Input/output ports

The input/output circuitries of the 87PS68 input/output ports are shown below.

Port	I/O	Input/Output Circuitry	Remarks
P0 P6	I/O	<p>initial "Hi-Z"</p>	<p>Tri-state I/O</p> <p>R = 1kΩ (typ.)</p>
P1	I/O	<p>initial "Hi-Z"</p>	<p>Tri-state I/O</p> <p>Hysteresis input</p> <p>R = 1kΩ (typ.)</p>
P2	I/O	<p>P20, P23</p> <p>initial "Hi-Z"</p>	<p>Sink open drain output</p> <p>Hysteresis input</p> <p>R = 1kΩ (typ.)</p>
		<p>P21, P22</p> <p>initial "Hi-Z"</p>	
P3	I/O	<p>initial "Hi-Z"</p>	<p>Sink open drain output</p> <p>High current output</p> <p>R = 1kΩ (typ.)</p>
P4 P5	I/O	<p>initial "Hi-Z"</p> <p>p-ch Control</p>	<p>Sink open drain</p> <p>or</p> <p>Tri-state I/O</p> <p>(Programmable port option)</p> <p>Hysteresis input</p> <p>R = 1kΩ (typ.)</p>
P7 P9	I/O	<p>initial "Hi-Z"</p> <p>p-ch Control</p>	<p>Sink open drain</p> <p>or</p> <p>Tri-state I/O</p> <p>(Programmable port option)</p> <p>R = 1kΩ (typ.)</p>
P8	I/O	<p>initial "Hi-Z"</p>	<p>Tri-state I/O</p> <p>Programmable</p> <p>Pull-up resistor</p> <p>R<sub>IN</sub> = 70kΩ (typ.)</p> <p>R = 1kΩ (typ.)</p> <p>Hysteresis input</p>

Electrical Characteristics

(1) 87PS68

Absolute Maximum Ratings (V<sub>SS</sub> = 0 V )

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	V
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Output Current (Per 1 pin)	I <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9	3.2	mA
	I <sub>OUT2</sub>	Port P3	30	
Output Current (Total)	Σ I <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9	160	mA
	Σ I <sub>OUT2</sub>	Port P3	120	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	T <sub>sld</sub>		260 (10s)	°C
Storage Temperature	T <sub>stg</sub>		- 55 to 125	°C
Operating Temperature	Topr		- 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V<sub>SS</sub> = 0 V, Topr = - 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit	
Supply Voltage	V <sub>DD</sub>		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc ≤ 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode	2.0		
				SLEEP mode			
STOP mode							
Input High Voltage	V <sub>IH1</sub>	Except hysteresis input	V <sub>DD</sub> ≥ 4.5 V	V <sub>DD</sub> × 0.70	V <sub>DD</sub>	V	
	V <sub>IH2</sub>	Hysteresis input		V <sub>DD</sub> × 0.75			
	V <sub>IH3</sub>			V <sub>DD</sub> < 4.5 V			V <sub>DD</sub> × 0.90
Input Low Voltage	V <sub>IL1</sub>	Except hysteresis input	V <sub>DD</sub> ≥ 4.5 V	0	V <sub>DD</sub> × 0.30	V	
	V <sub>IL2</sub>	Hysteresis input			V <sub>DD</sub> × 0.25		
	V <sub>IL3</sub>				V <sub>DD</sub> < 4.5 V		V <sub>DD</sub> × 0.10
Clock Frequency	fc	XIN, XOUT	V <sub>DD</sub> = 4.5 to 5.5 V	gear ratio	fc	8.0	MHz
					fc/2		
			V <sub>DD</sub> = 2.7 to 5.5 V	fc/4	4.19		
				fc/8			
	fs	XTIN, XTOUT			30.0	34.0	

Note 1: The recommended operating Conditions for a device are operating Conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating Conditions other than the recommended operating Conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating Conditions for the device are always adhered to.

Note2: Clock frequency fc: The supply voltage range of the conditions shows the value in NORMAL1, 2 modes and IDLE 1, 2 modes.

**D.C. Characteristics** ( $V_{SS} = 0\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit			
Hysteresis Voltage	$V_{HS}$	Hysteresis input		-	0.9	-	V			
Input Current	$I_{IN1}$	TEST	$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V}/0\text{ V}$	-	-	$\pm 2$	$\mu\text{A}$			
	$I_{IN2}$	Sink open drain port and tri-state port								
	$I_{IN3}$	RESET, STOP								
Input Resistance	$R_{IN2}$	RESET		100	220	450	$\text{k}\Omega$			
	$R_{IN}$	P8 pull-up resistor		30	70	150				
Output Leakage Current	$I_{LO}$	Sink open drain port and tri-state port	$V_{DD} = 5.5\text{ V}$ , $V_{OUT} = 5.5\text{ V}$	-	-	2	$\mu\text{A}$			
Output High Voltage	$V_{OH2}$	Tri-state port	$V_{DD} = 4.5\text{ V}$ , $I_{OH} = -0.7\text{ mA}$	4.1	-	-	V			
Output Low Voltage	$V_{OL}$	Except XOUT and P3	$V_{DD} = 4.5\text{ V}$ , $I_{OL} = 1.6\text{ mA}$	-	-	0.4	V			
Output Low Current	$I_{OL3}$	Port P3	$V_{DD} = 4.5\text{ V}$ , $V_{OL} = 1.0\text{ V}$	-	20	-	mA			
Supply Current in NORMAL 1, 2 mode	$I_{DD}$		$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.3\text{ V}/0.2\text{ V}$ $f_c = 8\text{ MHz}$ $f_s = 32.768\text{ kHz}$	-	9	12	mA			
Supply Currnt in IDLE 1, 2 mode								-	4.5	6.5
Supply Currnt in NORMAL 1, 2 mode								-	T.B.D	T.B.D
Supply Currnt in IDLE 1, 2 mode								-	T.B.D	T.B.D
Supply Current in SLOW mode	$I_{DD}$		$V_{DD} = 3.0\text{ V}$ $V_{IN} = 2.8\text{ V}/0.2\text{ V}$ $f_c = 4.2\text{ MHz}$ $f_s = 32.768\text{ kHz}$	-	30	60	$\mu\text{A}$			
Supply Current in SLEEP mode								-	15	30
Supply Current in STOP mode								-	0.5	10

Note 1: Typical values show those at  $T_{opr} = 25^{\circ}\text{C}$ ,  $V_{DD} = 5\text{V}$ .  
 Note 2: Input current: The current through pull-up or pull-down resistor is not included.

**A / D Conversion Characteristics** ( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	$V_{AREF}$	$V_{AREF} - V_{ASS} \geq 2.5\text{ V}$	2.7	-	$V_{DD}$	V
	$V_{ASS}$		$V_{SS}$	-	1.5	
Analog Input Voltage	$V_{AIN}$	$V_{DD} = V_{AREF} = 5.0\text{ V}$ $V_{SS} = V_{ASS} = 0.0\text{ V}$	$V_{ASS}$	-	$V_{AREF}$	V
Analog Supply Current	$I_{REF}$	$V_{AREF} = 5.5\text{ V}$ , $V_{ASS} = 0.0\text{ V}$	-	0.5	1.0	V
Nonlinearity Error		$V_{DD} = 2.7\text{ to }5.5\text{ V}$ $V_{SS} = 0.0\text{ V}$ $V_{AREF} = 2.700\text{ V}$ , $5.000\text{ V}$ $V_{ASS} = 0.000\text{ V}$	-	-	$\pm 1$	mA
Zero Point Error			-	-	$\pm 1$	
Full Scale Error			-	-	$\pm 1$	LSB
Total Error			-	-	$\pm 2$	

Note: Total Error = total number of each type error excluding quantization error



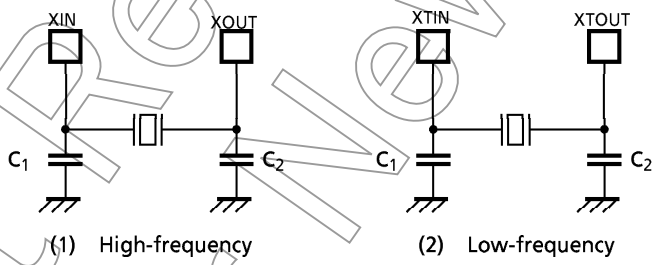
A.C. Characteristics

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 5.5 V, T<sub>opr</sub> = - 30 to 70 °C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t <sub>cy</sub>	In NORMAL1, 2 mode (gear ratio)	0.5 (1/1)	-	10 (1/8)	μs
		In IDLE1, 2 mode (gear ratio)				
		In SLOW mode	117.6		133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t <sub>wCH</sub>	For external clock operation (XIN input)	50	-	-	ns
Low Level Clock Pulse Width	t <sub>wCL</sub>	f <sub>c</sub> = 8 MHz				
High Level Clock Pulse Width	t <sub>wSH</sub>	For external clock operation (XTIN input)	14.7			μs
Low Level Clock Pulse Width	t <sub>wSL</sub>	f <sub>s</sub> = 32.768 kHz				

Recommended Oscillating Condition

Parameter	Oscillator	Frequency	Recommended Oscillator	Recommended Condition	
				C <sub>1</sub>	C <sub>2</sub>
High-frequency	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA KBR4.0MS		
			MURATA CSA4.00MG		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF



**Note:** When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations

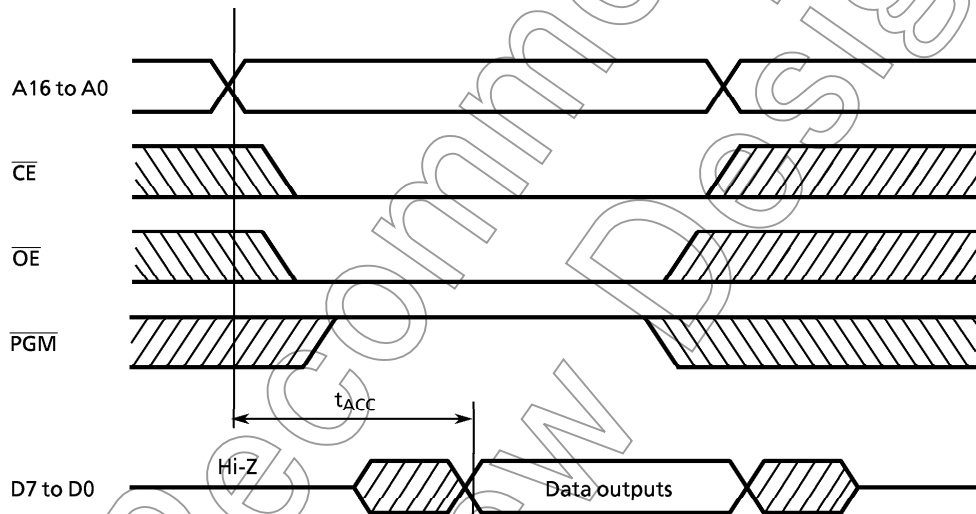
**Note:** To obtain an accurate oscillating frequency the condenser capacity must be adjusted on the sct.

D.C./A.C. Characteristics (PROM mode) ( $V_{SS} = 0\text{ V}$ )

(1) Read Operation

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	$V_{IH4}$		2.2	—	$V_{CC}$	V
Input Low Voltage	$V_{IL4}$		0	—	0.8	V
Power Supply Voltage	$V_{CC}$		4.75	5.0	5.25	V
Program Power Supply Voltage	$V_{PP}$					
Address Access Time	$t_{ACC}$	$V_{CC} = 5.0 \pm 0.25\text{ V}$	—	$1.5t_{cyc} + 300$	—	ns

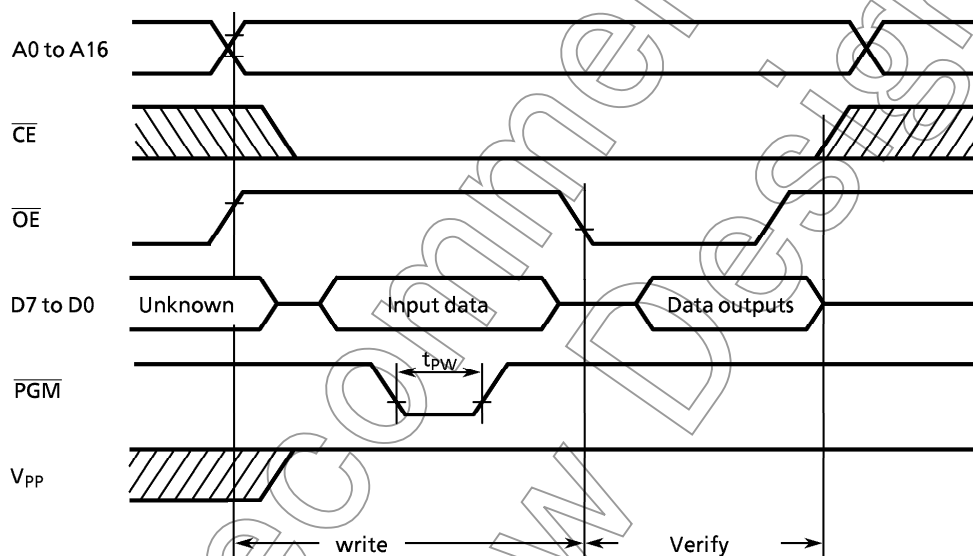
Note:  $t_{cyc} \approx 500\text{ ns}$  at 8 MHz



Not Recommended for New Design

(2) High-Speed Programming Operation ( $T_{opr} = 25 \pm 5 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	$V_{IH4}$		2.2	—	$V_{CC}$	V
Input Low Voltage	$V_{IL4}$		0	—	0.8	V
Power Supply Voltage	$V_{CC}$		6.0	6.25	6.5	V
Program Power Supply Voltage	$V_{PP}$		12.5	12.75	13.0	V
Initial Program Pulse Width	$t_{PW}$	$V_{CC} = 6.0 \text{ V}$	0.095	0.1	0.105	ms



**Note1:** When  $V_{CC}$  power supply is turned on or after,  $V_{PP}$  must be increased.  
 When  $V_{CC}$  power supply is turned off or before,  $V_{PP}$  must be increased.

**Note2:** The device must not be set to the EPROM programmer or picked up from it under applying the program voltage ( $12.5 \text{ V} \pm 0.5 \text{ V} = V$ ) to the  $V_{PP}$  pin as the device is damaged.

**Note3:** Be sure to execute the recommended programming mode with the recommended programming adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Not Recommended  
for New Design