

STL8NH3LL N-CHANNEL 30 V - 0.012 Ω - 8 A PowerFLAT™ ULTRA LOW GATE CHARGE STripFET™ MOSFET

Table 1: General Features

ТҮРЕ	V _{DSS}	R _{DS(on)}	I _D (2)
STL8NH3LL	30 V	< 0.015 Ω	8 A

- TYPICAL R_{DS}(on) = 0.012 Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE
- LOW THRESHOLD DEVICE

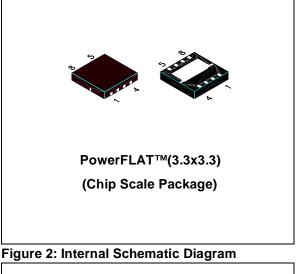
DESCRIPTION

This application specific MOSFET is the lastest generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

APPLICATIONS

CONTROL FET IN BUCK CONVERTER

Figure 1: Package



PRELIMINARY DATA

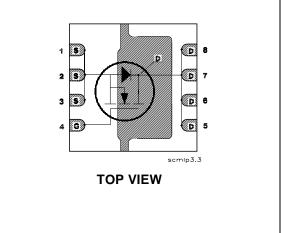


Table 2: Order Codes

Γ	Part Number	Marking	Package	Packaging
	STL8NH3LL	L8NH3LL	PowerFLAT™ (3.3x3.3)	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit	
V _{DS}	Drain-source Voltage (V _{GS} = 0) 30			
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V	
V _{GS}	Gate- source Voltage	± 16	V	
I _D (1)	Drain Current (continuous) at T _C = 25°C (Steady State) 8		А	
I _D (2)	Drain Current (continuous) at T _C = 100°C (Steady State)	5	А	
I _{DM} (3)	Drain Current (pulsed)	32	A	
P _{TOT} (1)	Total Dissipation at T _C = 25°C	50	W	
P _{TOT} (2)	Total Dissipation at T _C = 25°C (Steady State)	1.56		
	Derating Factor (2)	0.4 V		
T _{stg}	Storage Temperature	- 55 to 150		
Тj	Max. Operating Junction Temperature	– 55 to 150		

Table 4: Thermal Data

Rthj-Case	Thermal Resistance Junction-Case Max	2.5	°C/W
Rthj-a (4)	Thermal Operating Junction-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED) Table 5: On /Off

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_{D} = 250 \ \mu A, \ V_{GS} = 0$	30			V
IDSS	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T _C = 125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			± 100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		2.5	V
R _{DS(on}	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$		0.012 0.0135	0.015 0.017	Ω Ω

Table 6: Dynamic

Symbol	ol Parameter Test Conditions Min		Min.	Тур.	Max.	Unit
g _{fs} (5)	Forward Transconductance	V _{DS} = 15V, I _D = 4A		TBD		S
C _{iss}	Input Capacitance	V_{DS} = 25V, f= 1 MHz, V_{GS} = 0		965		pF
Coss	Output Capacitance			285		pF
C _{rss}	Reverse Transfer Capacitance			38		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	V _{DD} = 15 V, I _D = 4 A		15		ns
tr	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5V$ (see Figure 3)		32		ns
Qg Qgs Qgd	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 15V, I_D = 8 A, V_{GS} = 4.5 V (see Figure 5)		9 3.7 3	12	nC nC nC

Table 8: Switching

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off-Delay Time Fall Time	$V_{DD}=15 \text{ V}, \text{ I}_{D}=4 \text{ A},$ R _G = 4.7 Ω , V _{GS} = 4.5 V (see Figure 3)		18 8.5		ns ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (3)	Source-drain Current Source-drain Current (pulsed)				8 32	A A
V _{SD} (5)	Forward On Voltage	$I_{SD} = 8 \text{ A}, V_{GS} = 0$			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 8 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ $V_{DD} = 20\text{V}, \text{ T}_{\text{j}} = 150^{\circ}\text{C}$ (see Figure 4)		24 17.4 1.45		ns nC A

(1) The value is rated according Rthj-c

(2) The value is rated according R_{thj-a}
(3) Pulse width limited by safe operating area.

(4) When mounted on minimum footprint
(5) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3: Switching Times Test Circuit For Resistive Load

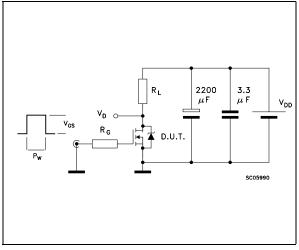


Figure 4: Test Circuit For Diode Recovery Times

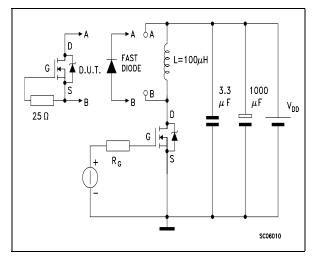
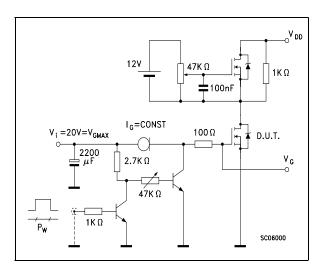


Figure 5: Gate Charge Test Circuit



PowerFLAT[™] (3.3x3.3) MECHANICAL DATA

DIM		mm.			inch	
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.23	0.30	0.38	0.009	0.011	0.015
С		0.328			0.012	
C1		0.12			0.004	
D		3.30			0.13	
D2	2.50	2.65	2.75	0.098	0.104	0.108
E		3.30			0.13	
E2	1.25	1.40	1.50	0.049	0.055	0.059
F		1.325			0.052	
F1		0.975			0.038	
е		0.65			0.025	
L	0.30		0.50	0.011		0.019

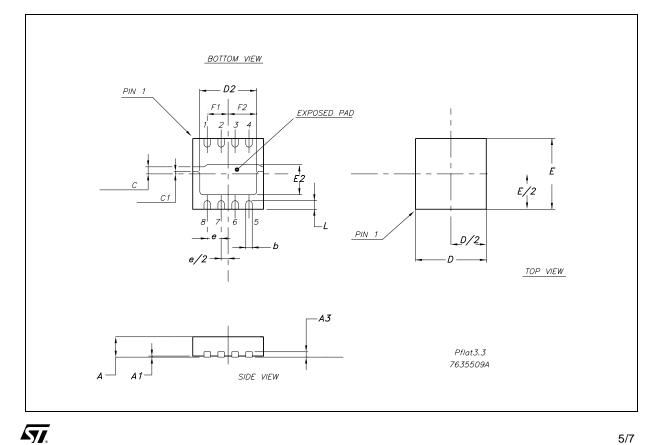


Table 10: Revision History

Date	Revision	Description of Changes
21-July-2004	1	First Release.
05-Oct-2004	2	Values changed
19-Oct-2004	3	New value inserted
22-Nov-2004	4	Document updated

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