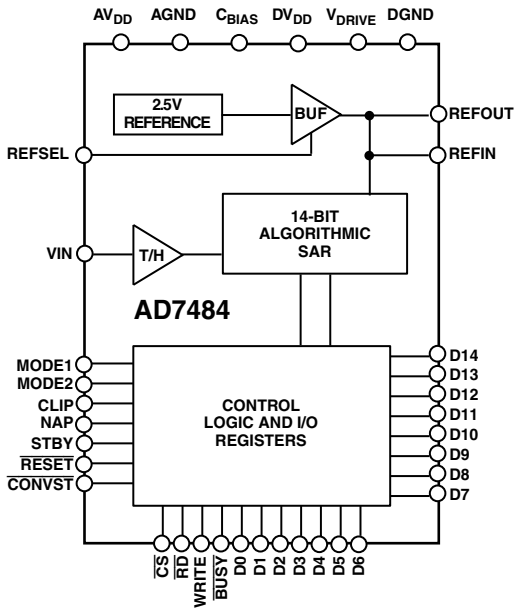
3 MSPS, 14-Bit SAR ADC

AD7484

FEATURES

Fast Throughput Rate: 3 MSPS
Wide Input Bandwidth: 40 MHz
No Pipeline Delays with SAR ADC
Excellent DC Accuracy Performance
Two Parallel Interface Modes
Low Power:
90 mW (Full Power) and 2.5 mW (NAP Mode)
Standby Mode: 2 μA Max
Single 5 V Supply Operation
Internal 2.5 V Reference
Full-Scale Overrange Mode (using 15th Bit)
System Offset Removal via User Access Offset Register
Nominal 0 V to 2.5 V Input with Shifted Range Capability
Pin Compatible Upgrade of 12-Bit AD7482

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7484 is a 14-bit, high speed, low power, successive-approximation ADC. The part features a parallel interface with throughput rates up to 3 MSPS. The part contains a low noise, wide bandwidth track-and-hold that can handle input frequencies in excess of 40 MHz.

The conversion process is a proprietary algorithmic successive-approximation technique that results in no pipeline delays. The input signal is sampled and a conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The conversion process is controlled via an internally trimmed oscillator. Interfacing is via standard parallel signal lines, making the part directly compatible with microcontrollers and DSPs.

The AD7484 provides excellent ac and dc performance specifications. Factory trimming ensures high dc accuracy resulting in very low INL, offset, and gain errors.

The part uses advanced design techniques to achieve very low power dissipation at high throughput rates. Power consumption in the normal mode of operation is 90 mW. There are two power-saving modes: a NAP Mode that keeps the reference circuitry alive for a quick power-up while consuming 2.5 mW, and a STANDBY Mode that reduces power consumption to a mere 10 μW.

The AD7484 features an on-board 2.5 V reference but can also accommodate an externally provided 2.5 V reference source. The nominal analog input range is 0 V to 2.5 V, but an offset shift capability allows this nominal range to be offset by ±200 mV. This allows the user considerable flexibility in setting the bottom end reference point of the signal range, a useful feature when using single-supply op amps.

The AD7484 also provides the user with an 8% overrange capability via a 15th bit. Thus, if the analog input range strays outside the nominal by up to 8%, the user can still accurately resolve the signal by using the 15th bit.

The AD7484 is powered by a 4.75 V to 5.25 V supply. The part also provides a V_{DRIVE} Pin that allows the user to set the voltage levels for the digital interface lines. The range for this V_{DRIVE} Pin is from 2.7 V to 5.25 V. The part is housed in a 48-lead LQFP package and is specified over a –40°C to +85°C temperature range.

REV. 0

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AD7484–SPECIFICATIONS[1] (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = External, f_{SAMPLE} = 3 MSPS; all specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[2,3]			
Signal-to-Noise + Distortion (SINAD)[4]	76.5	dB min	F_{IN} = 1 MHz
	78	dB typ	F_{IN} = 1 MHz
	79	dB typ	F_{IN} = 1 MHz, Extended Input
	77	dB typ	F_{IN} = 1 MHz, Internal Reference
Total Harmonic Distortion (THD)[4]	–90	dB max	
	–95	dB typ	
	–92	dB typ	Internal Reference
Peak Harmonic or Spurious Noise (SFDR)[4]	–90	dB max	
Intermodulation Distortion (IMD)[4]			
Second Order Terms	–96	dB typ	F_{IN1} = 95.053 kHz, F_{IN2} = 105.329 kHz
Third Order Terms	–94	dB typ	
Aperture Delay	10	ns typ	
Full-Power Bandwidth	40	MHz typ	@ 3 dB
	3.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	14	Bits	
Integral Nonlinearity[4]	±1	LSB max	
	±0.5	LSB typ	
Differential Nonlinearity[4]	±0.75	LSB max	Guaranteed No Missed Codes to 14 Bits
	±0.3	LSB typ	
Offset Error[4]	±6	LSB max	
	0.036	%FSR max	
Gain Error[4]	±6	LSB max	
	0.036	%FSR max	
ANALOG INPUT			
Input Voltage	–200	mV min	
	+2.7	V max	
DC Leakage Current	±1	μA max	V_{IN} from 0 V to 2.7 V
	±2	μA typ	V_{IN} = –200 mV
Input Capacitance[5]	35	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REFIN} Input Voltage	+2.5	V	±1% for Specified Performance
V_{REFIN} Input DC Leakage Current	±1	μA max	
V_{REFIN} Input Capacitance[5]	25	pF typ	
V_{REFIN} Input Current	220	μA typ	External Reference
V_{REFOUT} Output Voltage	+2.5	V typ	
V_{REFOUT} Error @ 25°C	±50	mV typ	
V_{REFOUT} Error T_{MIN} to T_{MAX}	±100	mV max	
V_{REFOUT} Output Impedance	1	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	V_{DRIVE} –1	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±1	μA max	
Input Capacitance, C_{IN}[5]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	0.7 × V_{DRIVE}	V min	
Output Low Voltage, V_{OL}	0.3 × V_{DRIVE}	V max	
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance[5]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	300	ns max	
Track-and-Hold Acquisition Time (t_{ACQ})	70	ns max	Sine Wave Input
	70	ns max	Full-Scale Step Input
Throughput Rate	2.5	MSPS max	Parallel Mode 1
	3	MSPS max	Parallel Mode 2

SPECIFICATIONS (continued)

(V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = External, f_{SAMPLE} = 3 MSPS; all specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Specification	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	5	V	±5%
V_{DRIVE}	2.7	V min	
	5.25	V max	
I_{DD}			
Normal Mode (Static)	12	mA max	$\overline{CS}$ and $\overline{RD}$ = Logic 1
Normal Mode (Operational)	18	mA max	
NAP Mode	0.5	mA max	
Standby Mode	2	μA max	
	0.5	μA typ	
Power Dissipation			
Normal Mode (Operational)	90	mW max	
NAP Mode	2.5	mW max	
Standby Mode[6]	10	μW max	

NOTES
[1]Temperature ranges as follows: –40°C to +85°C.
[2]SNR and SINAD figures quoted include external analog input circuit noise contribution of approximately 1 dB.
[3]See Typical Performance Characteristics section for analog input circuits used.
[4]See Terminology section.
[5]Sample tested @ 25°C to ensure compliance.
[6]Digital input levels at GND or V_{DRIVE}.

Specifications subject to change without notice.

TIMING CHARACTERISTICS*

(V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = External; all specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
DATA READ					
Conversion Time	t_{CONV}			300	ns
Quiet Time before Conversion Start	t_{QUIET}	100			ns
$\overline{CONVST}$ Pulsewidth	t_1	5			ns
$\overline{CONVST}$ Falling Edge to $\overline{BUSY}$ Falling Edge	t_2			20	ns
$\overline{CS}$ Falling Edge to $\overline{RD}$ Falling Edge	t_3	0			ns
Data Access Time	t_4			25	ns
$\overline{CONVST}$ Falling Edge to New Data Valid	t_5			30	ns
$\overline{BUSY}$ Rising Edge to New Data Valid	t_6			5	ns
Bus Relinquish Time	t_7		10		ns
$\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_8	0			ns
$\overline{CS}$ Pulsewidth	t_{14}	30			ns
$\overline{RD}$ Pulsewidth	t_{15}	30			ns
DATA WRITE					
WRITE Pulsewidth	t_9	5			ns
Data Setup Time	t_{10}	2			ns
Data Hold Time	t_{11}	6			ns
$\overline{CS}$ Falling Edge to WRITE Falling Edge	t_{12}	5			ns
WRITE Falling Edge to $\overline{CS}$ Rising Edge	t_{13}	0			ns

*All timing specifications given above are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.

Specifications subject to change without notice.

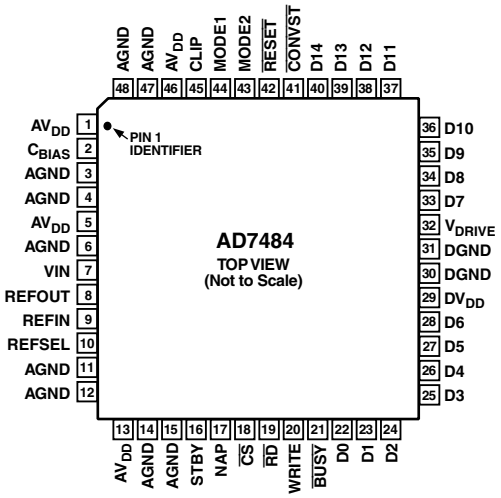
ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND ..... –0.3 V to +7 V
V_{DRIVE} to GND ..... –0.3 V to +7 V
Analog Input Voltage to GND ..... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND ..... –0.3 V to V_{DRIVE} + 0.3 V
REFIN to GND ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin except Supplies ..... ±10 mA
Operating Temperature Range
Commercial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
θ_{JA} Thermal Impedance ..... 50°C/W
θ_{JC} Thermal Impedance ..... 10°C/W
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... 215°C
Infrared (15 secs) ..... 220°C
ESD ..... 1 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Option
AD7484BST	–40°C to +85°C	Low-Profile Quad Flat Pack	ST-48
EVAL-AD7484CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES
[1]This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[2]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7484 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1, 5, 13, 46	AV_{DD}	Positive Power Supply for Analog Circuitry
2	C_{BIAS}	Decoupling Pin for Internal Bias Voltage. A 1 nF capacitor should be placed between this pin and AGND.
3, 4, 6, 11, 12, 14, 15, 47, 48	AGND	Power Supply Ground for Analog Circuitry
7	VIN	Analog Input. Single-ended analog input channel.
8	REFOUT	Reference Output. REFOUT connects to the output of the internal 2.5 V reference buffer. A 470 nF capacitor must be placed between this pin and AGND.
9	REFIN	Reference Input. A 470 nF capacitor must be placed between this pin and AGND. When using an external voltage reference source, the reference voltage should be applied to this pin.
10	REFSEL	Reference Decoupling Pin. When using the internal reference, a 1 nF capacitor must be connected from this pin to AGND. When using an external reference source, this pin should be connected directly to AGND.
16	STBY	Standby Logic Input. When this pin is logic high, the device will be placed in Standby Mode. See Power Saving section for further details.
17	NAP	NAP Logic Input. When this pin is logic high, the device will be placed in a very low power mode. See Power Saving section for further details.
18	$\overline{CS}$	Chip Select Logic Input. This pin is used in conjunction with $\overline{RD}$ to access the conversion result. The databus is brought out of three-state and the current contents of the output register driven onto the data lines following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ is also used in conjunction with WRITE to perform a write to the offset register. $\overline{CS}$ can be hardwired permanently low.
19	$\overline{RD}$	Read Logic Input. Used in conjunction with $\overline{CS}$ to access the conversion result.
20	WRITE	Write Logic Input. Used in conjunction with $\overline{CS}$ to write data to the offset register. When the desired offset word has been placed on the databus, the WRITE line should be pulsed high. It is the falling edge of this pulse that latches the word into the offset register.
21	$\overline{BUSY}$	Busy Logic Output. This pin indicates the status of the conversion process. The $\overline{BUSY}$ signal goes low after the falling edge of $\overline{CONVST}$ and stays low for the duration of the conversion. In Parallel Mode 1, the $\overline{BUSY}$ signal returns high when the conversion result has been latched into the output register. In Parallel Mode 2, the $\overline{BUSY}$ signal returns high as soon as the conversion has been completed, but the conversion result does not get latched into the output register until the falling edge of the next $\overline{CONVST}$ pulse.
22–28, 33–39	D0–D13	Data I/O Bits (D13 is MSB). These are three-state pins that are controlled by $\overline{CS}$, $\overline{RD}$, and WRITE. The operating voltage level for these pins is determined by the V_{DRIVE} input.
29	DV_{DD}	Positive Power Supply for Digital Circuitry
30, 31	DGND	Ground Reference for Digital Circuitry
32	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin will determine at what voltage the interface logic of the device will operate.
40	D14	Data Output Bit for Overranging. If the overrange feature is not used, this pin should be pulled to DGND via a 100 kΩ resistor.
41	$\overline{CONVST}$	Convert Start Logic Input. A conversion is initiated on the falling edge of the $\overline{CONVST}$ signal. The input track-and-hold amplifier goes from track mode to hold mode and the conversion process commences.
42	$\overline{RESET}$	Reset Logic Input. A falling edge on this pin resets the internal state machine and terminates a conversion that may be in progress. The contents of the offset register will also be cleared on this edge. Holding this pin low keeps the part in a reset state.
43	MODE2	Operating Mode Logic Input. See Table III for details.
44	MODE1	Operating Mode Logic Input. See Table III for details.
45	CLIP	Logic Input. A logic high on this pin enables output clipping. In this mode, any input voltage that is greater than positive full scale or less than negative full scale will be clipped to all "1s" or all "0s," respectively. Further details are given in the Offset/Overrange section.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 0.5 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track-and-hold returns to track mode).

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical *signal-to-(noise + distortion)* ratio for an ideal *N*-bit converter with a sine wave input is given by:

$$Signal\text{–}to\text{–}(Noise + Distortion) = \left(6.02\ N + 1.76\right)\ dB$$

Thus, for a 14-bit converter this is 86.04 *dB*.

Total Harmonic Distortion
Total harmonic distortion (*THD*) is the ratio of the rms sum of the harmonics to the fundamental. For the AD7484, it is defined as:

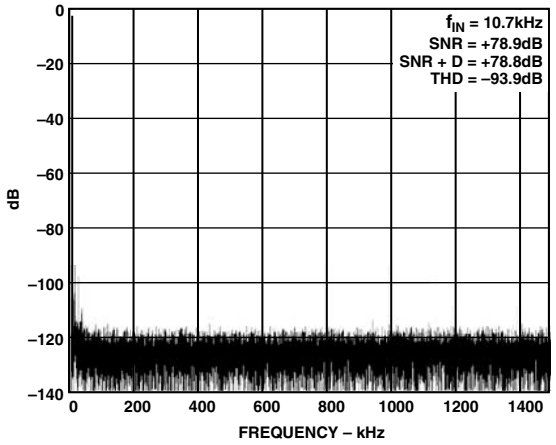
$$THD\ (dB) = 20\ log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

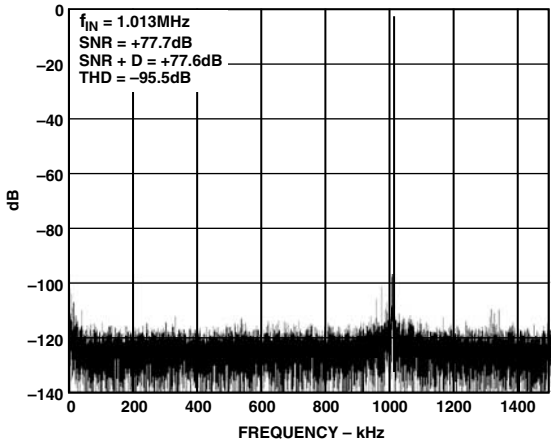
Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

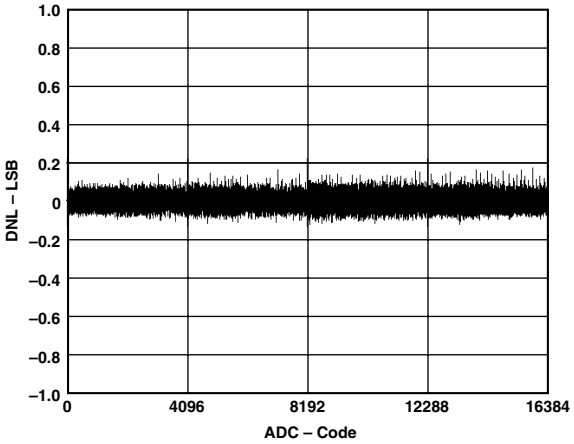
The AD7484 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.



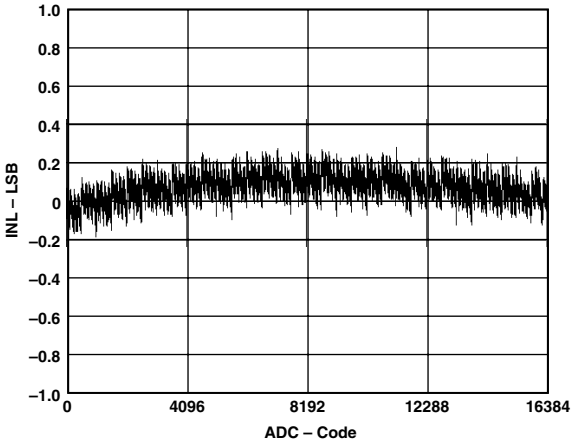
TPC 1. 64k FFT Plot With 10 kHz Input Tone



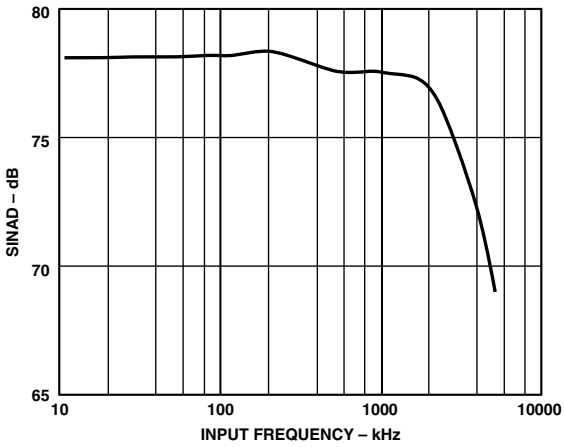
TPC 2. 64k FFT Plot With 1 MHz Input Tone



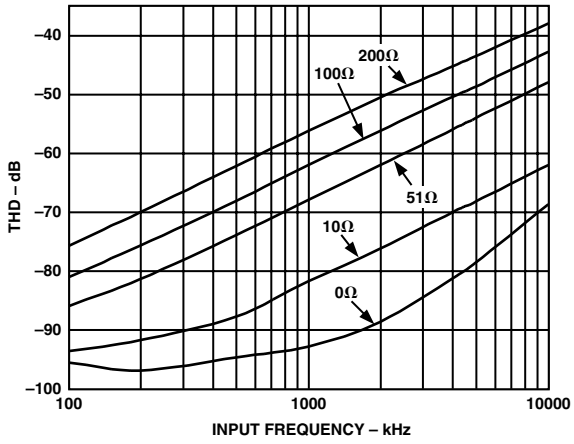
TPC 3. Typical DNL



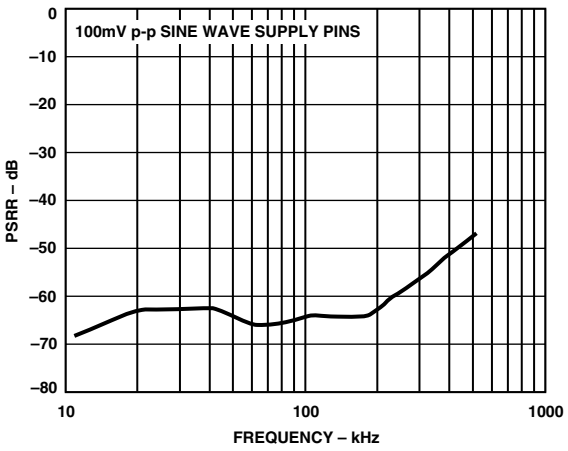
TPC 4. Typical INL



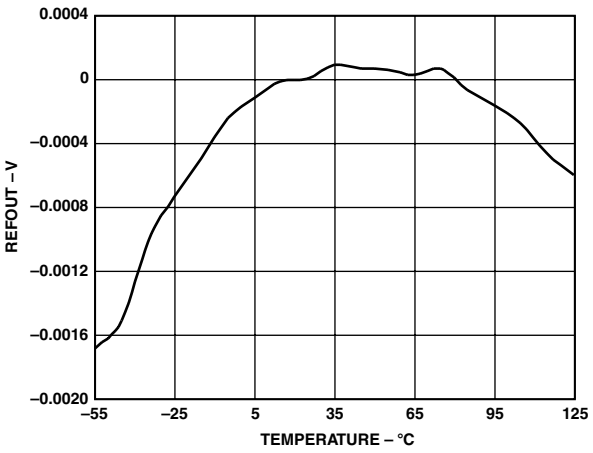
TPC 5. SINAD vs. Input Tone (AD8021 Input Circuit)



TPC 6. THD vs. Input Tone for Different Input Resistances



TPC 7. PSRR Without Decoupling



TPC 8. Reference Error

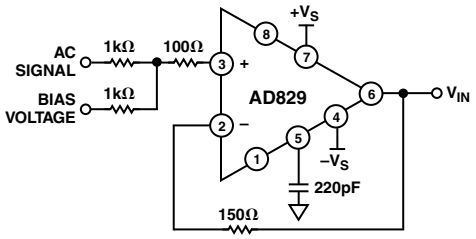


Figure 1. Analog Input Circuit Used for 10 kHz Input Tone

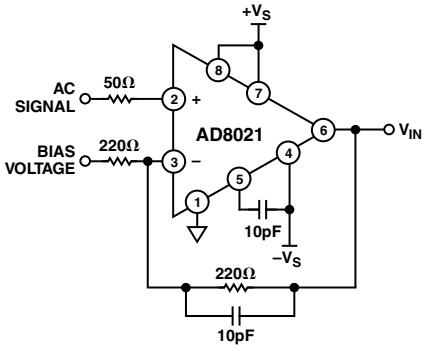


Figure 2. Analog Input Circuit Used for 1 MHz Input Tone

Figure 1 shows the analog input circuit used to obtain the data for the FFT plot shown in TPC 1. The circuit uses an Analog Devices AD829 op amp as the input buffer. A bipolar analog signal is applied as shown and biased up with a stable, low noise dc voltage connected to the labeled terminal shown. A 220 pF compensation capacitor is connected between Pin 5 of the AD829 and the analog ground plane. The AD829 is supplied with +12 V and –12 V supplies. The supply pins are decoupled as close to the device as possible, with both a 0.1 μF and 10 μF capacitor connected to each pin. In each case, the 0.1 μF capacitor should be the closer of the two caps to the device. More information on the AD829 is available on the Analog Devices website.

For higher input bandwidth applications, Analog Devices' AD8021 op amp (also available as a dual AD8022) is the recommended choice to drive the AD7484. Figure 2 shows the analog input circuit used to obtain the data for the FFT plot shown in TPC 2. A bipolar analog signal is applied to the terminal shown and biased up with a stable, low noise dc voltage connected as shown. A 10 pF compensation capacitor is connected between Pin 5 of the AD8021 and the negative supply. As with the previous circuit, the AD8021 is supplied with +12 V and –12 V supplies. The supply pins are decoupled as close to the device as possible, with both a 0.1 μF and 10 μF capacitor connected to each pin. In each case, the 0.1 μF capacitor should be the closer of the two caps to the device. The AD8021 logic reference pin is tied to analog ground, and the $\overline{\text{DISABLE}}$ Pin is tied to the positive supply as shown. Detailed information on the AD8021 is available on the Analog Devices website.

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7484 is a 14-bit algorithmic successive-approximation analog-to-digital converter based around a capacitive DAC. It provides the user with track-and-hold, reference, an A/D converter, and versatile interface logic functions on a single chip. The normal analog input signal range that the AD7484 can convert is 0 V to 2.5 V. By using the offset and overrange features on the ADC, the AD7484 can convert analog input signals from –200 mV to +2.7 V while operating from a single 5 V supply. The part requires a 2.5 V reference, which can be provided from the part's own internal reference or an external reference source. Figure 3 shows a very simplified schematic of the ADC. The control logic, SAR, and capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back to a balanced condition.

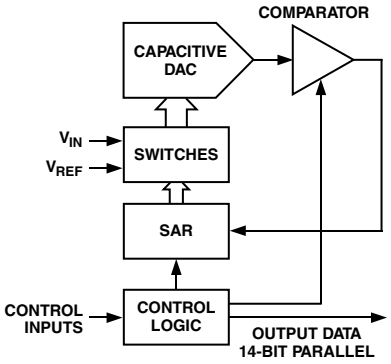


Figure 3. Simplified Block Diagram of AD7484

Conversion is initiated on the AD7484 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the track-and-hold goes from track mode to hold mode and the conversion sequence is started. Conversion time for the part is 300 ns. Figure 4 shows the ADC during conversion. When conversion starts, SW2 will open and SW1 will move to position B, causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR Register.

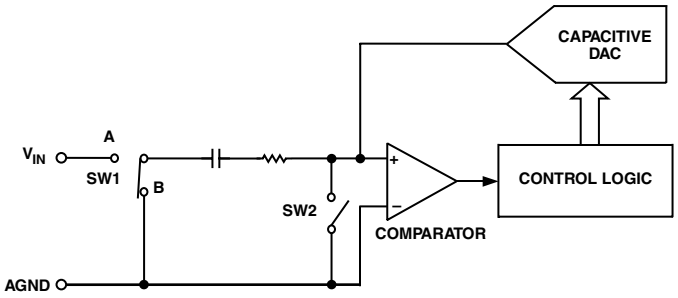


Figure 4. ADC Conversion Phase

At the end of conversion, the track-and-hold returns to track mode and the acquisition time begins. The track-and-hold acquisition time is 40 ns. Figure 5 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

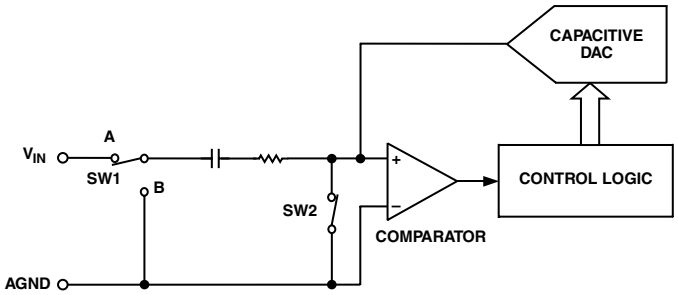


Figure 5. ADC Acquisition Phase

ADC TRANSFER FUNCTION

The output coding of the AD7484 is straight binary. The designed code transitions occur midway between the successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, and so on). The LSB size is $V_{REF}/16384$. The nominal transfer characteristic for the AD7484 is shown in Figure 6. This transfer characteristic may be shifted as detailed in the Offset/Overrange section.

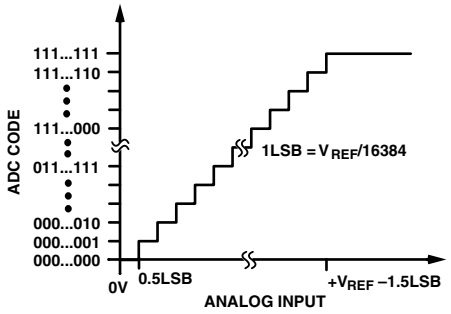


Figure 6. AD7484 Transfer Characteristic

POWER SAVING

The AD7484 uses advanced design techniques to achieve very low power dissipation at high throughput rates. In addition to this, the AD7484 features two power saving modes, NAP and Standby. These modes are selected by bringing either the NAP or STBY Pin to a logic high, respectively.

When operating the AD7484 in normal fully powered mode, the current consumption is 18 mA during conversion and the quiescent current is 12 mA. Operating at a throughput rate of 1 MSPS, the conversion time of 300 ns contributes 27 mW to the overall power dissipation.

$$(300\ ns/1\ \mu s) \times (5V \times 18\ mA) = 27\ mW$$

For the remaining 700 ns of the cycle, the AD7484 dissipates 42 mW of power.

$$(700\ ns/1\ \mu s) \times (5V \times 12\ mA) = 42\ mW$$

Thus, the power dissipated during each cycle is:

$$27\ mW + 42\ mW = 69\ mW$$

Figure 7 shows the AD7484 conversion sequence operating in normal mode.

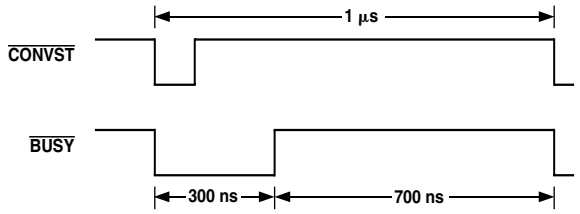


Figure 7. Normal Mode Power Dissipation

In NAP Mode, almost all of the internal circuitry is powered down. In this mode, the power dissipation of the AD7484 is reduced to 2.5 mW. When exiting NAP Mode, a minimum of 300 ns when using an external reference must be waited before initiating a conversion. This is necessary to allow the internal circuitry to settle after power-up and for the track-and-hold to properly acquire the analog input signal. The internal reference cannot be used in conjunction with the NAP Mode.

If the AD7484 is put into NAP Mode after each conversion, the average power dissipation will be reduced, but the throughput rate will be limited by the power-up time. Using the AD7484 with a throughput rate of 500 kSPS while placing the part in NAP Mode after each conversion would result in average power dissipation as follows:

The power-up phase contributes:

$$(300\ ns/2\ \mu s) \times (5\ V \times 12\ mA) = 9\ mW$$

The conversion phase contributes:

$$(300\ ns/2\ \mu s) \times (5\ V \times 18\ mA) = 13.5\ mW$$

While in NAP Mode for the rest of the cycle, the AD7484 dissipates only 1.75 mW of power.

$$(1400\ ns/2\ \mu s) \times (5\ V \times 0.5\ mA) = 1.75\ mW$$

Thus, the power dissipated during each cycle is:

$$9\ mW + 13.5\ mW + 1.75\ mW = 24.25\ mW$$

Figure 8 shows the AD7484 conversion sequence if putting the part into NAP Mode after each conversion.

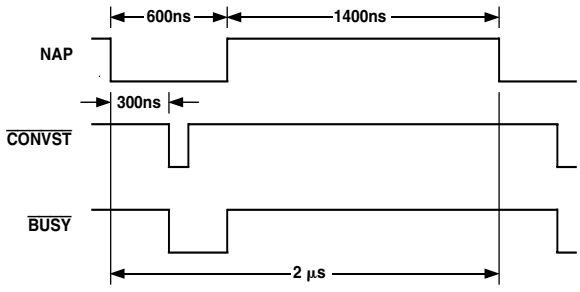


Figure 8. NAP Mode Power Dissipation

Figures 9 and 10 show a typical graphical representation of power versus throughput for the AD7484 when in normal and NAP Modes, respectively.

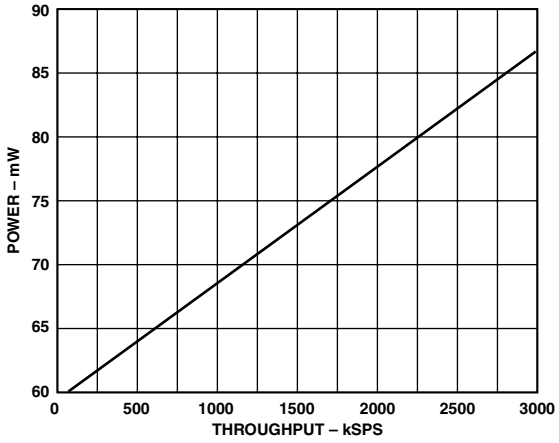


Figure 9. Normal Mode, Power vs. Throughput

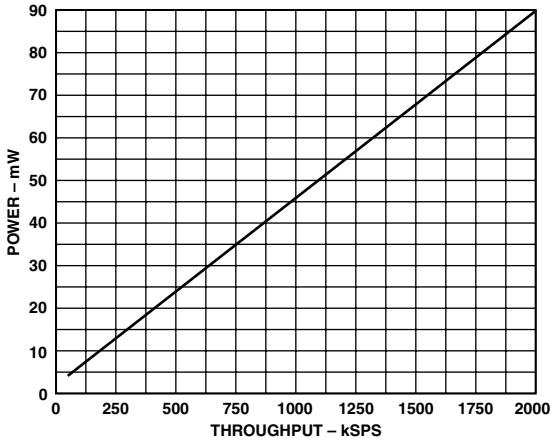


Figure 10. NAP Mode, Power vs. Throughput

In Standby Mode, all the internal circuitry is powered down and the power consumption of the AD7484 is reduced to 10 µW. The power-up time necessary before a conversion can be initiated is longer because more of the internal circuitry has been powered down. In using the internal reference of the AD7484, the ADC must be brought out of Standby Mode 500 ms before a conversion is initiated. Initiating a conversion before the required power-up time has elapsed will result in incorrect conversion data. If an external reference source is used and kept powered up while the AD7484 is in standby mode, the power-up time required will be reduced to 80 µs.

OFFSET/OVERRANGE

The AD7484 provides a ±8% overrange capability as well as a programmable offset register. The overrange capability is achieved by the use of a 15th bit (D14) and the CLIP input. If the CLIP input is at logic high and the contents of the offset register are zero, then the AD7484 operates as a normal 14-bit ADC. If the input voltage is greater than the full-scale voltage, the data output from the ADC will be all "1s." Similarly, if the input voltage is lower than the zero-scale voltage, the data output from the ADC will be all "0s." In this case, D14 acts as an overrange indicator. It is set to "1" if the analog input voltage is outside the nominal 0 V to 2.5 V range.

If the offset register contains any value other than "0," the contents of the register are added to the SAR result at the end of conversion. This has the effect of shifting the transfer function of the ADC as shown in Figure 11 and Figure 12. However, it should be noted that with the CLIP input set to logic high, the maximum and minimum codes that the AD7484 will output will be 0x3FFF and 0x0000, respectively. Further details are given in Table I and Table II.

Figure 11 shows the effect of writing a positive value to the offset register. If, for example, the contents of the offset register contained the value 1024, then the value of the analog input voltage for which the ADC would transition from reading all "0s" to 000...001 (the bottom reference point) would be:

$$0.5\ LSB - \left(1024\ LSB\right) = -156.326\ mV$$

The analog input voltage for which the ADC would read full-scale (0x3FFF) in this example would be:

$$2.5V - 1.5\ LSB - \left(1024\ LSB\right) = 2.34352V$$

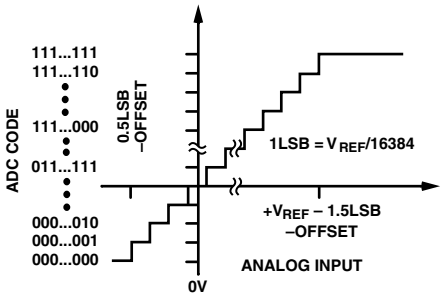


Figure 11. Transfer Characteristic with Positive Offset

The effect of writing a negative value to the offset register is shown in Figure 12. If a value of –512 was written to the offset register, the bottom end reference point would now occur at:

$$0.5\ LSB - \left(-512\ LSB\right) = 78.20\ mV$$

Following this, the analog input voltage needed to produce a full-scale (0x3FFF) result from the ADC would now be:

$$2.5V - 1.5\ LSB - \left(-512\ LSB\right) = 2.5779V$$

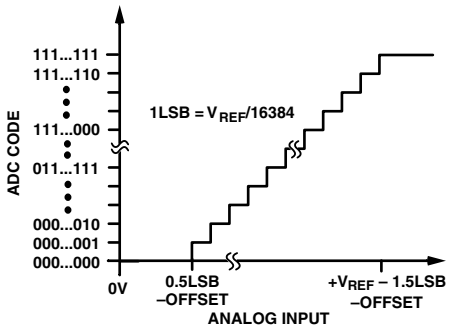


Figure 12. Transfer Characteristic with Negative Offset

Table I shows the expected ADC result for a given analog input voltage with different offset values and with CLIP tied to logic high. The combined advantages of the offset and overrange features of the AD7484 are shown clearly in Table II. It shows the same range of analog input and offset values as Table I but with the clipping feature disabled.

Table I. Clipping Enabled (CLIP = 1)

Offset	–512	0	+1024	
VIN	ADC DATA, D[0:13]			D14
–200 mV	0	0	0	1 1 1
–156.3 mV	0	0	0	1 1 0
0 V	0	0	1024	1 0 0
+78.2 mV	0	512	1536	0 0 0
+2.3435 V	14846	15358	16383	0 0 0
+2.5 V	15871	16383	16383	0 0 1
+2.5779 V	16383	16383	16383	0 1 1
+2.7 V	16383	16383	16383	1 1 1

Table II. Clipping Disabled (CLIP = 0)

Offset	–512	0	+1024
VIN	ADC DATA, D[0:14]		
–200 mV	–1823	–1311	–287
–156.3 mV	–1536	–1024	0
0 V	–512	0	1024
+78.2 mV	0	512	1536
+2.3435 V	14846	15358	16382
+2.5 V	15872	16384	17408
+2.5779 V	16383	16895	17919
+2.7 V	17183	17695	18719

Values from –1310 to +1310 may be written to the offset register. These values correspond to an offset of ±200 mV. A write to the offset register is performed by writing a 13-bit word to the part as detailed in the Parallel Interface section. The 12 LSBs of the 15-bit word contain the offset value, while the 3 MSBs must be set to 0. Failure to write zeros to the 3 MSBs may result in the incorrect operation of the device.

PARALLEL INTERFACE

The AD7484 features two parallel interfacing modes. These modes are selected by the mode pins as detailed in Table III.

Table III. Operating Modes

	Mode 2	Mode 1
Do Not Use	0	0
Parallel Mode 1	0	1
Parallel Mode 2	1	0
Do Not Use	1	1

In Parallel Mode 1, the data in the output register is updated on the rising edge of $\overline{BUSY}$ at the end of a conversion and is available for reading almost immediately afterwards. Using this mode, throughput rates of up to 2.5 MSPS can be achieved. This mode should be used if the conversion data is required immediately after the conversion has completed. An example where this may be of use is if the AD7484 was operating at much lower throughput rates in conjunction with NAP Mode (for power-saving reasons), and the input signal was being compared with set limits within the DSP or other controller. If the limits were exceeded, the ADC would then be brought immediately into full power operation and commence sampling at full speed. Figure 17 shows a timing diagram for the AD7484 operating in Parallel Mode 1 with both $\overline{CS}$ and $\overline{RD}$ tied low.

In Parallel Mode 2, the data in the output register is not updated until the next falling edge of $\overline{CONVST}$. This mode could be used where a single sample delay is not vital to the system operation and conversion speeds of greater than 2.5 MSPS are desired. This may occur, for example, in a system where a large amount of samples are taken at high speed before a Fast Fourier Transform is performed for frequency analysis of the input signal. Figure 18 shows a timing diagram for the AD7484 operating in Parallel Mode 2 with both $\overline{CS}$ and $\overline{RD}$ tied low.

Data must not be read from the AD7484 while a conversion is taking place. For this reason, if operating the AD7484 at throughput speeds greater than 2.5 MSPS, it will be necessary to tie both the $\overline{CS}$ and $\overline{RD}$ Pins on the AD7484 low and use a buffer on the data lines. This situation may also arise in the case where a read operation cannot be completed in the time after the end of one conversion and the start of the quiet period before the next conversion.

The maximum slew rate at the input of the ADC should be limited to 500v/µS while $\overline{BUSY}$ is low to avoid corrupting the ongoing conversion. In any multiplexed application where the channel is switched during conversion, this should happen as early as possible after the $\overline{BUSY}$ falling edge.

Reading Data from the AD7484

Data is read from the part via a 15-bit parallel databus with the standard $\overline{CS}$ and $\overline{RD}$ signals. The $\overline{CS}$ and $\overline{RD}$ signals are internally gated to enable the conversion result onto the databus. The data lines D0 to D14 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low. Therefore, $\overline{CS}$ may be permanently tied logic low if required, and the $\overline{RD}$ signal used to access the conversion result. Figure 15 shows a timing specification called t_{QUIET}. This is the amount of time that should be left after any databus activity before the next conversion is initiated.

Writing to the AD7484

The AD7484 features a user-accessible offset register. This allows the bottom of the transfer function to be shifted by ±200 mV. This feature is explained in more detail in the Offset/Overrange section.

To write to the offset register, a 15-bit word is written to the AD7484 with the 12 LSBs containing the offset value in two's complement format. The 3 MSBs must be set to 0. The offset value must be within the range –1310 to +1310, corresponding to an offset from –200 mV to +200 mV. The value written to the offset register is stored and used until power is removed from the device, or the device is reset. The value stored may be updated at any time between conversions by another write to the device. Table IV shows some examples of offset register values and their effective offset voltage. Figure 16 shows a timing diagram for writing to the AD7484.

Table IV. Offset Register Examples

Code (Dec)	D14–D12	D11–D0 (Two's Complement)	Offset (mV)
–1310	000	101011100010	–200
–512	000	111000000000	–78.12
+256	000	000100000000	+39.06
+1310	000	010100011110	+200

Driving the $\overline{CONVST}$ Pin

To achieve the specified performance from the AD7484, the $\overline{CONVST}$ Pin must be driven from a low-jitter source. Since the falling edge on the $\overline{CONVST}$ Pin determines the sampling instant, any jitter that may exist on this edge will appear as noise when the analog input signal contains high frequency components. The relationship between the analog input frequency (f_{IN}), timing jitter (t_j), and resulting SNR is given by the equation:

$$SNR_{JITTER}(dB) = 10\log\frac{1}{(2\pi \times f_{IN} \times t_j)^2}$$

As an example, if the desired SNR due to jitter was 100 dB with a maximum full-scale analog input frequency of 1.5 MHz, ignoring all other noise sources, the result is an allowable jitter on the $\overline{CONVST}$ falling edge of 1.06 ps. For a 14-bit converter (ideal SNR = 86.04 dB), the allowable jitter will be greater than the figure given above, but due consideration must be given to the design of the $\overline{CONVST}$ circuitry to achieve 14-bit performance with large analog input frequencies.

Typical Connection

Figure 13 shows a typical connection diagram for the AD7484 operating in Parallel Mode 1. Conversion is initiated by a falling edge on $\overline{\text{CONVST}}$. Once $\overline{\text{CONVST}}$ goes low, the $\overline{\text{BUSY}}$ signal goes low, and at the end of conversion, the rising edge of $\overline{\text{BUSY}}$ is used to activate an interrupt service routine. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ lines are then activated to read the 14 data bits (15 bits if using the overrange feature).

In Figure 13, the V_{DRIVE} Pin is tied to DV_{DD}, which results in logic output levels being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output levels would be either 0 V or 3 V. This feature allows the AD7484 to interface to 3 V devices while still enabling the ADC to process signals at a 5 V supply.

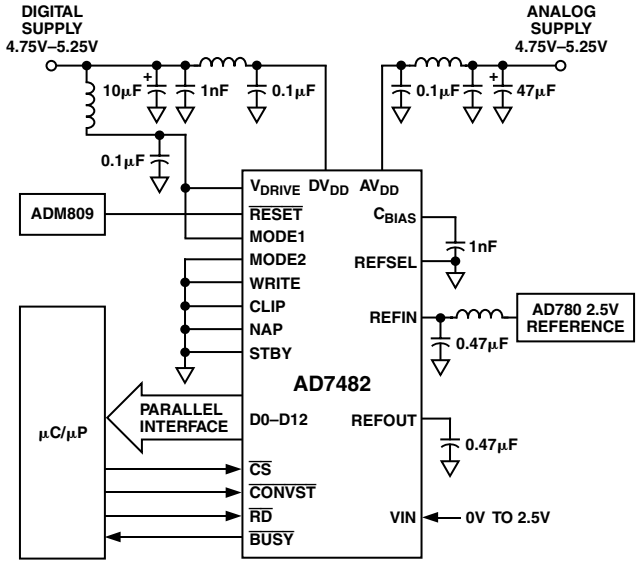


Figure 13. Typical Connection Diagram

Board Layout and Grounding

To obtain optimum performance from the AD7484, it is recommended that a printed circuit board with a minimum of three layers be used. One of these layers, preferably the middle layer, should be as complete a ground plane as possible to give the best shielding. The board should be designed in such a way that the analog and digital circuitry is separated and confined to certain areas of the board. This practice, along with avoiding running digital and analog lines close together, should help to avoid coupling digital noise onto analog lines.

The power supply lines to the AD7484 should be approximately 3 mm wide to provide low impedance paths and reduce the effects of glitches on the power supply lines. It is vital that good decoupling is also present. A combination of ferrites and decoupling capacitors should be used as shown in Figure 13.

The decoupling capacitors should be as close to the supply pins as possible. This is made easier by the use of multilayer boards. The signal traces from the AD7484 pins can be run on the top layer while the decoupling capacitors and ferrites can be mounted on the bottom layer where the power traces exist. The ground plane between the top and bottom planes provide excellent shielding.

Figures 14a to 14e show a sample layout of the board area immediately surrounding the AD7484. Pin 1 is the bottom left corner of the device. Figure 14a shows the top layer where the AD7484 is mounted with vias to the bottom routing layer highlighted. Figure 14b shows the bottom layer where the power routing is with the same vias highlighted. Figure 14c shows the bottom layer silkscreen where the decoupling components are soldered directly beneath the device. Figure 14d shows the silkscreen overlaid on the solder pads for the decoupling components, and Figure 14e shows the top and bottom routing layers overlaid. The black area in each figure indicates the ground plane present on the middle layer.

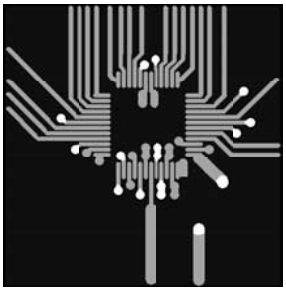


Figure 14a

Figure 14b

Figure 14c

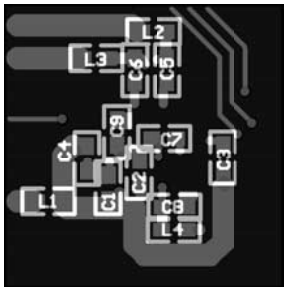


Figure 14d

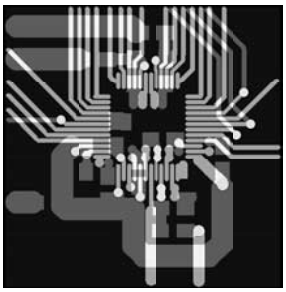


Figure 14e

C1–6: 100 nF, C7–8: 470 nF, C9: 1 nF

L1–4: Meggit-Sigma Chip Ferrite Beads (BMB2A0600RS2)

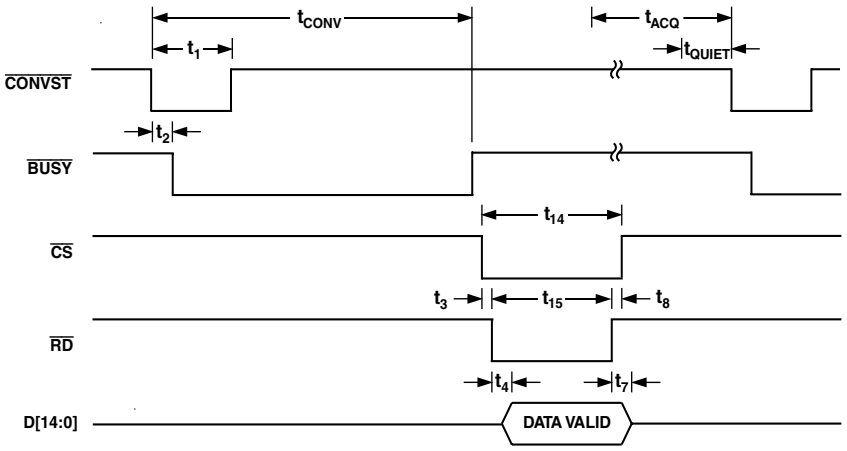


Figure 15. Parallel Mode READ Cycle

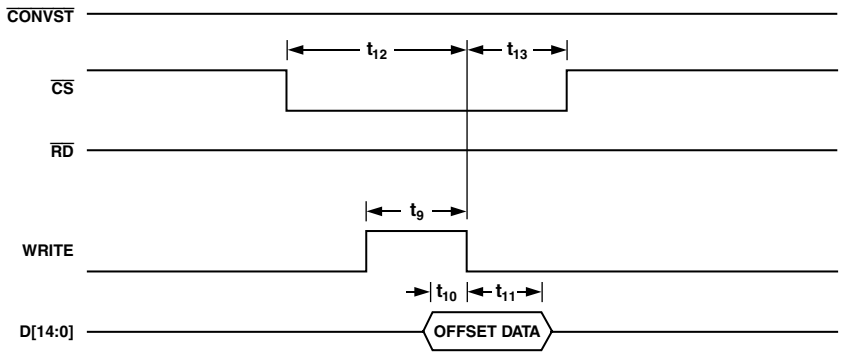


Figure 16. Parallel Mode WRITE Cycle

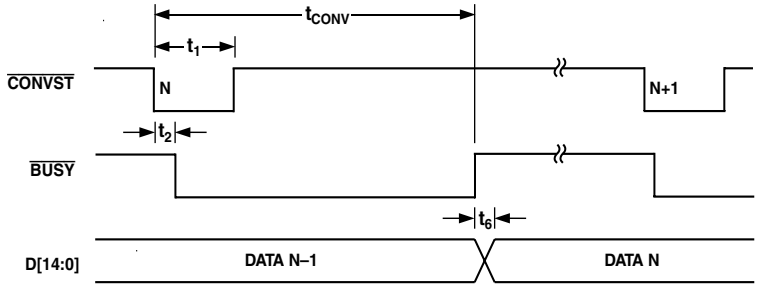


Figure 17. Parallel Mode 1 READ Cycle

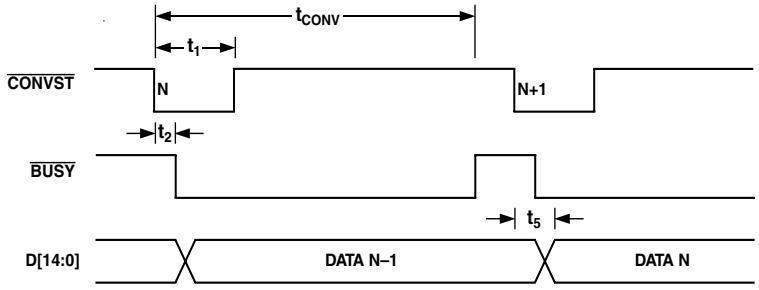
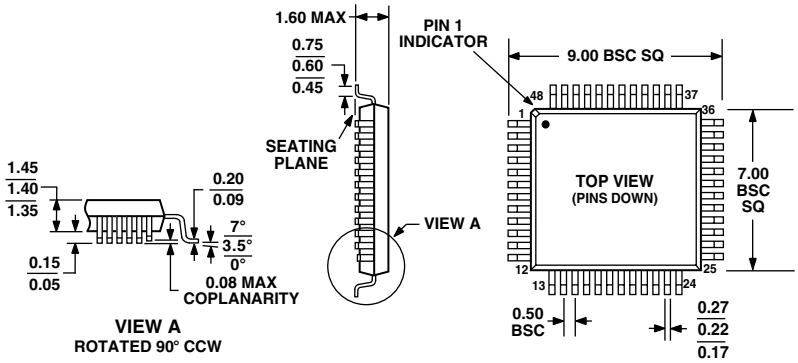


Figure 18. Parallel Mode 2 READ Cycle

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
(ST-48)
Dimensions shown in millimeters



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