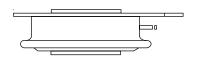


Vishay High Power Products

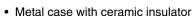
Phase Control Thyristors (Hockey PUK Version), 500 A

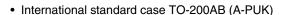


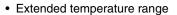
TO-200AB (A-PUK)

FEATURES









· Lead (Pb)-free



ROHS

PRODUCT SUMMARY I_{T(AV)} 500 A

TYPICAL APPLICATIONS

- · DC motor controls
- Controlled DC power supplies
- · AC controllers

MAJOR RATINGS AND CHARACTERISTICS							
PARAMETER	TEST CONDITIONS	VALUES	UNITS				
		500	А				
$I_{T(AV)}$	T _{hs}	80	°C				
1		1130	А				
I _{T(RMS)}	T _{hs}	25	°C				
1	50 Hz	7200	^				
I _{TSM}	60 Hz	7500	Α				
l ² t	50 Hz	260	1.42-				
I-I	60 Hz	230	kA ² s				
V _{DRM} /V _{RRM}		400 to 600	V				
t _q	Typical	100	μs				
T _J		- 40 to 150	°C				

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V _{DRM} /V _{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA			
ST280CHC 04		400	500	75			
31200CHC	06 600		700	75			

ST280CHPbF Series

Vishay High Power Products Phase Control Thyristors (Hockey PUK Version), 500 A



ABSOLUTE MAXIMUM RATIN	GS						
PARAMETER	SYMBOL		TEST CONDITIONS			UNITS	
Maximum average on-state current	-	180° condu	180° conduction, half sine wave		500 (185)	Α	
at heatsink temperature	$I_{T(AV)}$	double side	(single side) co	oled	80 (110)	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C	heatsink tempe	erature double side cooled	1130		
		t = 10 ms	No voltage		7200		
Maximum peak, one-cycle	I _{TSM}	t = 8.3 ms	reapplied		7500	A kA ² s	
non-repetitive surge current		t = 10 ms	100 % V _{RRM}	Sinusoidal half wave, initial $T_J = T_J$ maximum	6000		
		t = 8.3 ms	reapplied		6300		
	l ² t	t = 10 ms	No voltage		260		
Maximum 12t for fraing		t = 8.3 ms	reapplied		235		
Maximum I ² t for fusing		t = 10 ms	100 % V _{RRM}		180		
		t = 8.3 ms reapplied		165	1		
Maximum I $^2\sqrt{t}$ for fusing	I ² √t	t = 0.1 to 10	t = 0.1 to 10 ms, no voltage reapplied			kA²√s	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % x π	x I _{T(AV)} < I < π x	$I_{T(AV)}$, $T_J = T_J$ maximum	0.84	V	
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(A)})$	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			ľ	
Low level value of on-state slope resistance	r _{t1}	$(16.7 \% \text{ x } \pi \text{ x } I_{T(AV)} < I < \pi \text{ x } I_{T(AV)}), T_J = T_J \text{ maximum}$			0.50	m 0	
High level value of on-state slope resistance	r _{t2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			0.47	mΩ	
Maximum on-state voltage	V_{TM}	$I_{pk} = 1000 \text{ A}, T_J = T_J \text{ maximum}, t_p = 10 \text{ ms sine pulse}$			1.35	V	
Maximum holding current	I _H	T 05 °C	T _J = 25 °C, anode supply 12 V resistive load		600	A	
Maximum (typical) latching current	ΙL	1]=25 °C,	anoue supply 17	z v resistive idad	1000 (300)	- mA	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dl/dt	Gate drive 20 V, 20 Ω , $t_r \le 1~\mu s$ $T_J = T_J$ maximum, anode voltage $\le 80~\%~V_{DRM}$	1000	A/µs
Typical delay time	t _d	Gate current 1 A, $dl_g/dt = 1$ A/ μ s V_d 0.67 % V_{DRM} , $T_J = 25$ °C	1.0	
Typical turn-off time	t _q	$I_{TM}=300~A,~T_J=T_J~maximum,~dl/dt=20~A/\mu s, \\ V_R=50~V,~dV/dt=20~V/\mu s,~gate~0~V~100~\Omega,~t_p=500~\mu s$	100	μs

BLOCKING							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs			
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	75	mA			





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TRIGGERING						
PARAMETER	CVMBOL	TE	TECT CONDITIONS			UNITS
PANAMETEN	STINIBUL	SYMBOL TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum,	$t_p \leq 5 \ ms$	10	0.0	W
Maximum average gate power	P _{G(AV)}	$T_J = T_J$ maximum,	f = 50 Hz, d% = 50	2	.0	VV
Maximum peak positive gate current	I _{GM}	$T_J = T_J$ maximum,	$t_p \leq 5 \text{ ms}$	3	.0	Α
Maximum peak positive gate voltage	+ V _{GM}	20		0	V	
Maximum peak negative gate voltage	- V _{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms			5.0	
	I _{GT}	T _J = - 40 °C		180	-	mA
DC gate current required to trigger		T _J = 25 °C	Maximum required gate trigger/	90	150	
		T _J = 150 °C current/voltage are the lowes		30	-	
		T _J = - 40 °C	value which will trigger all units	2.9	-	
DC gate voltage required to trigger	V _{GT}	T _J = 25 °C	12 V anode to cathode applied	1.8	3.0	V
		T _J = 150 °C		1.0	-	
DC gate current not to trigger	I _{GD}	T - T movimum	Maximum gate current/voltage not to trigger is the maximum	10		mA
DC gate voltage not to trigger	V _{GD}	$T_J = T_J \text{ maximum}$	value which will not trigger any unit with rated V _{DRM} anode to cathode applied	0.:	30	V

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	ARAMETER SYMBOL TEST CONDITIONS		VALUES	UNITS		
Maximum operating junction and storage temperature range	T _J , T _{Stg}		- 40 to 150	°C		
Maximum thermal resistance,	В	DC operation single side cooled	0.17			
junction to heatsink	R _{thJ-hs}	DC operation double side cooled	0.08	K/W		
Maximum thermal resistance,	В	DC operation single side cooled	0.033	TV/VV		
case to heatsink	R _{thC-hs}	DC operation double side cooled	0.017			
Mounting force, ± 10 %			4900	N		
Woulding force, ± 10 /8			(500)	(kg)		
Approximate weight			50	g		
Case style		See dimensions - link at the end of datasheet	TO-200AB (A	A-PUK)		

∆R _{thJ-hs} CONDUCTIO	∆R _{thJ-hs} CONDUCTION							
CONDUCTION ANGLE	SINUSOIDAL	CONDUCTION	RECTANGULA	R CONDUCTION	TEGT COMPLETIONS	UNITS		
CONDUCTION ANGLE	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE	TEST CONDITIONS	UNITS		
180°	0.016	0.017	0.011	0.011				
120°	0.019	0.019	0.019	0.019				
90°	0.024	0.024	0.026	0.026	$T_J = T_J$ maximum	K/W		
60°	0.035	0.035	0.036	0.037				
30°	0.060	0.060	0.060	0.061				

Note

• The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

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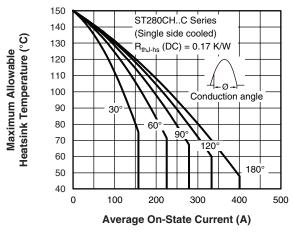


Fig. 1 - Current Ratings Characteristics

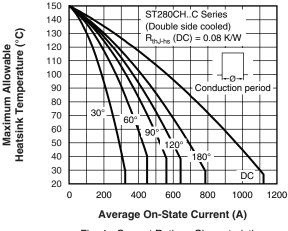


Fig. 4 - Current Ratings Characteristics

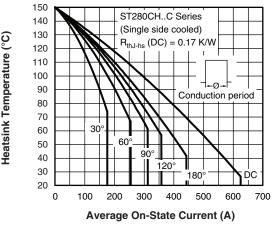


Fig. 2 - Current Ratings Characteristics

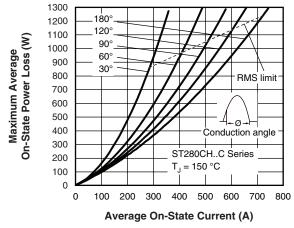


Fig. 5 - On-State Power Loss Characteristics

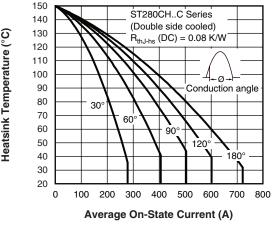


Fig. 3 - Current Ratings Characteristics

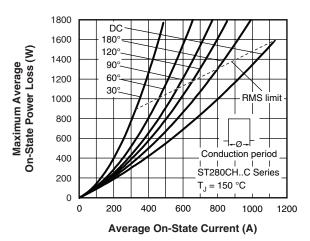


Fig. 6 - On-State Power Loss Characteristics

Maximum Allowable

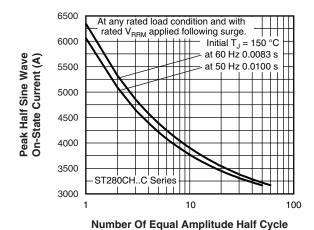
Maximum Allowable

4





Phase Control Thyristors Vishay High Power Products (Hockey PUK Version), 500 A



Current Pulses (N)

Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

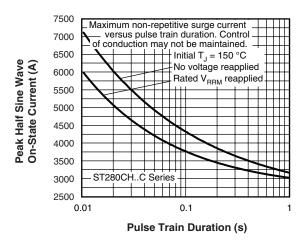


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

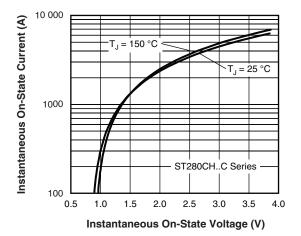


Fig. 9 - On-State Voltage Drop Characteristics

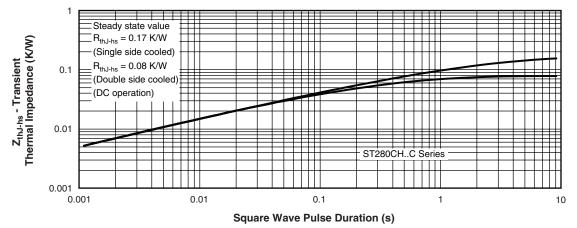


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

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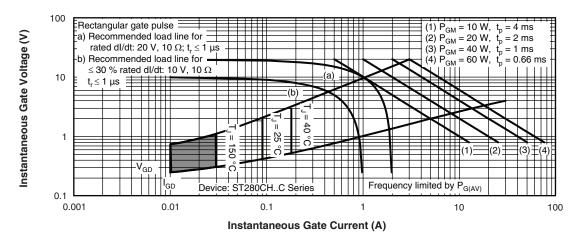


Fig. 11 - Gate Characteristics

Device code

ORDERING INFORMATION TABLE

ST	28	0	СН	06	С	1	-	PbF
1	2	3	4	5	6	7	8	9

1 - Thyristor

2 - Essential part number

3 - 0 = Converter grade

4 - CH = Ceramic PUK, high temperature

Voltage code x 100 = V_{RRM} (see Voltage Ratings table)

6 - C = PUK case TO-200AB (A-PUK)

7 - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)

1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)

2 = Eyelet terminals (gate and auxiliary cathode soldered leads)

3 = Fast-on terminals (gate and auxiliary cathode soldered leads)

8 - Critical dV/dt: • None = 500 V/µs (standard selection)

• L = 1000 V/µs (special selection)

9 - Lead (Pb)-free

LINKS TO RELATED DOCUMENTS				
Dimensions	http://www.vishay.com/doc?95074			



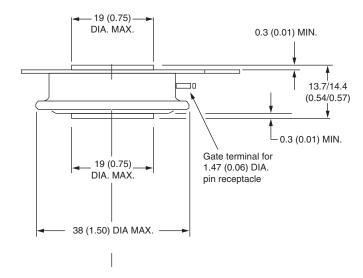
Vishay Semiconductors

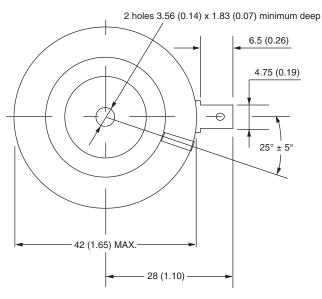
TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate

Creepage distance: 7.62 (0.30) minimum Strike distance: 7.12 (0.28) minimum





Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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