# RHF1401

## Rad-hard 14-bit 30 Msps A/D converter

**Datasheet – production data**

## Features

- Qml-V qualified, smd 5962-06260
- Rad hard: 300 kRad(Si) TID
- Failure immune (SEFI) and latch-up immune (SEL) up to 120 MeV-cm$^2$/mg at 2.7 V and 125° C
- Hermetic package
- Tested at $F_s$ = 20 Msps
- Low power: 85 mW at 20 Msps
- Optimized for 2 Vpp differential input
- High linearity and dynamic performances
- 2.5 V/3.3 V compatible digital I/O
- Internal reference voltage with external reference option

**Ceramic SO-48 package**

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package.

## Applications

- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics

## Description

The RHF1401 is a 14-bit analog-to-digital converter that uses pure (ELDRS-free) CMOS 0.25 µm technology combining high performance, radiation robustness and very low power consumption.

The RHF1401 is based on a pipeline structure and digital error correction to provide excellent static linearity. Specifically designed to optimize power consumption, the device only dissipates 85 mW at 20 Msps, while maintaining a high level of performance. The device also integrates a proprietary track-and-hold structure to ensure a large effective resolution bandwidth.

Voltage references are integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs to allow common bus sharing. A data-ready signal, which is raised when the data is valid on the output, can be used for synchronization purposes.

The RHF1401 has an operating temperature range of -55° C to +125° C and is available in a small 48-pin ceramic SO-48 package.

**Table 1. Device summary**

| Order code | SMD pin | Quality level | Package | Lead finish | Mass | EPPL(1) | Temp range |
|---|---|---|---|---|---|---|---|
| RHF1401KSO1 | - | Engineering model | SO-48 | Gold | 1.1 g | Yes | -55 °C to +125 °C |
| RHF1401KSO-01V | 5962F0626001VXC | QMLV-Flight | | | | | |

1. EPPL = ESA preferred part list



This is information on a product in full production. www.st.com

# Contents


**1 Description . . . . . 7**

1.1 Block diagram . . . . . 7

1.2 Pin connections . . . . . 8

1.3 Pin descriptions . . . . . 9

1.4 Equivalent circuits . . . . . 10

**2 Electrical characteristics . . . . . 12**

2.1 Absolute maximum ratings and operating conditions . . . . . 12

2.2 Timing characteristics . . . . . 13

2.3 Electrical characteristics (after 300 kRad) . . . . . 14

2.4 Results for differential input . . . . . 16

2.5 Results for single ended input . . . . . 21

**3 User manual . . . . . 25**

3.1 Optimizing the power consumption . . . . . 25

3.2 Driving the analog input . . . . . 27

3.2.1 Differential mode . . . . . 27

3.2.2 Single-ended mode . . . . . 29

3.3 Reference connections . . . . . 31

3.3.1 Internal voltage reference . . . . . 31

3.3.2 External voltage reference . . . . . 31

3.4 Clock input . . . . . 33

3.5 Operating modes . . . . . 34

3.5.1 Digital inputs . . . . . 34

3.5.2 Digital outputs . . . . . 34

3.5.3 Digital output load considerations . . . . . 35

3.6 PCB layout precautions . . . . . 35

**4 Definitions of specified parameters . . . . . 36**

4.1 Static parameters . . . . . 36

4.2 Dynamic parameters . . . . . 36

**5 Package information . . . . . 37**

6 Ordering information . . . . . 39

7 Revision history . . . . . 40

# List of tables

Table 1. Device summary . . . 1
Table 2. Pin descriptions . . . 9
Table 3. Absolute maximum ratings . . . 12
Table 4. Operating conditions . . . 12
Table 5. Timing characteristics . . . 13
Table 6. Analog inputs . . . 14
Table 7. Internal reference voltage . . . 14
Table 8. External reference voltage . . . 14
Table 9. Static accuracy . . . 14
Table 10. Digital inputs and outputs . . . 15
Table 11. Dynamic characteristics . . . 15
Table 12. Differential mode output codes . . . 27
Table 13. Single-ended mode output codes with Vinb = INCM . . . 29
Table 14. RHF1401 operating modes . . . 34
Table 15. Ceramic SO-48 package mechanical data . . . 38
Table 16. Order codes . . . 39
Table 17. Document revision history . . . 40

# List of figures

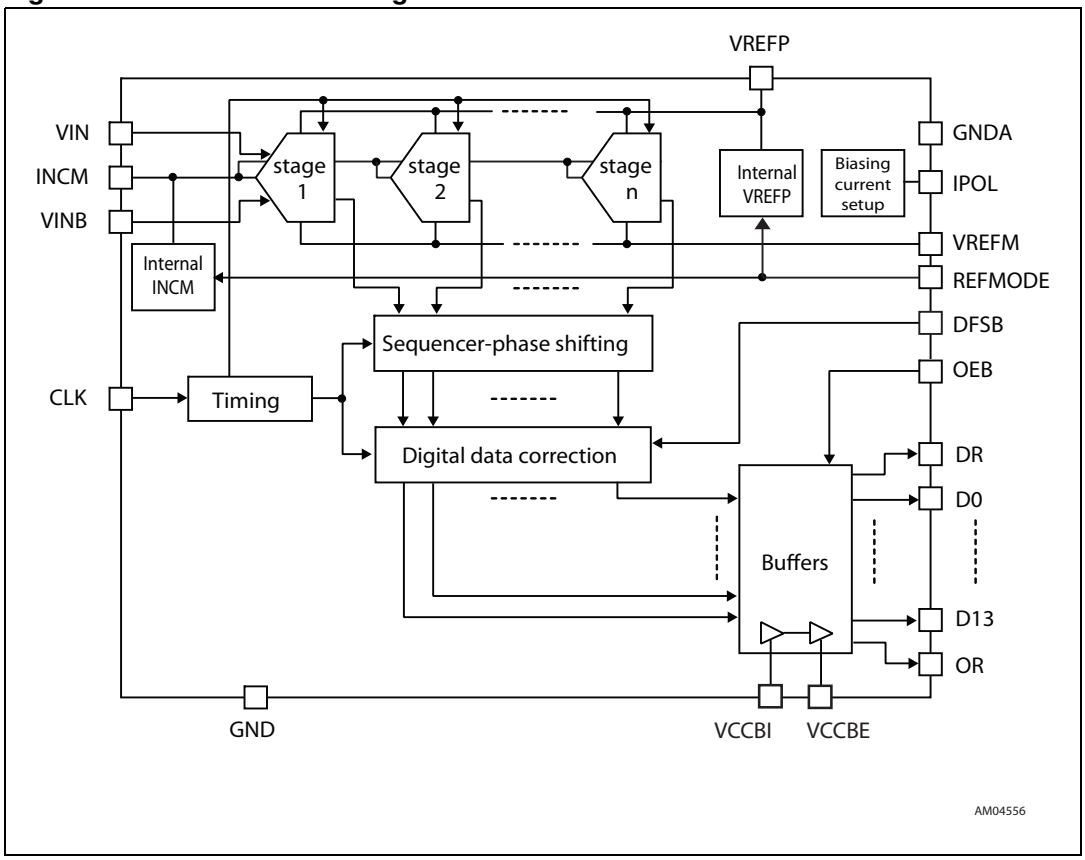
Figure 1. RHF1401 block diagram . . . 7
Figure 2. pin connections (top view) . . . 8
Figure 3. Analog inputs . . . 10
Figure 4. Output buffers . . . 10
Figure 5. Clock input . . . 10
Figure 6. Data format input . . . 10
Figure 7. Reference mode control input . . . 10
Figure 8. Output enable input . . . 10
Figure 9. VREFP and INCM input/output . . . 11
Figure 10. VREFM input . . . 11
Figure 11. Timing diagram . . . 13
Figure 12. Differential configuration . . . 16
Figure 13. ENOB vs. input frequency . . . 17
Figure 14. SINAD vs. input frequency . . . 17
Figure 15. THD vs. input frequency . . . 17
Figure 16. SNR vs. input frequency . . . 17
Figure 17. SFDR vs. input frequency . . . 17
Figure 18. Consumption vs. input frequency . . . 17
Figure 19. ENOB vs. sampling frequency . . . 18
Figure 20. SINAD vs. sampling frequency . . . 18
Figure 21. THD vs. sampling frequency . . . 18
Figure 22. SNR vs. sampling frequency . . . 18
Figure 23. SFDR vs. sampling frequency . . . 18
Figure 24. Power consumption vs. sampling frequency . . . 18
Figure 25. ENOB vs. VREFP . . . 19
Figure 26. SINAD vs. VREFP . . . 19
Figure 27. SNR vs. VREFP . . . 19
Figure 28. THD vs. VREFP . . . 19
Figure 29. ENOB vs. sine clock, diff. input . . . 19
Figure 30. Clock threshold vs. temperature . . . 19
Figure 31. ENOB vs. temperature . . . 20
Figure 32. Power consumption vs. temp . . . 20
Figure 33. DNL, differential input . . . 20
Figure 34. INL, differential input . . . 20
Figure 35. Single-ended input configuration . . . 21
Figure 36. ENOB vs. Fin, single-ended . . . 22
Figure 37. SINAD vs. Fin, single-ended . . . 22
Figure 38. THD vs. Fin, single-ended . . . 22
Figure 39. SNR vs. Fin, single-ended . . . 22
Figure 40. SFDR vs. Fin, single-ended . . . 22
Figure 41. Power consumption vs. Fin . . . 22
Figure 42. ENOB vs. Vin, Fin 1 kHz, Vrefp = 0.8 V . . . 23
Figure 43. ENOB vs Vin, Fin = 2 MHz, Vrefp = 0.8 V . . . 23
Figure 44. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.0 V . . . 23
Figure 45. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.0 V . . . 23
Figure 46. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.2 V . . . 23
Figure 47. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.2 V . . . 23
Figure 48. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.4 V . . . 24

Figure 49. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.4 V . . . 24
Figure 50. Rpol values vs. $F_s$ . . . 25
Figure 51. Power consumption values vs. $F_s$ with internal references disabled . . . 26
Figure 52. Equivalent VIN - VINB (differential input) . . . 27
Figure 53. 2 $V_{pp}$ differential input . . . 28
Figure 54. Differential implementation using a balun . . . 28
Figure 55. Optimized single-ended configuration (DC coupling), external REFP . . . 29
Figure 56. AC-coupling single-ended input configuration . . . 30
Figure 57. AC-coupling single-ended input configuration for low frequencies . . . 30
Figure 58. Internal voltage reference setting . . . 31
Figure 59. External voltage reference setting . . . 32
Figure 60. Example with zeners . . . 32
Figure 61. Clock input schematic . . . 33
Figure 62. Output buffer fall time . . . 35
Figure 63. Output buffer rise time . . . 35
Figure 64. Ceramic SO-48 package mechanical drawing . . . 38

# 1 Description

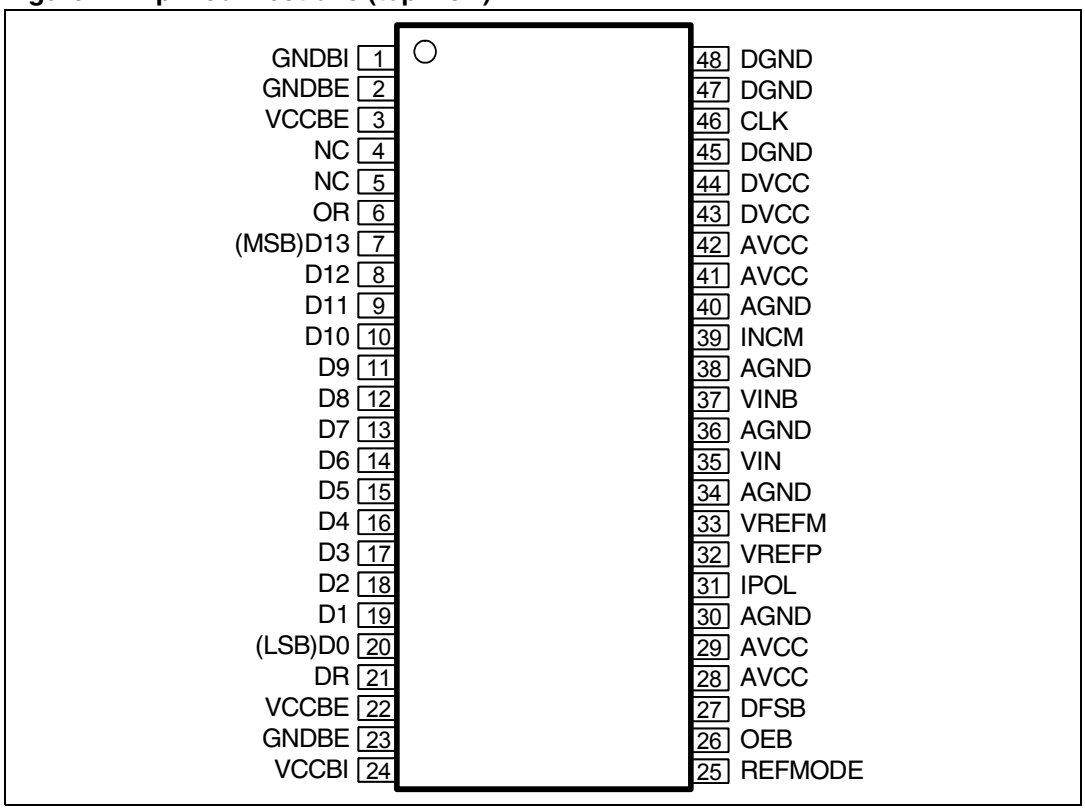
## 1.1 Block diagram

**Figure 1. RHF1401 block diagram**



## 1.2 Pin connections

**Figure 2. pin connections (top view)**



## 1.3 Pin descriptions

**Table 2. Pin descriptions**

| Pin | Name | Description | Observations | Pin | Name | Description | Observations |
|---|---|---|---|---|---|---|---|
| 1 | GNDBI | Digital buffer ground | 0 V | 25 | REFMODE | Ref. mode control input | 2.5 V/3.3 V CMOS input |
| 2 | GNDBE | Digital buffer ground | 0 V | 26 | OEB | Output enable input | 2.5 V/3.3 V CMOS input |
| 3 | VCCBE | Digital buffer power supply | 2.5 V/3.3 V | 27 | DFSB | Data format select input | 2.5 V/3.3 V CMOS input |
| 4 | | NC | Not connected to the dice | 28 | AVCC | Analog power supply | 2.5 V |
| 5 | | NC | Not connected to the dice | 29 | AVCC | Analog power supply | 2.5 V |
| 6 | OR | Out of range output | CMOS output (2.5 V/3.3 V) | 30 | AGND | Analog ground | 0 V |
| 7 | D13(MSB) | Most significant bit output | CMOS output (2.5 V/3.3 V) | 31 | IPOL | Analog bias current input | |
| 8 | D12 | Digital output | CMOS output (2.5 V/3.3 V) | 32 | VREFP | Top voltage reference | Can be external or internal |
| 9 | D11 | Digital output | CMOS output (2.5 V/3.3 V) | 33 | VREFM | Bottom voltage reference | 0 V |
| 10 | D10 | Digital output | CMOS output (2.5 V/3.3 V) | 34 | AGND | Analog ground | 0 V |
| 11 | D9 | Digital output | CMOS output (2.5 V/3.3 V) | 35 | VIN | Analog input | 1 $V_{pp}$ |
| 12 | D8 | Digital output | CMOS output (2.5 V/3.3 V) | 36 | AGND | Analog ground | 0 V |
| 13 | D7 | Digital output | CMOS output (2.5 V/3.3 V) | 37 | VINB | Inverted analog input | 1 $V_{pp}$ |
| 14 | D6 | Digital output | CMOS output (2.5 V/3.3 V) | 38 | AGND | Analog ground | 0 V |
| 15 | D5 | Digital output | CMOS output (2.5 V/3.3 V) | 39 | INCM | Input common mode | Can be external or internal |
| 16 | D4 | Digital output | CMOS output (2.5 V/3.3 V) | 40 | AGND | Analog ground | 0 V |
| 17 | D3 | Digital output | CMOS output (2.5V /3.3 V) | 41 | AVCC | Analog power supply | 2.5 V |
| 18 | D2 | Digital output | CMOS output (2.5 V/3.3 V) | 42 | AVCC | Analog power supply | 2.5 V |
| 19 | D1 | Digital output | CMOS output (2.5 V/3.3 V) | 43 | DVCC | Digital power supply | 2.5 V |
| 20 | D0(LSB) | Digital output LSB | CMOS output (2.5 V/3.3 V) | 44 | DVCC | Digital power supply | 2.5 V |
| 21 | DR | Data ready output(1) | CMOS output (2.5 V/3.3 V) | 45 | DGND | Digital ground | 0 V |
| 22 | VCCBE | Digital buffer power supply | 2.5 V/3.3 V | 46 | CLK | Clock input | 2.5 V compatible CMOS input |
| 23 | GNDBE | Digital buffer ground | 0 V | 47 | DGND | Digital ground | 0 V |
| 24 | VCCBI | Digital buffer power supply | 2.5 V | 48 | DGND | Digital ground | 0 V |

1. See load considerations in *Section 2.2: Timing characteristics*.

## 1.4 Equivalent circuits

**Figure 3. Analog inputs**

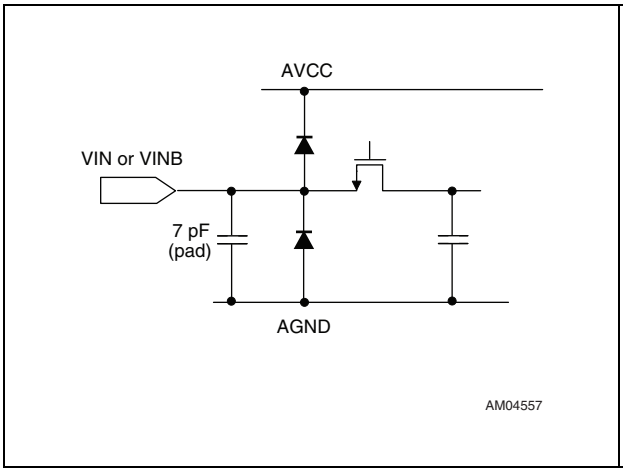



**Figure 4. Output buffers**

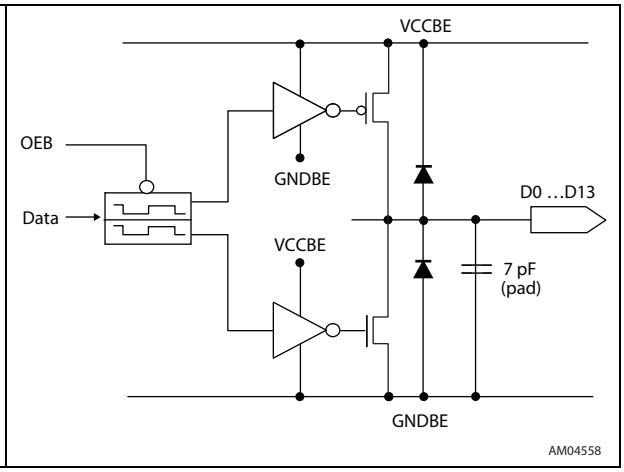



**Figure 5. Clock input**

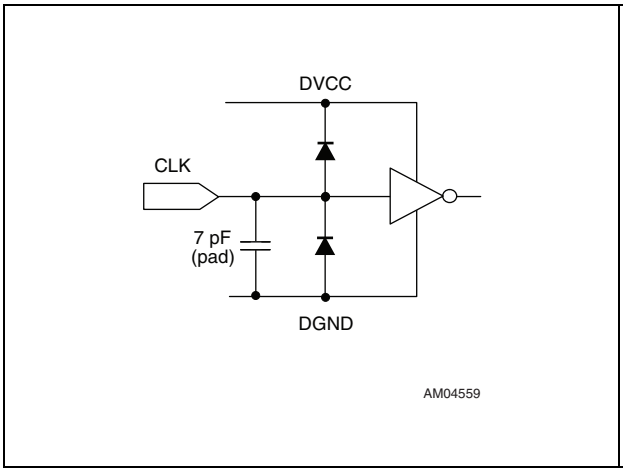



**Figure 6. Data format input**

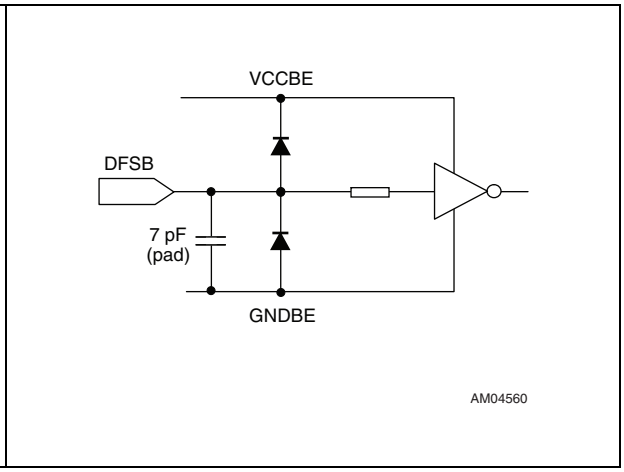



**Figure 7. Reference mode control input**

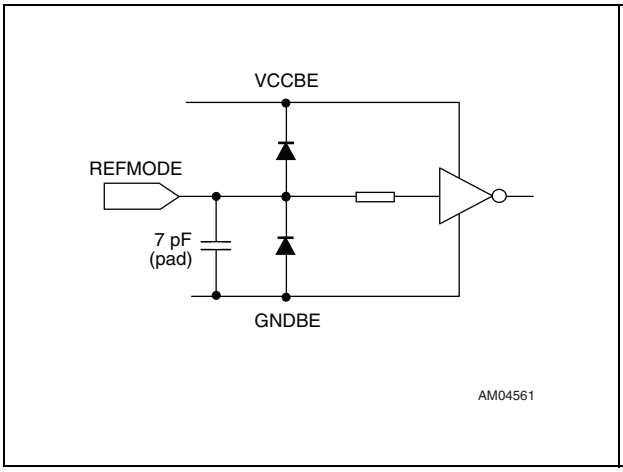



**Figure 8. Output enable input**

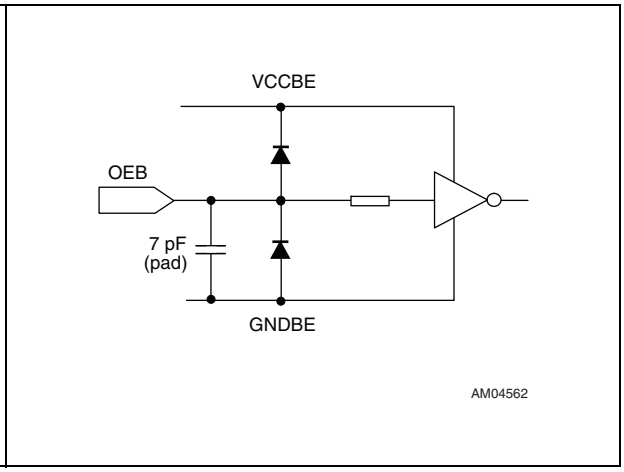


**Figure 9. VREFP and INCM input/output**

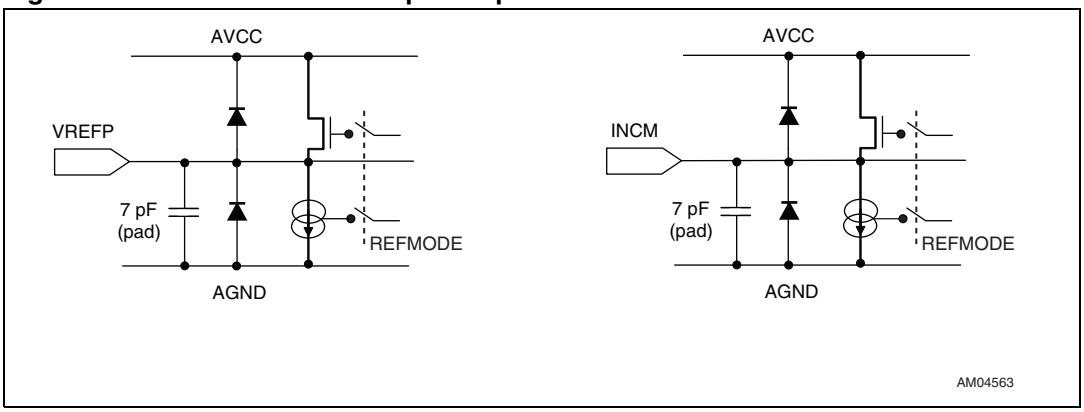
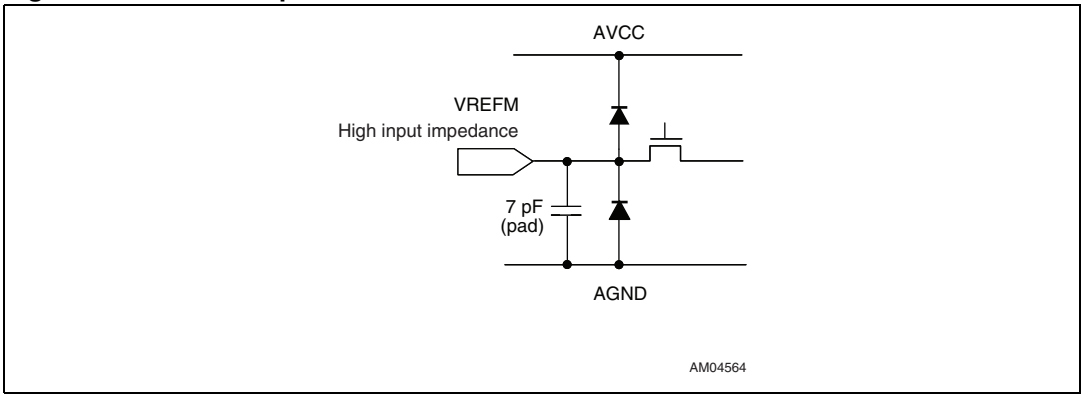



**Figure 10. VREFM input**



# 2 Electrical characteristics

## 2.1 Absolute maximum ratings and operating conditions

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | 3.3 | V |
| $DV_{CC}$ | Digital supply voltage | 3.3 | V |
| $V_{CCBI}$ | Digital buffer supply voltage | 3.3 | V |
| $V_{CCBE}$ | Digital buffer supply voltage | 3.6 | V |
| $V_{IN}$ $V_{INB}$ | Analog inputs: bottom limit ⇒ top limit | -0.6 V ⇒ $AV_{CC}$+0.6 V | V |
| $V_{REFP}$ $V_{INCM}$ | External references: bottom limit ⇒ top limit | -0.6 V ⇒ $AV_{CC}$+0.6 V | V |
| $I_{Dout}$ | Digital output current | -100 to 100 | mA |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $R_{thjc}$ | Thermal resistance junction to case | 22 | °C/W |
| $R_{thja}$ | Thermal resistance junction to ambient | 125 | °C/W |
| ESD | HBM (human body model)(1) | 2 | kV |

1. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

**Table 4. Operating conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | 2.3 | 2.5 | 2.7 | V |
| $DV_{CC}$ | Digital supply voltage | 2.3 | 2.5 | 2.7 | V |
| $V_{CCBI}$ | Digital internal buffer supply | 2.3 | 2.5 | 2.7 | V |
| $V_{CCBE}$ | Digital output buffer supply | 2.3 | 2.5 | 3.4 | V |
| $V_{REFP}$ | Forced top voltage reference | 0.7 | 1 | 1.4 | V |
| $V_{REFM}$ | Bottom external reference voltage | 0 | 0 | 0.5 | V |
| $V_{INCM}$ | Forced common mode voltage | 0.2 | 0.5 | 1.1 | V |
| $V_{IN}$ or $V_{INB}$ | Max. voltage versus GND | | 1 | 1.6(1) | V |
| | Min. voltage versus GND | -0.2 | GND | | V |
| DFSB | Digital inputs | 0 | | $V_{CCBE}$ | V |
| REFMODE | | | | | |
| OEB | | | | | |

1. See *Figure 25.* for differential input and *Figure 42.* to *Figure 49.* for single-ended.

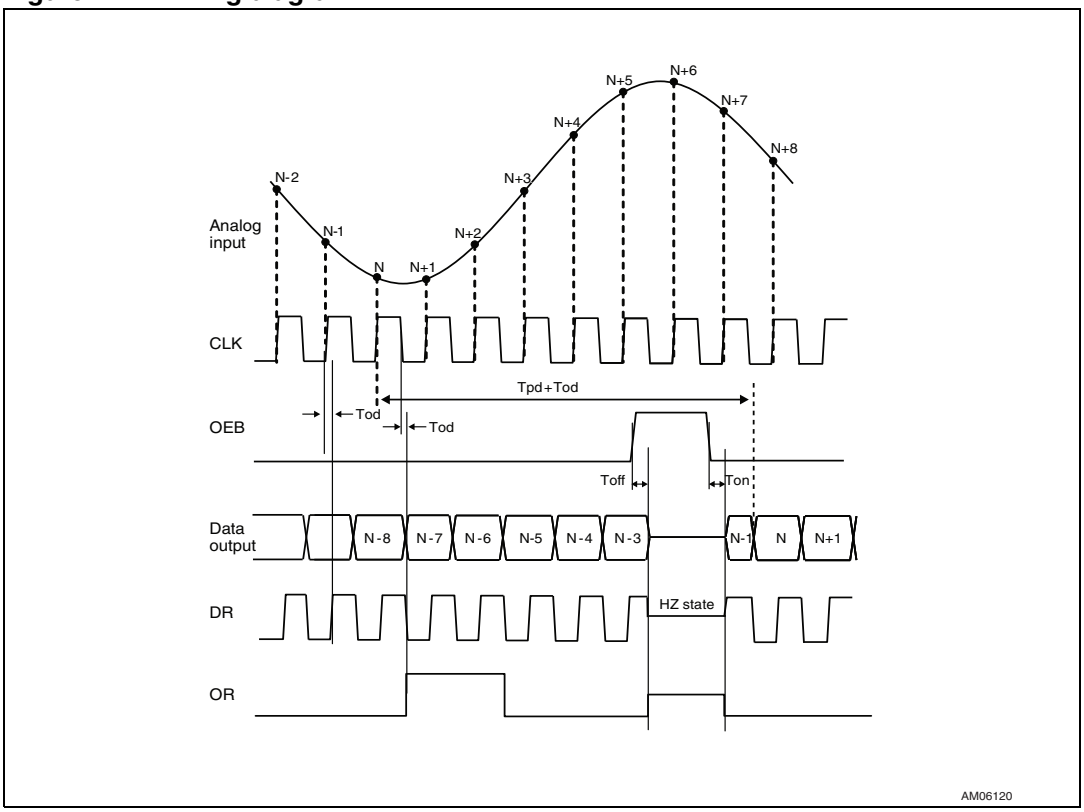
## 2.2 Timing characteristics

**Table 5. Timing characteristics**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC | Clock duty cycle | $F_s$ = 20 Msps | 45 | 50 | 65 | % |
| $T_{od}$ | Data output delay (fall of clock to data valid) (1) | 10 pF load capacitance | 5 | 7.5 | 13 | ns |
| $T_{pd}$ | Data pipeline delay(2) | Duty cycle = 50% | 7.5 | 7.5 | 7.5 | cycles |
| $T_{on}$ | Falling edge of OEB to digital output valid data | | | 1 | | ns |
| $T_{off}$ | Rising edge of OEB to digital output tri-state | | | 1 | | ns |
| $T_{rD}$ | Data rising time | 10 pF load capacitance | | 6 | | ns |
| $T_{fD}$ | Data falling time | 10 pF load capacitance | | 3 | | ns |

1. As per *Figure 11*.
2. If the duty cycle does not equal 50%: $T_{pd}$ = 7 cycles + CLK pulse width.

**Figure 11. Timing diagram**




The input signal is sampled on the rising edge of the clock while the digital outputs are synchronized on the falling edge of the clock. The duty cycles on DR and CLK are the same.

The rising and falling edges of the OR pin are synchronized with the falling edge of the DR pin.

## 2.3 Electrical characteristics (after 300 kRad)

Unless otherwise specified, the test conditions in the following tables are:
AVCC = DVCC = VCCBI =VCCBE = 2.5 V, $F_s$=20 Msps, $F_{IN}$= 15 MHz, $V_{IN}$ at -1 dBFS, VREFP = 1 V, INCM = 0.5 V, VREFM = 0 V, $T_{amb}$ = 25 °C.

**Table 6. Analog inputs**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$-$V_{INB}$ | Full-scale reference voltage (FS)(1) | VREFP = 1 V (forced) VREFM = 0 V | | 2 | | $V_{pp}$ |
| $C_{IN}$ | Input capacitance | | | 7 | | pF |
| $Z_{IN}$ | Input impedance | $F_s$ = 20 Msps | | 3.3 | | kΩ |
| ERB | Effective resolution bandwidth(1) | | | 70 | | MHz |

1. See *Section 4: Definitions of specified parameters* for more information.

**Table 7. Internal reference voltage**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{out}$ | Output resistance of internal reference | REFMODE = 0 internal reference on | | 30 | | Ω |
| | | REFMODE = 1 internal reference off | | 7.5 | | kΩ |
| $V_{REFP}$ | Top internal reference voltage | REFMODE = 0 | 0.76 | 0.84 | 0.95 | V |
| $V_{INCM}$ | Input common mode voltage | REFMODE = 0 | 0.40 | 0.44 | 0.50 | V |

**Table 8. External reference voltage(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFP}$ | Forced top reference voltage | REFMODE = 1 | 0.7 | | 1.4 | V |
| $V_{REFM}$ | Forced bottom ref voltage | REFMODE = 1 | 0 | | 0.5 | V |
| $V_{INCM}$ | Forced common mode voltage | REFMODE = 1 | 0.2 | | 1.1 | V |

1. See *Figure 59.*& *Figure 60*

**Table 9. Static accuracy**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DNL | Differential non-linearity(1) | $F_{in}$ = 1.5 Msps $V_{in}$ at +1 dBFS $F_s$ = 1.5 Msps | | ±0.4 | | LSB |
| INL | Integral non-linearity(2) | | | ±3 | | LSB |
| | Monotonicity and no missing codes | | Guaranteed | | | |

1. See *Figure 33* and *Section 4* for more information. This parameter is not tested.
2. See *Figure 34* and *Section 4* for more information. This parameter is not tested.

**Table 10. Digital inputs and outputs**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Clock input** | | | | | | |
| CT | Clock threshold | $DV_{CC}$ = 2.5 V | | 1.25 | | V |
| CA | Square clock amplitude (DC component = 1.25 V) | $DV_{CC}$ = 2.5 V | 0.8 | | 2.5 | Vpp |
| **Digital inputs** | | | | | | |
| $V_{IL}$ | Logic "0" voltage | $V_{CCBE}$ = 2.5 V | 0 | | 0.25 x $V_{CCBE}$ | V |
| $V_{IH}$ | Logic "1" voltage | $V_{CCBE}$ = 2.5 V | 0.75 x $V_{CCBE}$ | | $V_{CCBE}$ | V |
| **Digital outputs** | | | | | | |
| $V_{OL}$ | Logic "0" voltage | $I_{OL}$ = -10 µA | | 0 | 0.25 | V |
| $V_{OH}$ | Logic "1" voltage | $I_{OH}$ = 10 µA | $V_{CCBE}$ -0.25 | | | V |
| $I_{OZ}$ | High impedance leakage current | OEB set to $V_{IH}$ | -15 | | 15 | µA |
| $C_L$ | Output load capacitance | High CLK frequencies | | | 15 | pF |

**Table 11. Dynamic characteristics**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SFDR | Spurious free dynamic range | $F_{in}$ = 15 MHz<br>$F_s$ = 20 Msps<br>$V_{in}$ at -1 dBFS<br>internal references<br>$C_L$ = 6 pF | 70 | 91 | | dBFS |
| SNR | Signal to noise ratio | | 66 | 70 | | dB |
| THD | Total harmonic distortion | | 70 | 86 | | dB |
| SINAD | Signal to noise and distortion ratio | | 65 | 70 | | dB |
| ENOB | Effective number of bits | | 10.6 | 11.5 | | bits |

Higher values of SNR, SINAD and ENOB can be obtained by increasing the full-scale range of the analog input if the sampling frequency allows it.

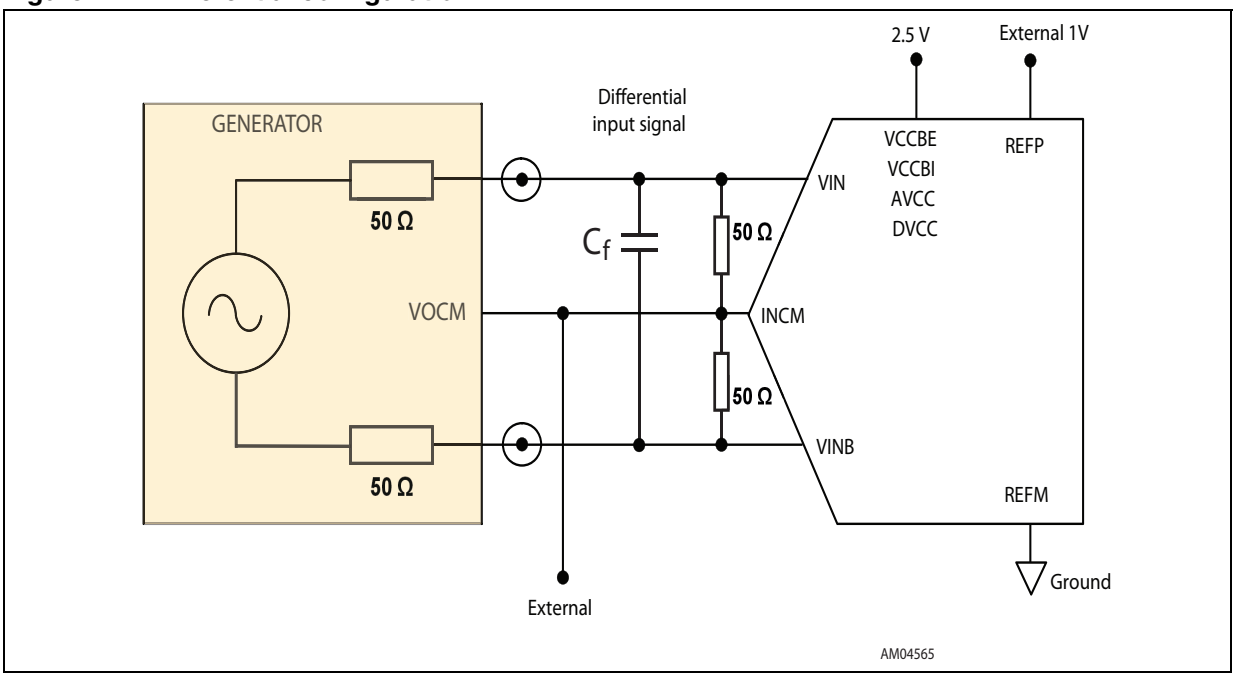
## 2.4 Results for differential input

### Setup

- AVCC = DVCC = VCCBI = VCCBE = 2.5V
- VREFP = 1 V
- VREFM = 0 V
- INCM = VREFP/2
- REFMODE = 1 (internal references are disabled)
- Vin = full scale - 0.3 dB
- Tamb = 25C°
- A square clock is applied

Unless other test conditions are specified.

**Figure 12. Differential configuration**




$C_f$ is a filter capacitor to cut the HF noise. Its value is 10 nF for input frequencies equal to or below 20 kHz. The value of the capacitor is divided by two when the input frequency is multiplied by 2.

**Figure 13. ENOB vs. input frequency**

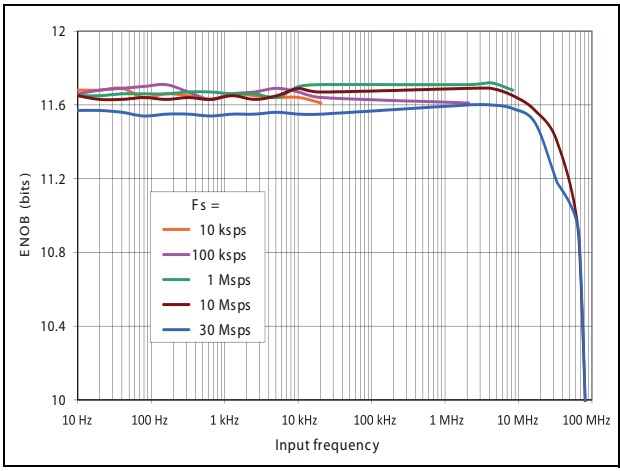



**Figure 14. SINAD vs. input frequency**

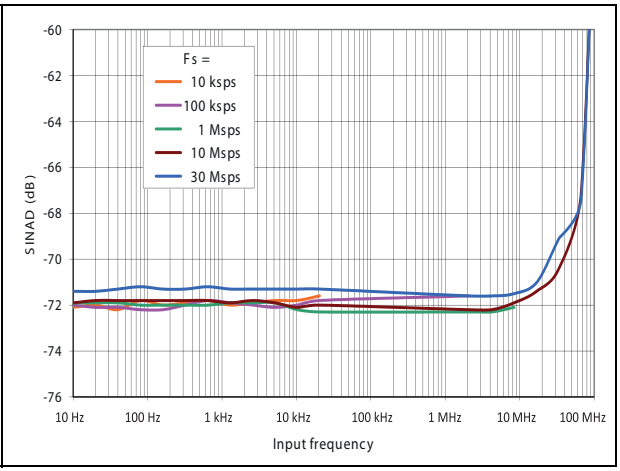



**Figure 15. THD vs. input frequency**

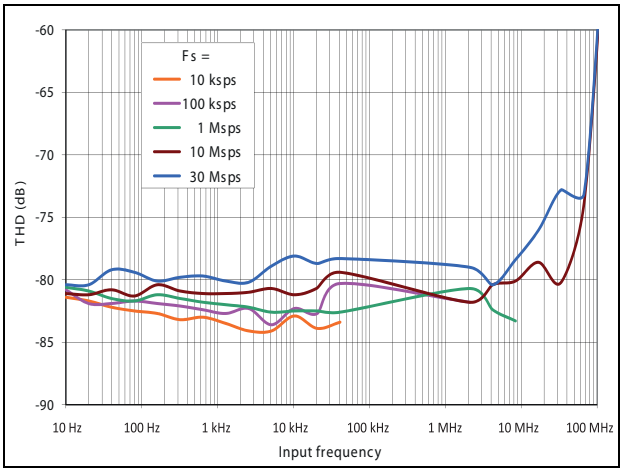



**Figure 16. SNR vs. input frequency**

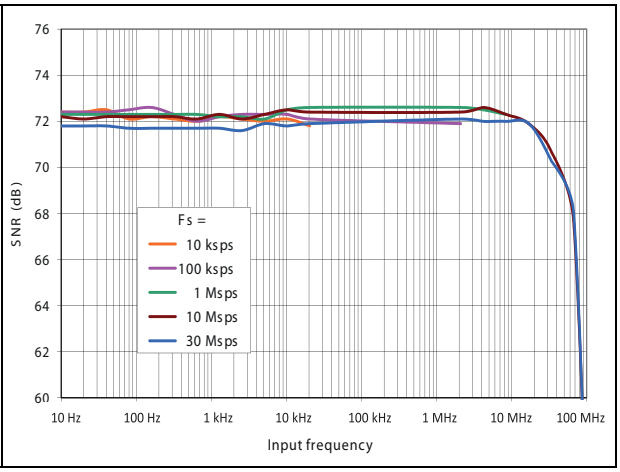



**Figure 17. SFDR vs. input frequency**

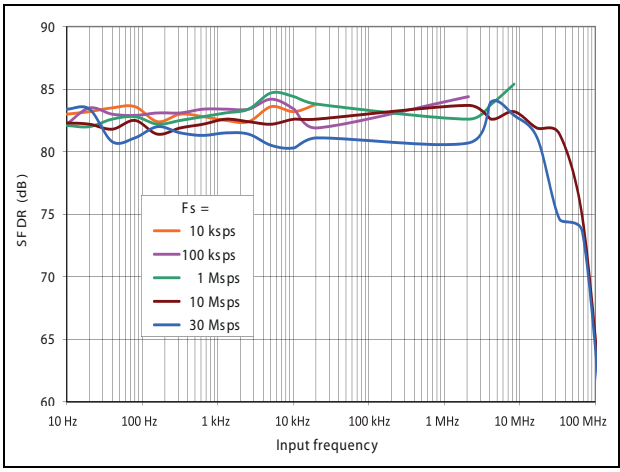



**Figure 18. Consumption vs. input frequency**

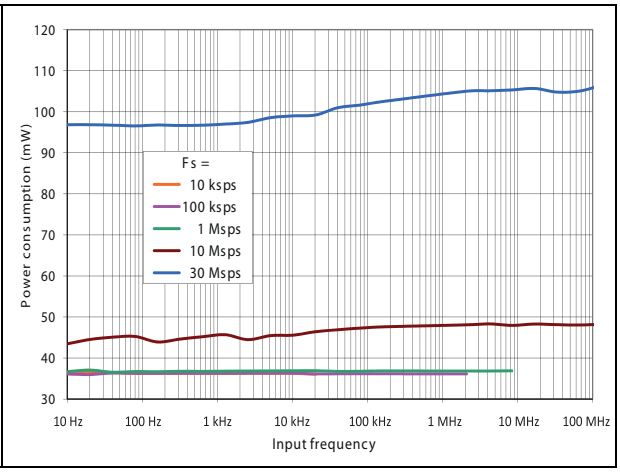


**Figure 19. ENOB vs. sampling frequency**

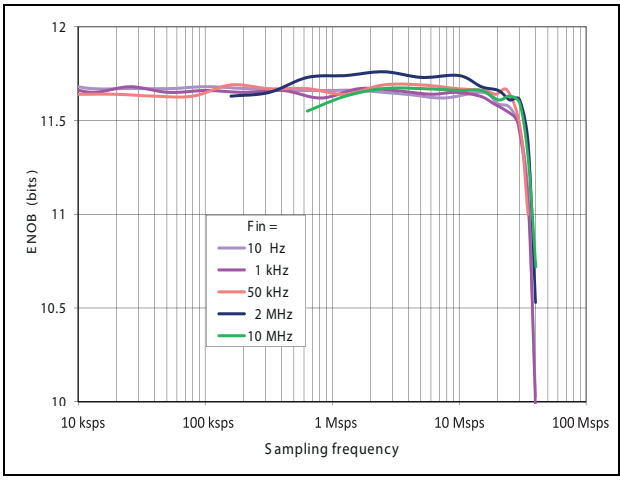



**Figure 20. SINAD vs. sampling frequency**

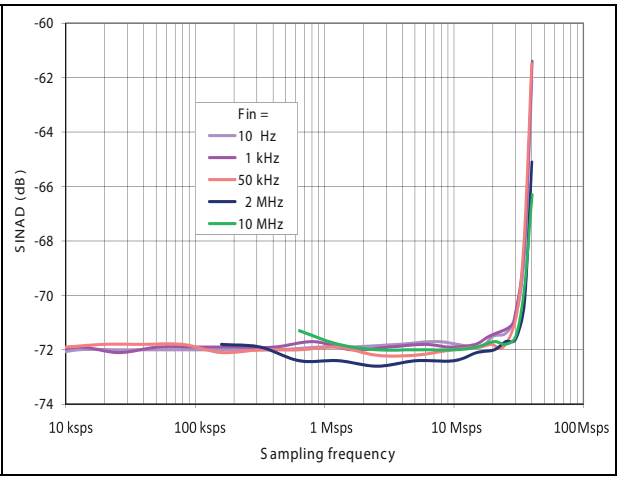



**Figure 21. THD vs. sampling frequency**

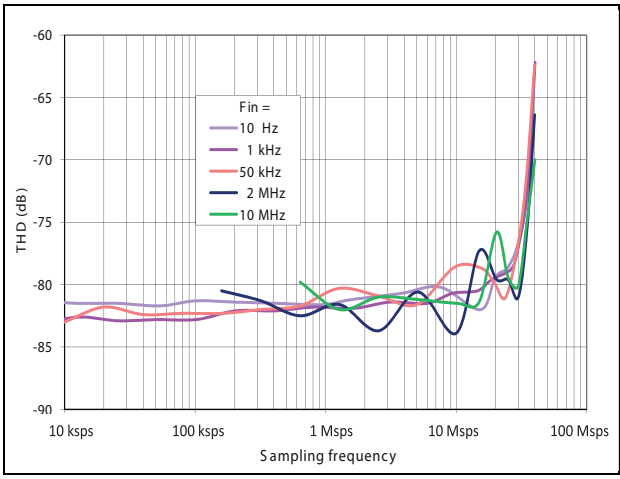



**Figure 22. SNR vs. sampling frequency**

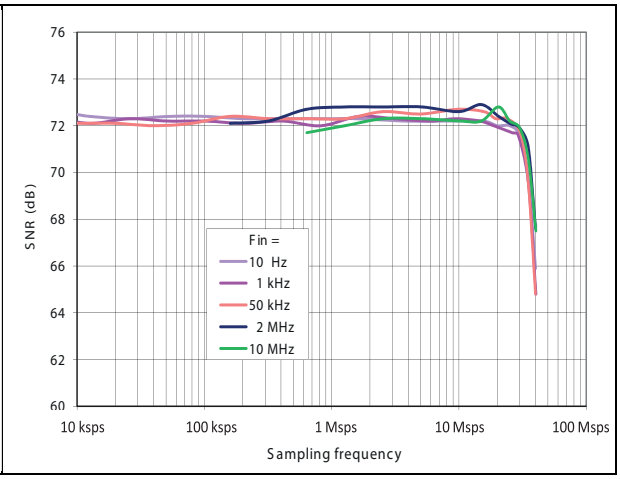



**Figure 23. SFDR vs. sampling frequency**

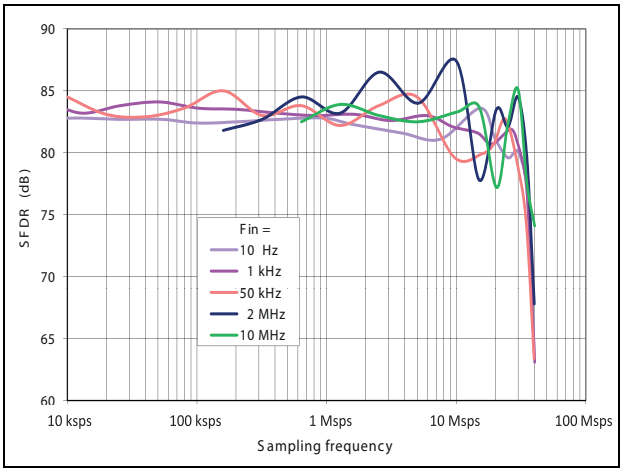



**Figure 24. Power consumption vs. sampling frequency**

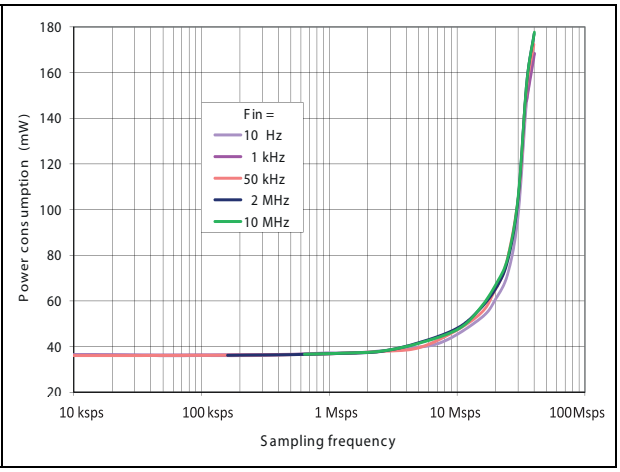


**Figure 25. ENOB vs. VREFP**

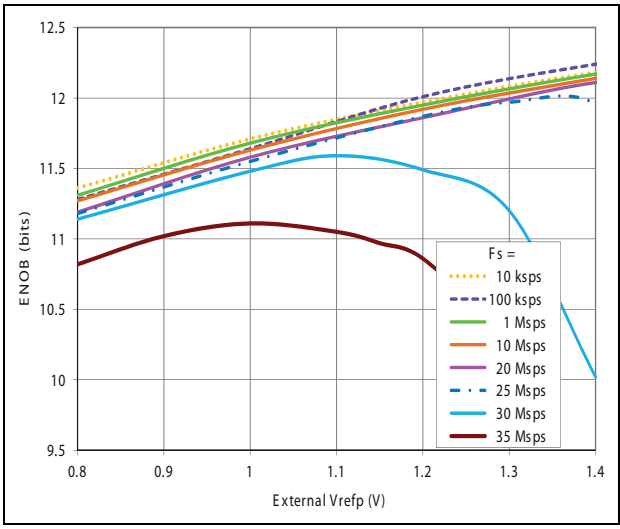



**Figure 26. SINAD vs. VREFP**

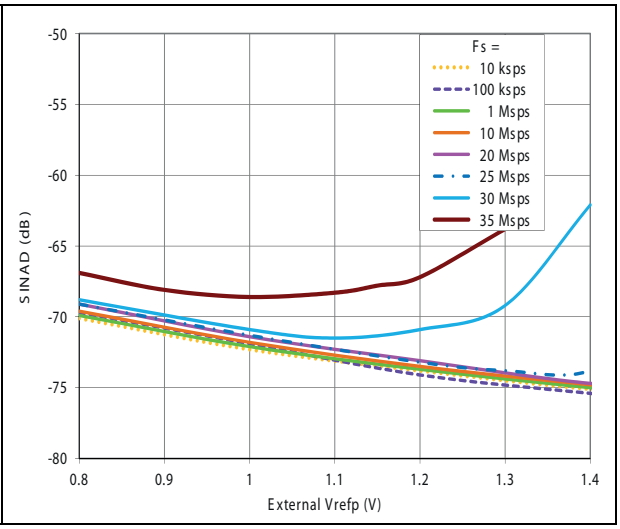



**Figure 27. SNR vs. VREFP**

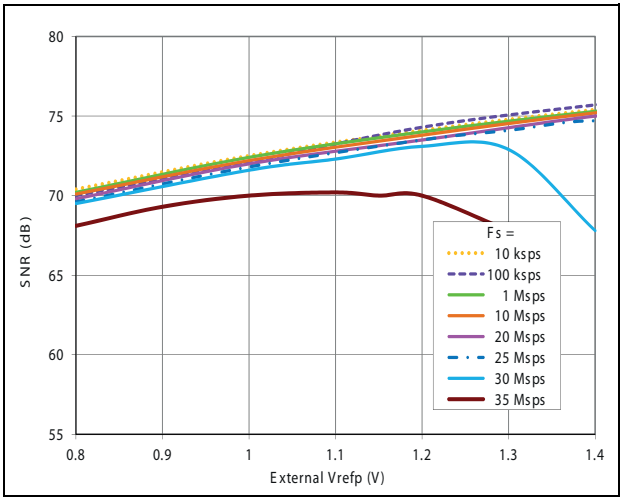



**Figure 28. THD vs. VREFP**

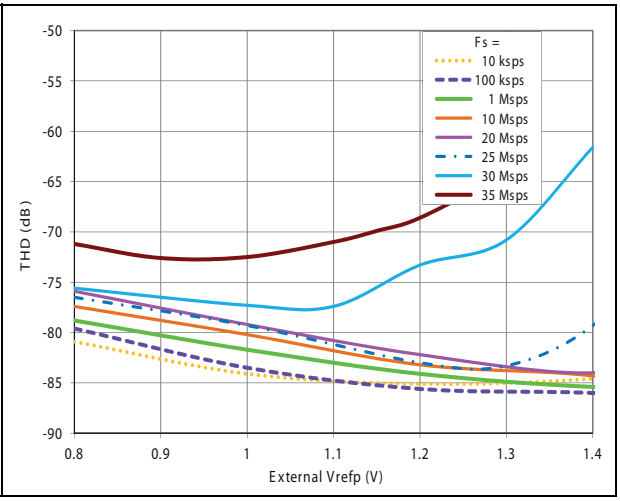



**Figure 29. ENOB vs. sine clock, diff. input**

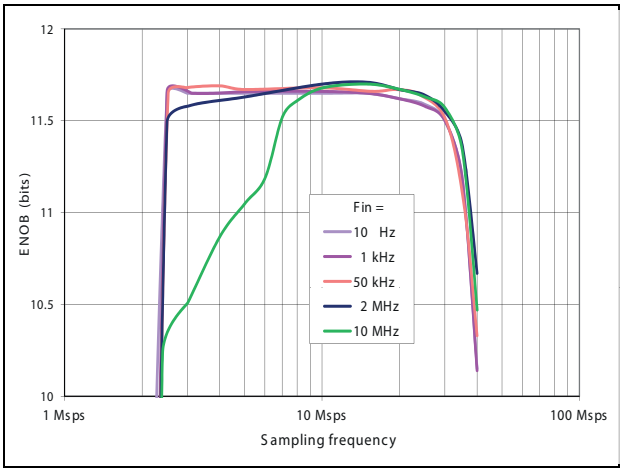



**Figure 30. Clock threshold vs. temperature**

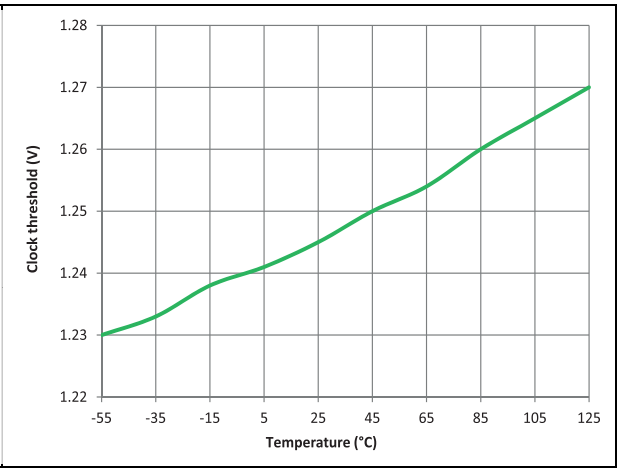


**Figure 31. ENOB vs. temperature**

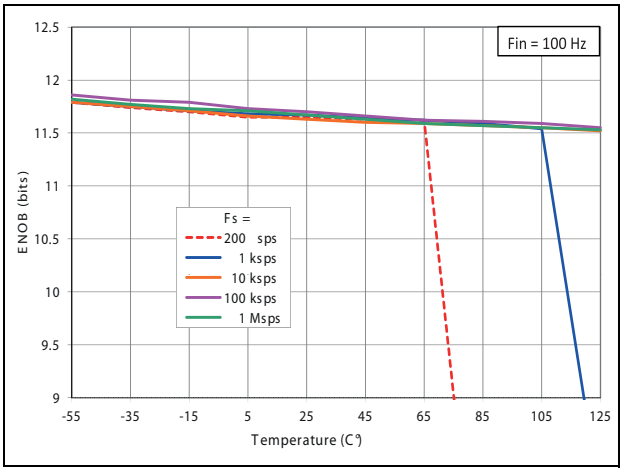



**Figure 32. Power consumption vs. temp.**

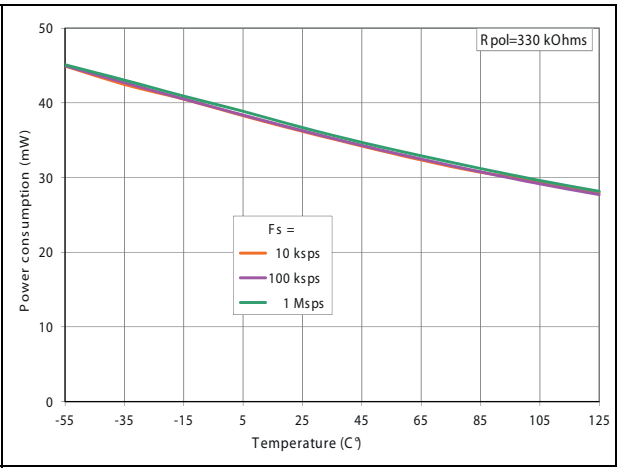



**Figure 33. DNL, differential input**

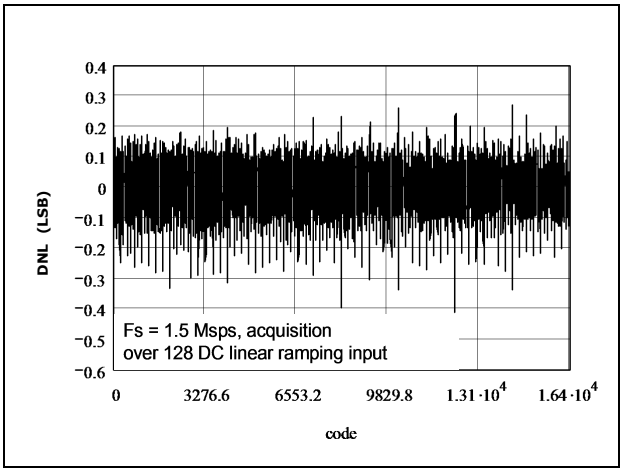
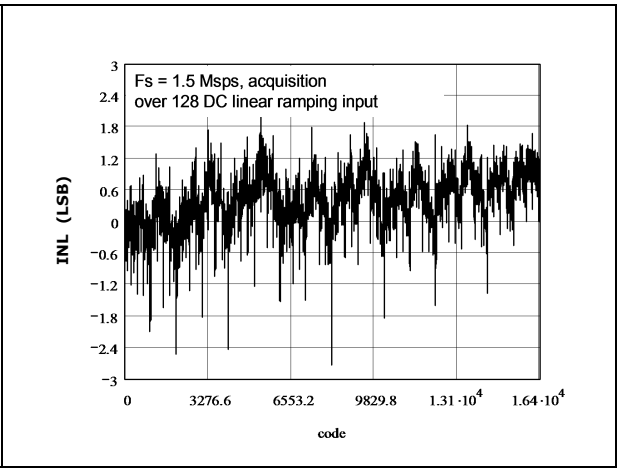



**Figure 34. INL, differential input**



## 2.5 Results for single ended input

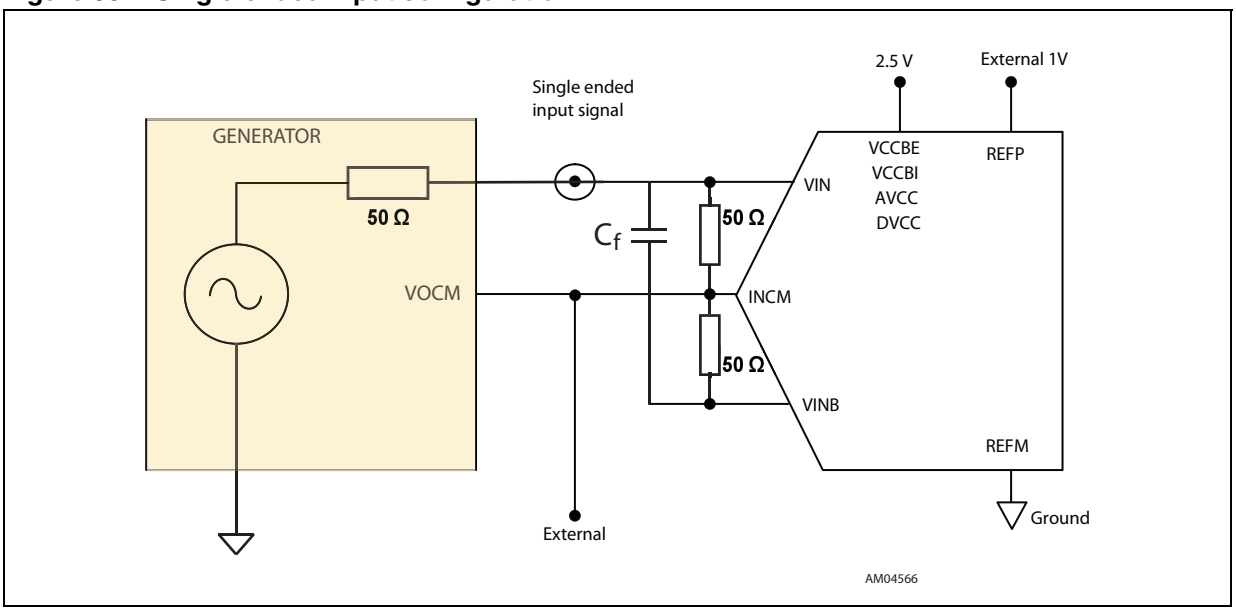
### Setup

- AVCC = DVCC = VCCBI = VCCBE = 2.5 V
- VREFP = 1 V
- VREFM = 0 V
- INCM = Vin/2
- REFMODE = 1 (internal references are disabled)
- Vin = 1 Vpp
- Tamb = 25 °C
- A square clock is applied

Unless other test conditions are specified.

In the following graphs, the input signal is seldom full scale.

**Figure 35. Single-ended input configuration**




$C_f$ is a filter capacitor to cut the HF noise. Its value is 10 nF for input frequencies equal to or below 20 kHz. The value of the capacitor is divided by two when the input frequency is multiplied by 2.

Figure 36. ENOB vs. Fin, single-ended

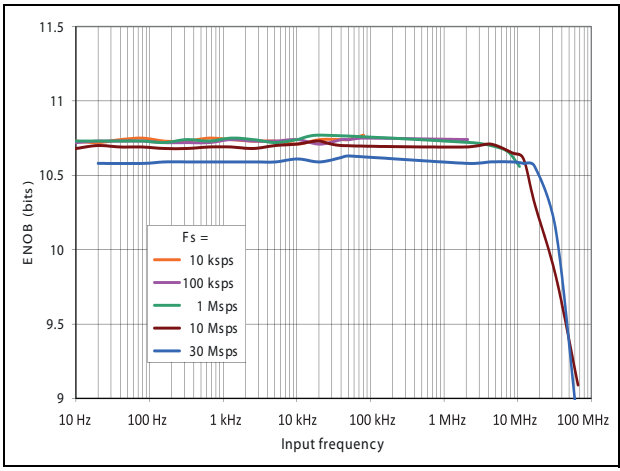



Figure 37. SINAD vs. Fin, single-ended

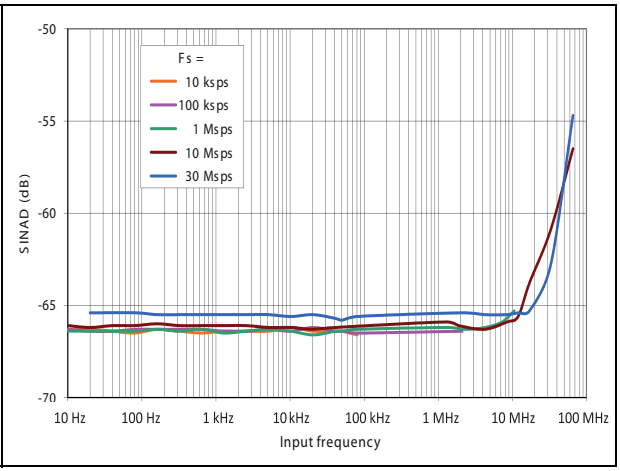



Figure 38. THD vs. Fin, single-ended

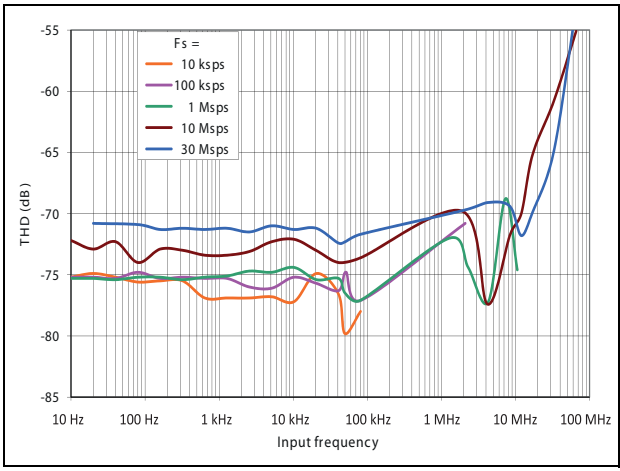



Figure 39. SNR vs. Fin, single-ended

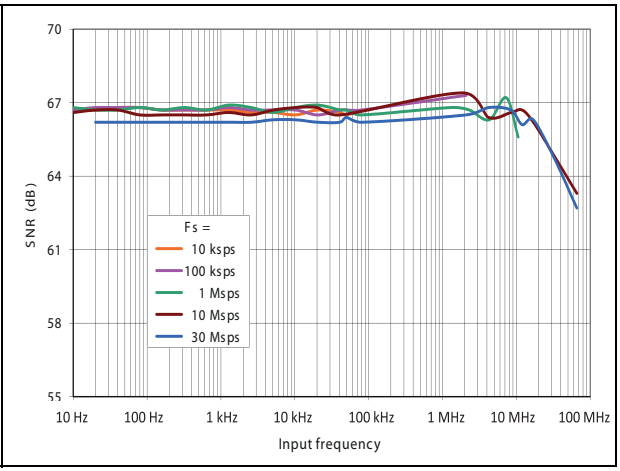



Figure 40. SFDR vs. Fin, single-ended

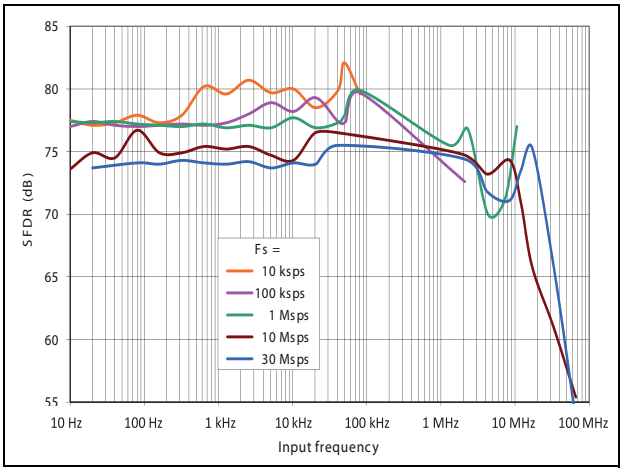



Figure 41. Power consumption vs. Fin

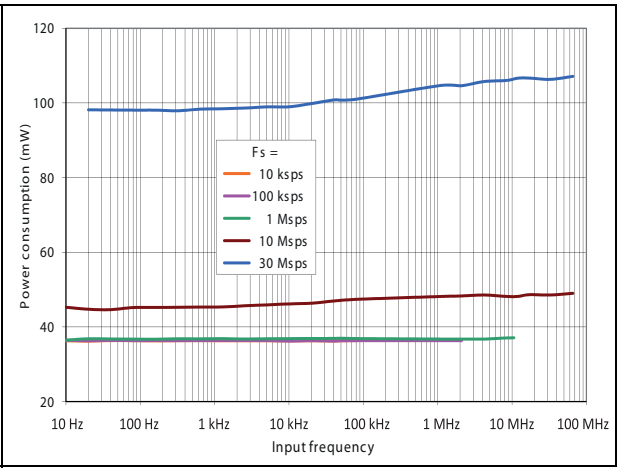


**Figure 42. ENOB vs. Vin, Fin 1 kHz, Vrefp = 0.8 V**

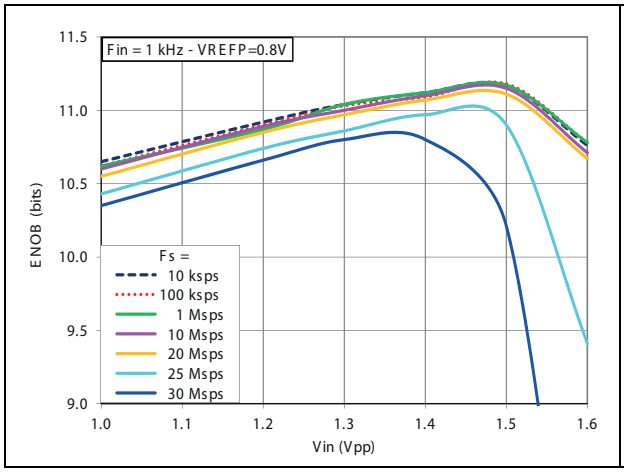



**Figure 43. ENOB vs Vin, Fin = 2 MHz, Vrefp = 0.8 V**

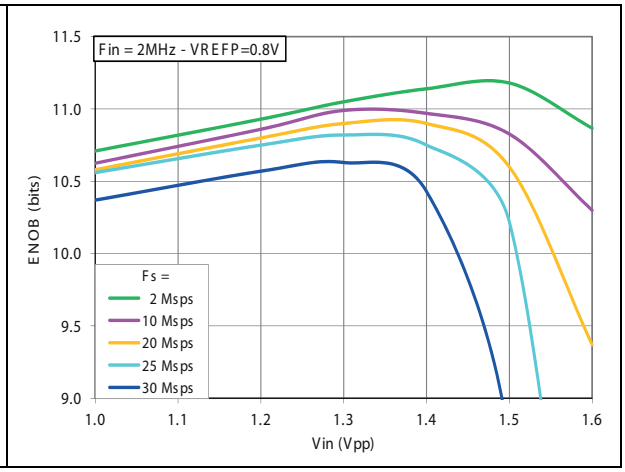



**Figure 44. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.0 V**

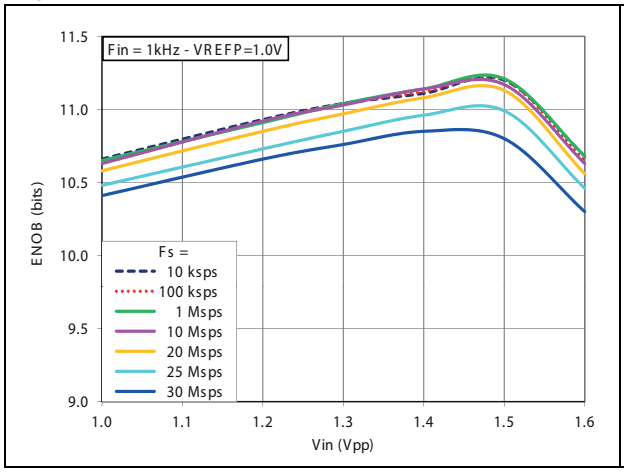



**Figure 45. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.0 V**

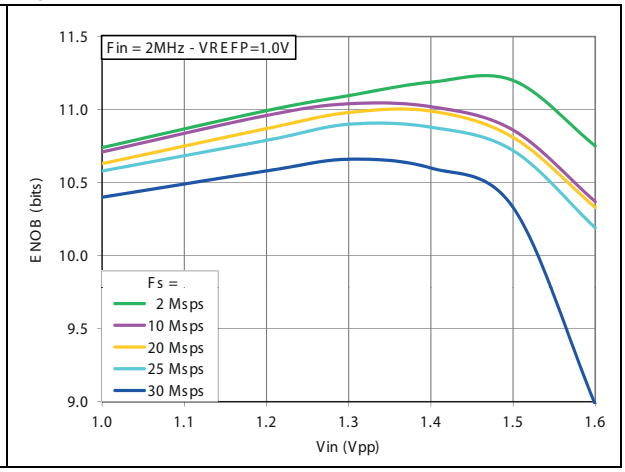



**Figure 46. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.2 V**

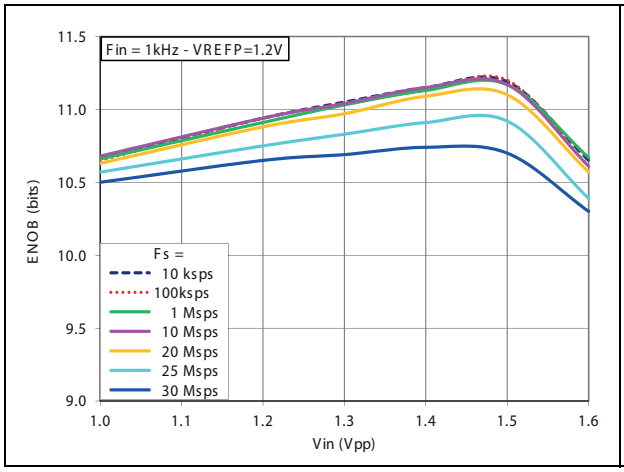



**Figure 47. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.2 V**

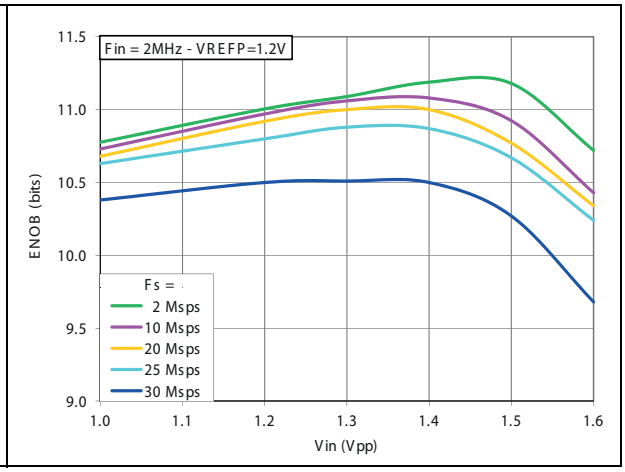


**Figure 48. ENOB vs. Vin, Fin 1 kHz, Vrefp = 1.4 V**

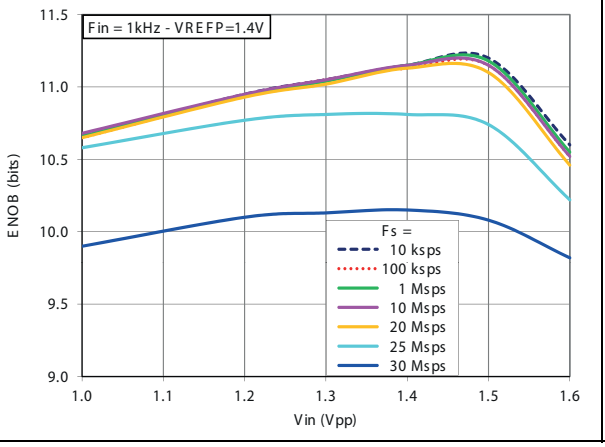
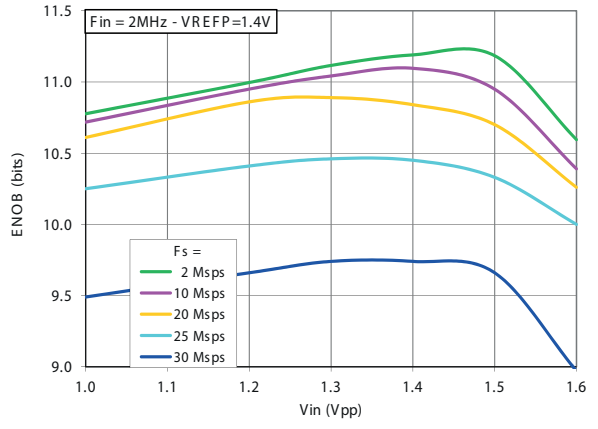



**Figure 49. ENOB vs Vin, Fin = 2 MHz, Vrefp = 1.4 V**



# 3 User manual

## 3.1 Optimizing the power consumption

The polarization current in the input stage is set by an external resistor ($R_{pol}$). When selecting the resistor value, it is possible to optimize the power consumption according to the sampling frequency of the application. For this purpose, an external $R_{pol}$ resistor is placed between the IPOL pin and the analog ground.

The values in *Figure 50* are achieved with VREFP = 1 V, VREFM = 0 V, INCM = 0.5 V and the input signal is 2 Vpp with a differential DC connection. If the conditions are changed, the Rpol resistor varies slightly.

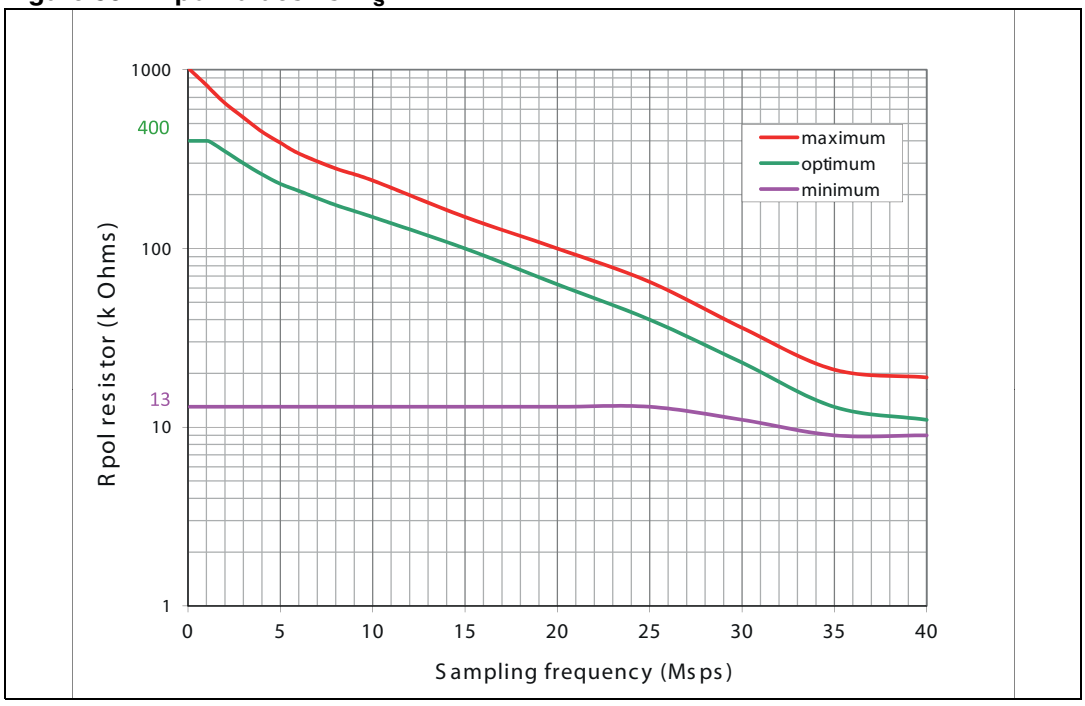
*Figure 50* shows the optimum Rpol resistor value to obtain the best ENOB value. It also shows the minimum and maximum values to get good results. ENOB decreases by approximately 0.2 dB when you change Rpol from optimum to maximum or minimum.

If Rpol is higher than the maximum value, there is not enough polarization current in the analog stage to obtain good results. If Rpol is below the minimum, THD increases significantly.

Therefore, the total dissipation can be adjusted across the entire sampling range to fulfill the requirements of applications where power saving is critical.

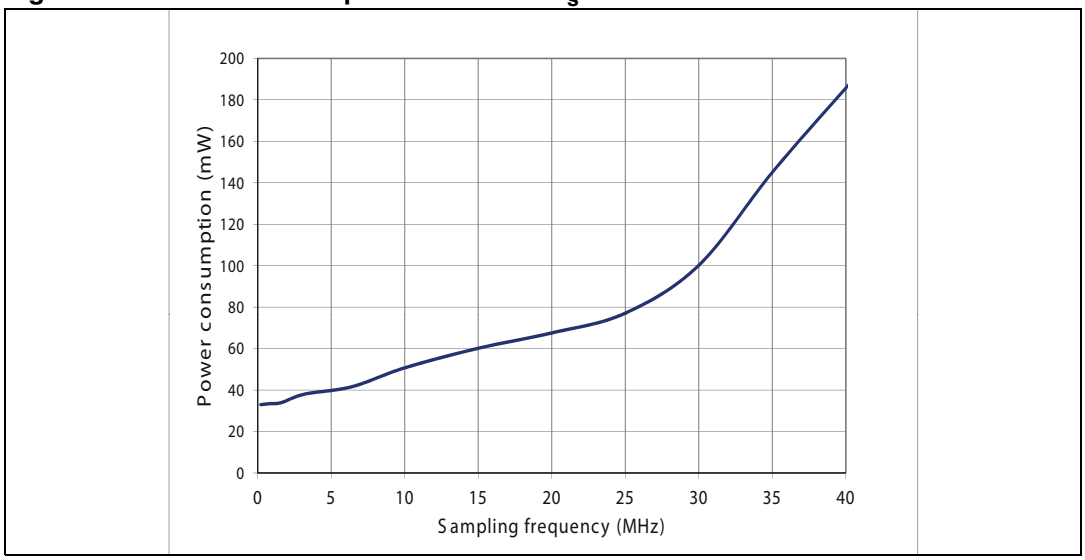
For sampling frequencies below 2 MHz, the optimum resistor value is approximately 400 kOhms.

**Figure 50. Rpol values vs. $F_s$**




The power consumption depends on the Rpol value and the sampling frequency. In *Figure 51*, it is shown with the internal references disabled (REFMODE = 1) and Rpol defined in *Figure 50* as the optimum.

**Figure 51. Power consumption values vs. $F_s$ with internal references disabled**



## 3.2 Driving the analog input

The input frequency can range from DC to tens of MHz.

The input stages (VIN and VINB) have a special design that limits the input amplitude. For each of them, the maximum input voltage is about 1.6 V for low sampling frequencies and less for high sampling frequencies. Low voltage is ground.

Consequently, the maximum input voltage read by the ADC for Single-ended mode is 1.6 V regardless of the VREFP and VREFM voltages.

### 3.2.1 Differential mode

The INCM value must be equal to the medium input voltage value.

In differential mode, high sampling limitation is seen in *Figure 25.*

For all input frequencies, it is mandatory to add a capacitor on the PCB (between VIN and VINB) to cut the HF noise. The lower the frequency, the higher the capacitor.

The full-scale range is twice the difference between Vrep and Vrefm.

**Figure 52. Equivalent VIN - VINB (differential input)**

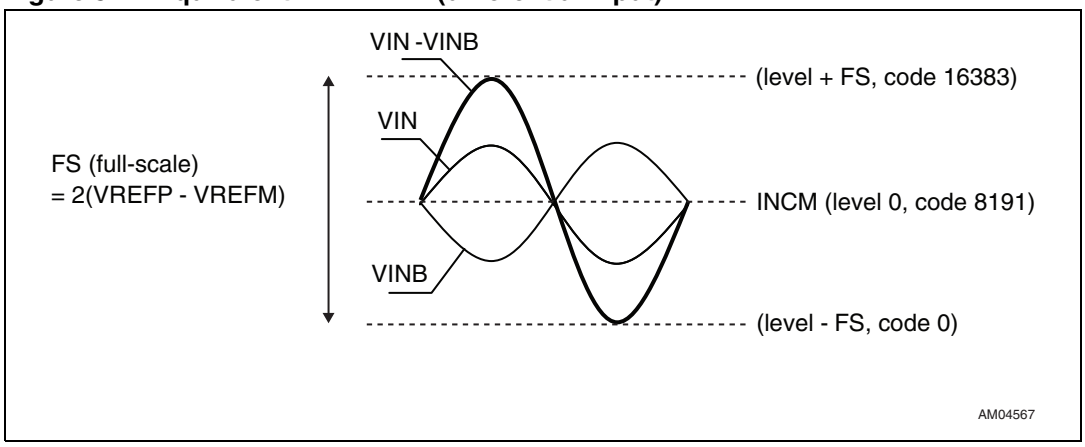



**Table 12. Differential mode output codes**

| Vin - Vinb = | DFSB = 1 | DFSB = 0 |
|---|---|---|
| + (VREFP-VREFM) | 3FFF | 1FFF |
| 0 | 1FFF | 3FFF |
| - (VREFP-VREFM) | 0000 | 2000 |

The RHF1401 is designed to obtain optimum performance when driven on differential inputs with a differential amplitude of two volts peak-to-peak (2 $V_{pp}$). This is the result of 1 $V_{pp}$ on the VIN and VINB inputs in phase opposition.

The RHF1401 is specifically designed to meet sampling requirements for intermediate frequency (IF) input signals. In particular, the track-and-hold in the first stage of the pipeline is designed to minimize the linearity limitations as the analog frequency increases.

**Figure 53. 2 $V_{pp}$ differential input**

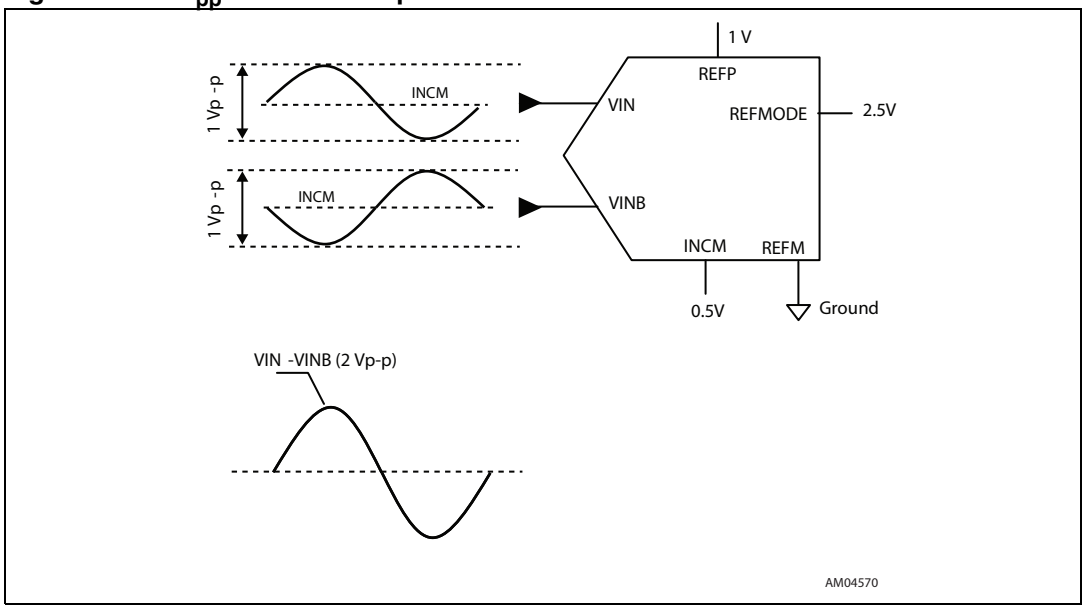
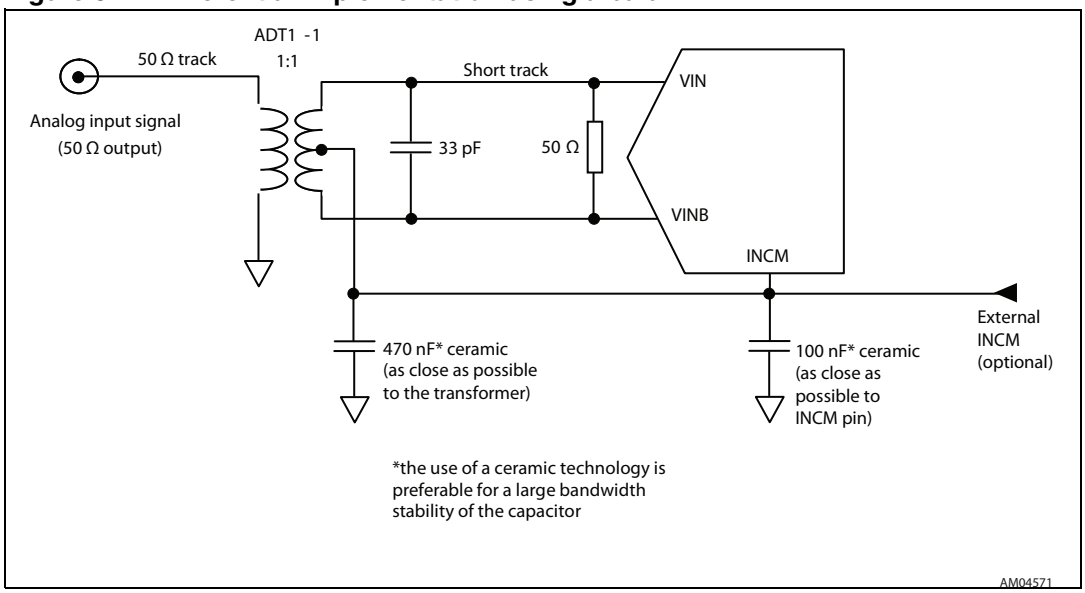



*Figure 54* shows a differential input solution. The input signal is fed to the transformer's primary, while the secondary drives both ADC inputs. The transformer must be matched with generator output impedance: 50 Ω in this case for proper matching with a 50 Ω generator. The tracks between the secondary and VIN and VINB pins must be as short as possible.

**Figure 54. Differential implementation using a balun**




The input common-mode voltage of the ADC (INCM) is connected to the center tap of the transformer's secondary in order to bias the input signal around the common voltage (see *Table 7: Internal reference voltage*).The INCM is decoupled to maintain a low noise level on this node. Ceramic technology for decoupling provides good capacitor stability across a wide bandwidth.

### 3.2.2 Single-ended mode

**Figure 55. Optimized single-ended configuration (DC coupling), external REFP**

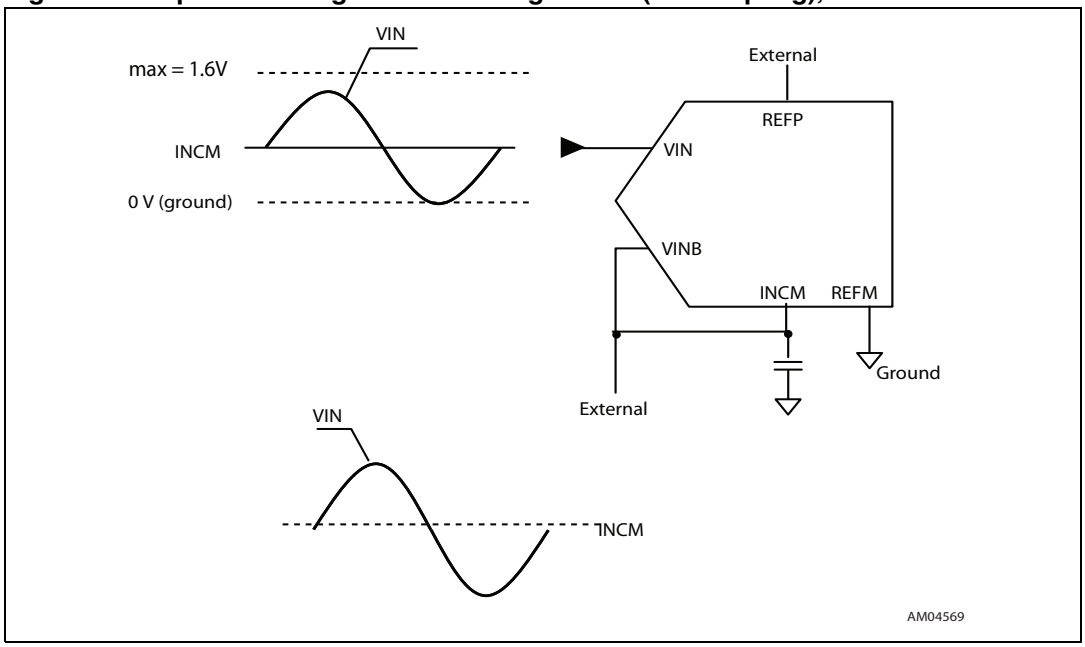



**Table 13. Single-ended mode output codes with Vinb = INCM**

| Vin = | DFSB = 1 | DFSB = 0 |
|---|---|---|
| INCM + (VREFP-VREFM) | 3FFF | 1FFF |
| INCM | 1FFF | 3FFF |
| INCM - (VREFP-VREFM) | 0000 | 2000 |

The RHF1401 is designed for use in a differential input configuration. Nevertheless, it can achieve good performance in a single-ended input configuration. In single-ended, performances depend on the input voltage, input frequency, voltage of references and sampling frequency (refer to *Figure 42.* to *Figure 49.*)

VREFP and INCM internal voltage references are not adapted to Single-ended mode.

Some applications may require a single-ended input, which can easily be achieved with the configuration shown in *Figure 56*, *Figure 57* for AC coupling or *Figure 35.* for DC coupling. However, with this type of configuration, a degradation in the rated performance of the RHF1401 may occur compared with a differential configuration. A sufficiently decoupled DC reference should be used to bias the RHF1401 inputs. An AC-coupled analog input can also be used and the DC analog level set with a high value resistor R (6 kΩ to 100 kΩ) connected to a proper DC source. Cin and R behave like a high-pass filter and are calculated to set the lowest possible cut-off frequency.

Each input is limited to about 1.6 V due to the CMOS transistor on the input path. Voltage can be a bit more or less than 1.6 V depending on temperature, AVCC, and variations from one die to another (see *Figure 3* for the analog input schematic). This “input limitation” is independent of the VREFP and VREFM values.

The OR pin should rise to 1 when the signal is out of range. However, when VREFP = 0.8 V, VREFM = 0 V, and input voltage max = 1.6 V, the ADC may not read the maximum input voltage due to the CMOS input transistor. Consequently, the OR pin does not rise to 1. To avoid this situation occurring, it is recommended to limit the input amplitude to 1.5 V, VREFP to 0.75 V, and VREFM to 0 V.

**Figure 56. AC-coupling single-ended input configuration**

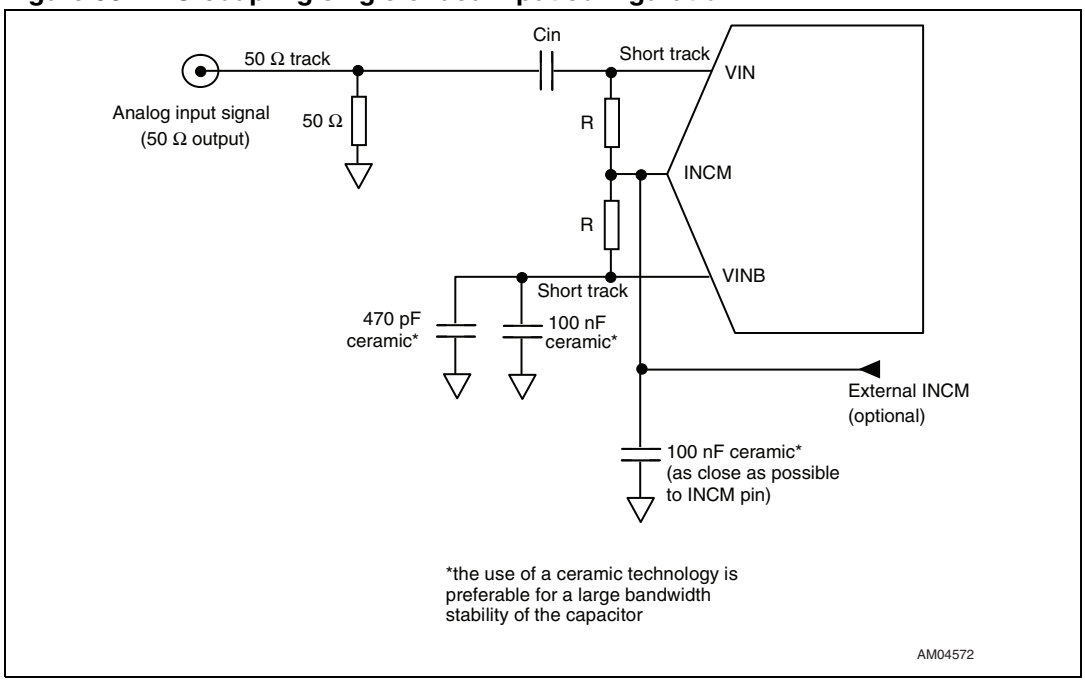
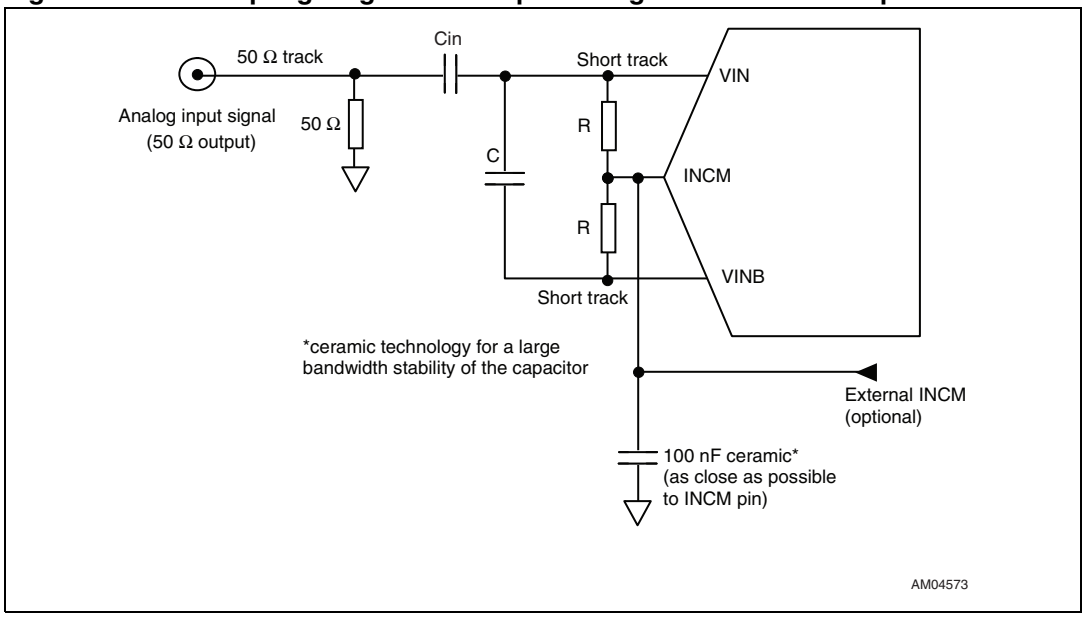



**Figure 57. AC-coupling single-ended input configuration for low frequencies**




The C capacitor is efficient in reducing noise at high frequencies. When coupled with the resistors, R and C together behave like a high-pass filter. For example, if R = 10 k and C = 33 pF, the cut-off frequency of this filter equals 482 kHz.

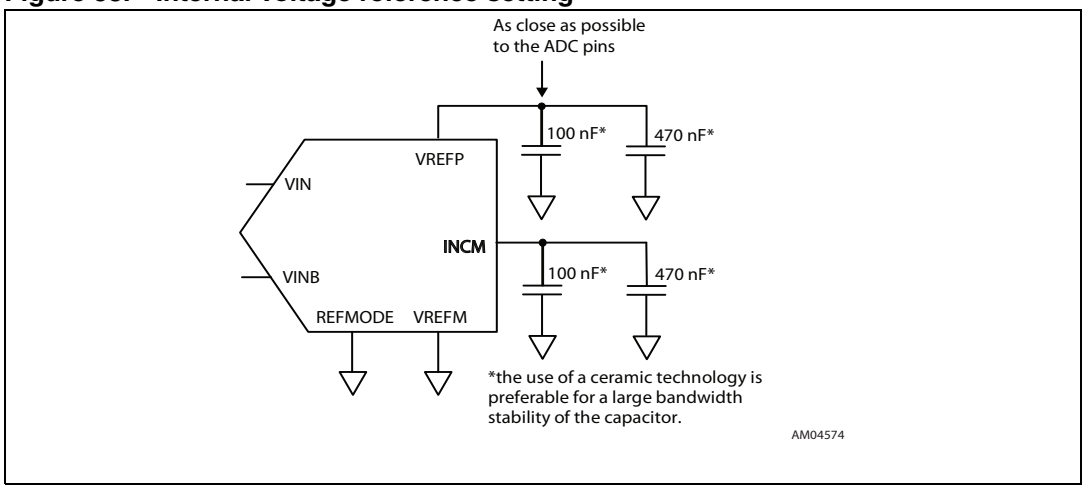
## 3.3 Reference connections

### 3.3.1 Internal voltage reference

In standard configuration, the ADC is biased with two internal voltage references: VREFP and INCM. They should be decoupled to minimize low and high frequency noise. When the REFMODE pin is set to 0 both internal voltage references are enabled and they can drive external components or be forced by an external value.

The VREFM pin has no internal reference and must be connected to a voltage reference. It is usually connected to the analog ground.

**Figure 58. Internal voltage reference setting**




### 3.3.2 External voltage reference

External voltage references can be used for specific applications requiring better linearity, enhanced temperature behavior, or different voltage values (see *Table 7: Internal reference voltage*). Internal voltage references are disabled when the REFMODE pin is equal to 1. In this case, external voltage references must be applied to the device.

External voltage references can be applied when internal voltage references are disabled or not.

When internal voltage reference are disabled, ADC consumption is about 13 mA less than when they are enabled.

The external voltage references with the configuration shown in *Figure 59* and *Figure 60* can be used to obtain optimum performance. Decoupling is achieved by using ceramic capacitors, which provide optimum linearity versus frequency.

**Figure 59. External voltage reference setting**

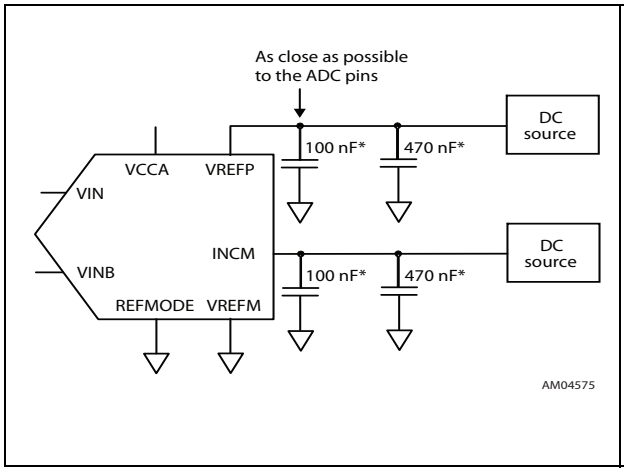
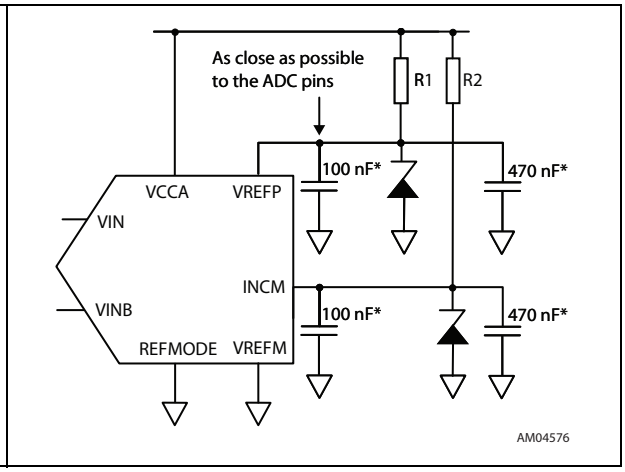



**Figure 60. Example with zeners**




*Note: *The use of ceramic technology is preferable to ensure large bandwidth stability of the capacitor.*

In multi-channel applications, the high impedance input (when REFMODE = 1) of the references allows one to drive several ADCs with only two voltage reference devices.

In Differential mode the voltage of the analog input common mode (INCM) should be around $V_{REFP}/2$. Higher levels introduce more distortion.

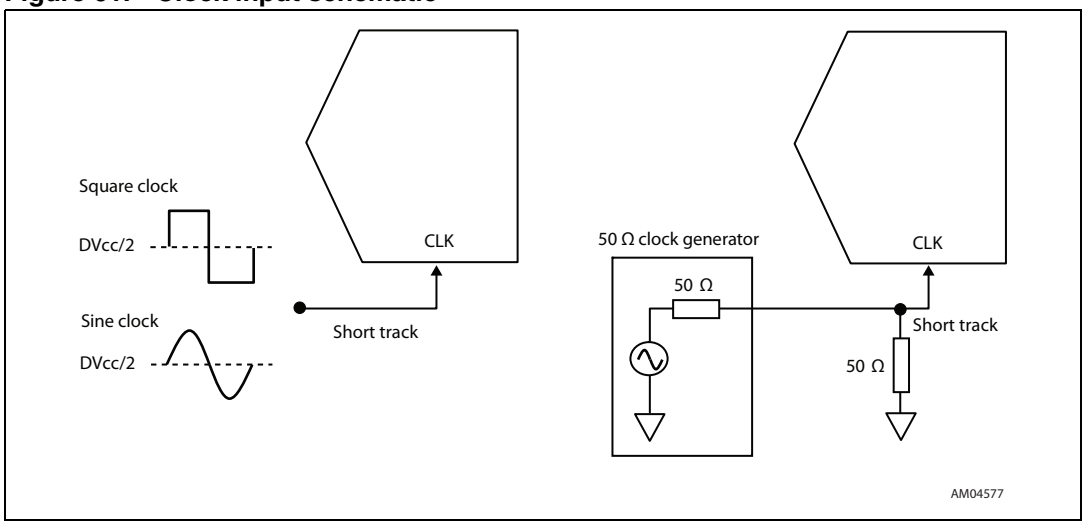
## 3.4 Clock input

The quality of the converter very much depends on the accuracy of the clock input in terms of jitter. The use of a low-jitter, crystal-controlled oscillator is recommended.

The following points should also be considered.

- The clock's power supplies must be independent of the ADC's output supplies to avoid digital noise modulation at the output.
- When powered-on, the circuit needs several clock periods to reach its normal operating conditions.

**Figure 61. Clock input schematic**




The signal applied to the CLK pin is critical to obtain full performance from the RHF1401. Below 10 MHz, the sine clock does not have transition times fast enough to achieve good performances. It is recommended to use a square signal with fast transition times and to place proper termination resistors as close as possible to the device.

The sampling instant is determined by the clock signal's rising edge. The jitter associated with this instant must be as low as possible to avoid SNR degradation on fast moving input signals. To make sure any error is less than 0.5 LSB, the total jitter $T_j$ must satisfy the following condition for a full-scale input signal.

$$T_j < \frac{1}{\pi \cdot F_{in} \cdot 2^{n+1}}$$

For example, the total jitter with a 14-bit resolution for a 10 MHz full-scale input should be no more than 1 picosecond (rms).

In most cases, the clock signal jitter is responsible for noise. Therefore, you must pay attention to the clock signal when fast signals are acquired with a low frequency clock.

## 3.5 Operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operating modes offered by the RHF1401 are described in *Table 14*.

**Table 14. RHF1401 operating modes**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| **Analog input differential amplitude** | **DFSB** | **OEB** | **OR** | **DR** | **Most significant bit (MSB)** |
| ($V_{IN}$-$V_{INB}$) above maximum range | H | L | H | CLK | D13 |
| | L | L | H | CLK | D13 complemented |
| ($V_{IN}$-$V_{INB}$) below minimum range | H | L | H | CLK | D13 |
| | L | L | H | CLK | D13 complemented |
| ($V_{IN}$-$V_{INB}$) within range | H | L | L | CLK | D13 |
| | L | L | L | CLK | D13 complemented |
| X | X | H | HZ(1) | HZ | HZ (all digital outputs are in high impedance) |

1. High impedance.

### 3.5.1 Digital inputs

**Data format select bit (DFSB):** when set to low level ($V_{IL}$), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing. When set to high level ($V_{IH}$), DFSB provides standard binary output coding (see *Table 12*).

**Output enable bit (OEB):** when set to low level ($V_{IL}$), all digital outputs remain active. When set to high level ($V_{IH}$), all digital output buffers are in a high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short $T_{on}$ delay. This feature enables the chip select of the device. *Figure 11: Timing diagram* summarizes this functionality.

**Reference mode control (REFMODE):** this allows the internal or external settings of the voltage references VREFP and INCM. REFMODE = 0 for internal references, REFMODE = 1 for external references (and disables both references VREFP and INCM).

### 3.5.2 Digital outputs

**Out of range (OR):** this function is implemented on the output stage in order to set an "out-of-range" flag whenever the digital data is over the full-scale range. Typically, there is a detection of all data at '0' or all data at '1'. It sets an output signal OR, which is in a low level state ($V_{OL}$) when the data stays within the range, or in a high-level state ($V_{OH}$) when the data read by the ADC is out of range.

**Data ready (DR):** the Data Ready output is an image of the clock being synchronized on the output data (D0 to D13). This is a very helpful signal that simplifies the synchronization of the measurement equipment of the controlling DSP. Like all other digital outputs, DR goes into high impedance when OEB is set to a high level, as shown in *Figure 11: Timing diagram*.

### 3.5.3 Digital output load considerations

The features of the internal output buffers limit the maximum load on the digital data output. In particular, the shape and amplitude of the Data Ready signal, toggling at the clock frequency, can be weakened by a higher equivalent load.

In applications that impose higher load conditions, it is recommended to use the falling edge of the master clock instead of the Data Ready signal. This is possible because the output transitions are internally synchronized with the falling edge of the clock.

**Figure 62. Output buffer fall time**

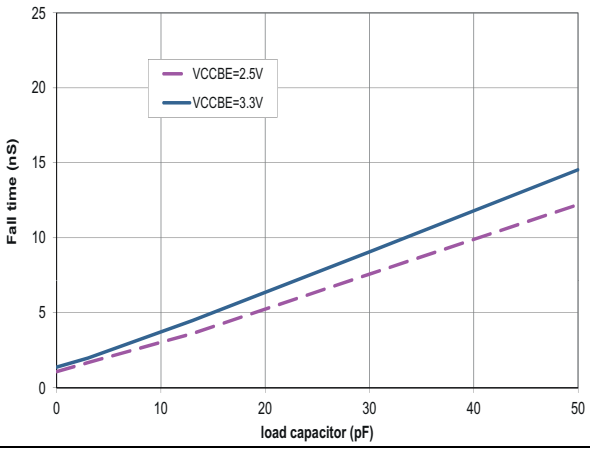
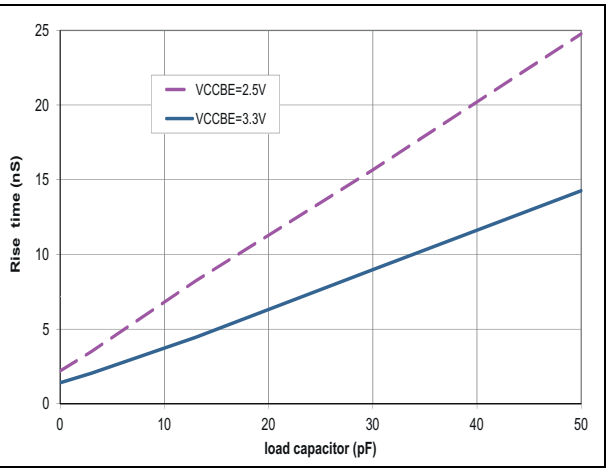



**Figure 63. Output buffer rise time**




## 3.6 PCB layout precautions

- The use of dedicated analog and digital ground planes on the PCB is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. AGND is connected to the analog ground plane and DGND, GNDBI, GNDBE are connected to the digital ground plane.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest-possible routing tracks. One way to reduce the capacitive load is to remove the ground plane under the output digital pins and layers at high sampling frequencies.
- The separation of the analog signal from the clock signal and digital outputs is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so as to decrease parasitic capacitance and inductance.
- Choose the smallest-possible component sizes (SMD).

# 4 Definitions of specified parameters

## 4.1 Static parameters

### Differential non-linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

### Integral non-linearity (INL)

An ideal converter exhibits a transfer function that is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

## 4.2 Dynamic parameters

### Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always a harmonic) and the amplitude of the fundamental tone (signal power) over the full Nyquist band.
Expressed in dBc.

### Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. Expressed in dB.

### Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($F_s/2$) excluding DC, fundamental and the first five harmonics. Reported in dB.

### Signal-to-noise and distortion ratio (SINAD)

A similar ratio to the SNR but that includes the harmonic distortion components in the noise figure (not the DC signal). Expressed in dB. From SINAD, the effective number of bits (ENOB) can easily be deduced using the formula:

$$SINAD = 6.02 \times ENOB + 1.76\ dB$$

When the analog input signal is not full-scale (FS) but has an $A_0$ amplitude, the SINAD expression becomes:

$$SINAD = 6.02 \times ENOB + 1.76\ dB + 20\ log\ (A_0 / FS)$$

### Analog input bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3 dB. Higher values can be achieved with smaller input levels.

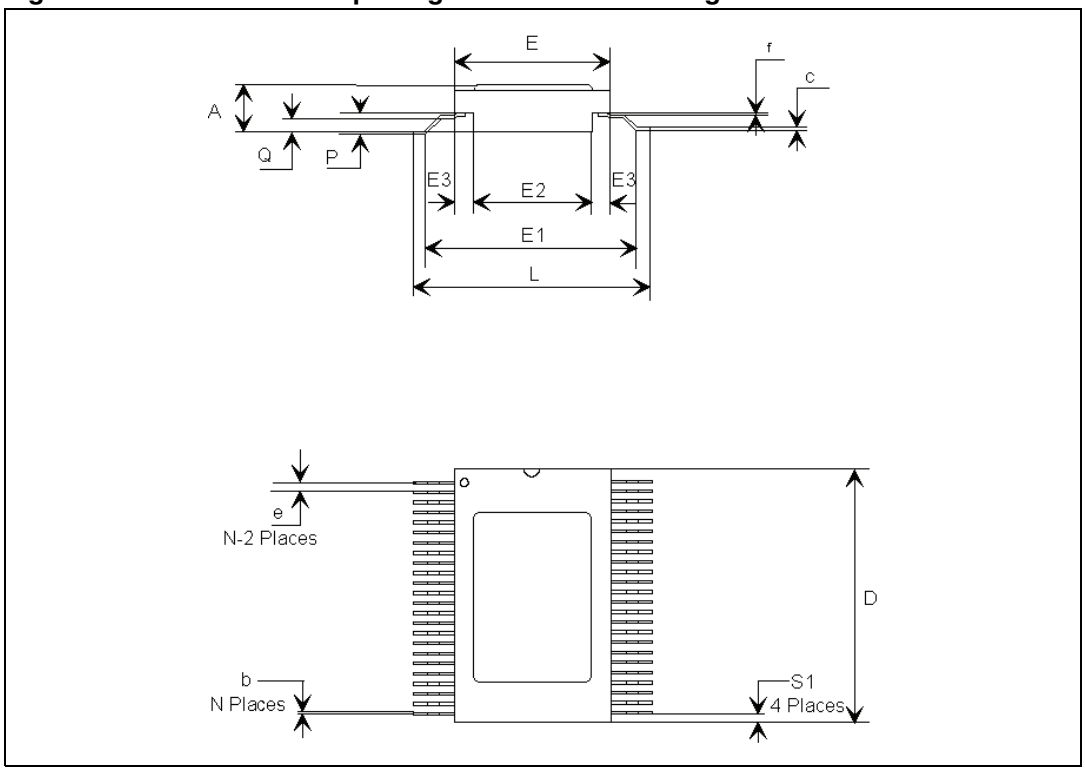
### Pipeline delay

The delay between the initial sample of the analog input and the availability of the corresponding digital data output on the output bus. Also called data latency. Expressed as a number of clock cycles.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 64. Ceramic SO-48 package mechanical drawing**




*Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.*

**Table 15. Ceramic SO-48 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.18 | 2.47 | 2.72 | 0.086 | 0.097 | 0.107 |
| b | 0.20 | 0.254 | 0.30 | 0.008 | 0.010 | 0.012 |
| c | 0.12 | 0.15 | 0.18 | 0.005 | 0.006 | 0.007 |
| D | 15.57 | 15.75 | 15.92 | 0.613 | 0.620 | 0.627 |
| E | 9.52 | 9.65 | 9.78 | 0.375 | 0.380 | 0.385 |
| E1 | | 10.90 | | | 0.429 | |
| E2 | 6.22 | 6.35 | 6.48 | 0.245 | 0.250 | 0.255 |
| E3 | 1.52 | 1.65 | 1.78 | 0.060 | 0.065 | 0.070 |
| e | | 0.635 | | | 0.025 | |
| f | | 0.20 | | | 0.008 | |
| L | 12.28 | 12.58 | 12.88 | 0.483 | 0.495 | 0.507 |
| P | 1.30 | 1.45 | 1.60 | 0.051 | 0.057 | 0.063 |
| Q | 0.66 | 0.79 | 0.92 | 0.026 | 0.031 | 0.036 |
| S1 | 0.25 | 0.43 | 0.61 | 0.010 | 0.017 | 0.024 |

# 6 Ordering information

**Table 16. Order codes**

| Order code | Quality level | Temp range | Package | Marking | Packing |
|---|---|---|---|---|---|
| RHF1401KSO1 | Engineering model | -55 °C to +125 °C | SO-48 | RHF1401KSO1 | Strip pack |
| RHF1401KSO-01V | QMLV-Flight | | | 5962F0626001VXC | |

*Note: Contact your local ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.*

# 7 Revision history

**Table 17. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 29-Jun-2007 | 1 | First public release.<br>Failure immune and latchup immune value increased to 120 MeV-cm2/mg.<br>Updated package mechanical information.<br>Removed reference to non rad-hard components from *External references, common mode: on page 16*. |
| 29-Oct-2007 | 2 | Updated *Figure 1: RHF1401 block diagram*.<br>Added explanation on *Figure 3: Timing diagram*.<br>Added introduction to *Section 6: Typical performance characteristics*.<br>Updated *Section 7.2: Clock signal requirements* and *Section 7.3: Power consumption optimization.*<br>Added *Section 7.4: Low sampling rate recommendations.*<br>Updated information on Data Ready signal in *Section 7.5: Digital inputs/outputs*.<br>Added *Figure 24: Impact of clock frequency on RHF1401 performance* and *Figure 25: CLK signal derivation*. |
| 09-Nov-2009 | 3 | Changed input clock features in *Table 10*.<br>Modified *Table 14*.<br>Added *Figure 62* to *Figure 42*. |
| 26-Feb-2010 | 4 | Modified *Figure 1: RHF1401 block diagram*.<br>Added details for Tdr and changed values for Tpd in *Table 5: Timing characteristics*.<br>Modified *Figure 11: Timing diagram*.<br>Changed values for VREFP in *Table 4*.<br>Changed Vin operating conditions in *Table 4*, *Figure 42* and *Figure 55*.<br>Changed values for DNL in *Table 9*. |
| 13-Sep-2010 | 5 | Modified *Figure 1 on page 7* and *Figure 9 on page 11*.<br>Added note *2. on page 13*.<br>Modified $C_{IN}$ typ value in *Table 6: Analog inputs* as per *Figure 3*.<br>Modified *Figure 11: Timing diagram*.<br>Replaced *Figure 18*.<br>Added *Table 12: Output codes for DFSB = 1*.<br>Modified *Figure 53: 2 Vpp differential input*. |
| 29-Jul-2011 | 6 | Added *Note: on page 31* and in the "Pin connections" diagram on the cover page. |

**Table 17. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 06-Apr-2012 | 7 | Added *Table 1: Device summary* on cover page.<br>Updated curves in *Section 2.3: Electrical characteristics (after 300 kRad)*.<br>Modified *Section 3.1: Optimizing the power consumption*.<br>Modified *Section 3.2: Driving the analog input*.<br>Modified *Section 3.3.1: Internal voltage reference*.<br>Modified *Section 3.3.2: External voltage reference*.<br>Modified *Section 3.6: PCB layout precautions*. |
| 24-Oct-2012 | 8 | Updated *Table 1*<br>Modified *Figure 1: RHF1401 block diagram*<br>Modified *Figure 4: Output buffers*<br>Modified *Table 4*, *Table 7*, and *Table 8*<br>Modified *Section 2.4: Results for differential input*<br>Modified *Section 2.5: Results for single ended input*<br>Added comments and changed layout of *Section 3.2: Driving the analog input*.<br>Modified *Table 12*<br>Modified *Figure 55*<br>Added *Table 13*<br>Added comments to *Section 3.3: Reference connections*<br>Modified *Section 3.5.1: Digital inputs* |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**