



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV5761V — Bi-CMOS LSI 1-channel Step-down Switching Regulator

Overview

The LV5761V is a 1-channel step-down switching regulator.

Functions

- 1 channel step-down switching regulator controller.
- Frequency decrease function at pendent.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Synchronous rectification.
- Current mode control.
- Synchronous drive by external signal.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	$V_{IN\text{ max}}$		45	V
Allowable Power dissipation	$P_d\text{ max}$	Mounted on a specified board. *	0.74	W
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board

Recommended Operating Range at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{IN}		8.5 to 42	V
Error amplifier input voltage			0 to 1.6	V

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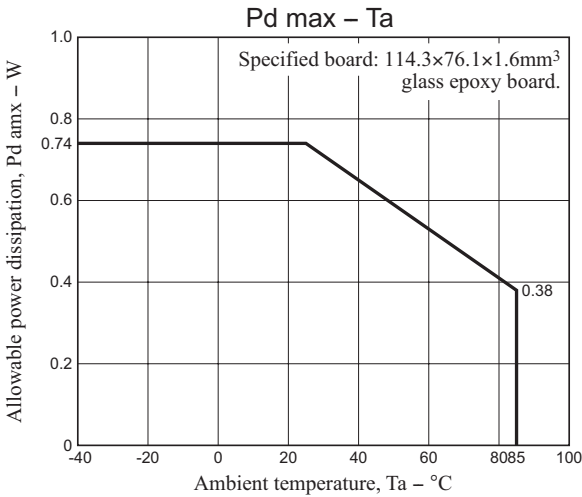
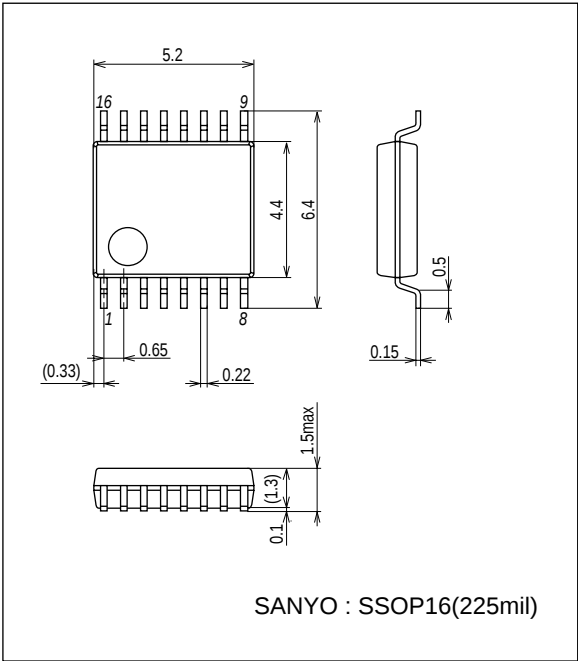
LV5761V

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

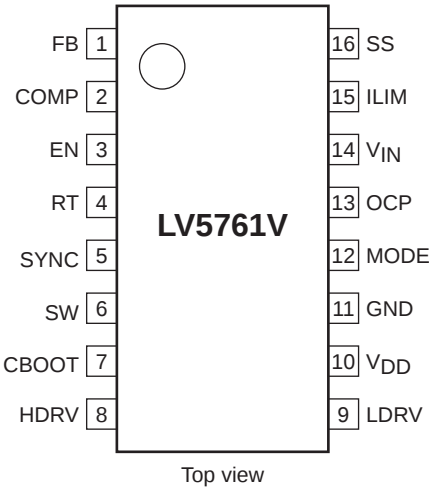
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A	0.654	0.67	0.686	V
5V power supply	VDD	IOUT = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	FOSC	RT = 220kΩ	110	125	140	kHz
Frequency variation	FOSC DV	VIN = 8 to 42V		1		%
Oscillation frequency fold back detection voltage	VOSC FB	FB voltage detection after SS ends		0.1		V
Oscillatory frequency after fold back	FOSC FB			1/3FOSC		kHz
ON/OFF circuit block						
IC start-up voltage	VEN on		2.5	3.0	3.5	V
IC off voltage	VEN off		1.0	1.2	1.4	V
Soft start circuit block						
Soft start source current	ISS SC	EN > 3.5V	4	5	6	μA
Soft start sink current	ISS SK	EN < 1V, VDD = 5V		2		mA
UVLO circuit block						
UVLO lock release voltage	VUVLO		7.5	8.0	8.5	V
UVLO hysteresis	VUVLO H			0.7		V
OCP circuit block						
OCP charge current	I _{OCP}			5		μA
Error amplifier						
Input bias current	IEA IN				100	nA
Error amplifier transconductance	GEA		1000	1400	1800	μA/V
Sink output current	IEA OSK	FB = 1.0V		-100		μA
Source output current	IEA OSC	FB = 0V		100		μA
Current detection amplifier gain	GISNS			1.5		
over current limiter circuit block						
Reference current 1	ILIM1	MODE = L (GND)	-10%	18.5	+10%	μA
Reference current 2	ILIM2	MODE = H (VIN)	-10%	37.0	+10%	μA
Over current detection comparator offset voltage	VLIM OFS		-5		+5	mA
Over current detection comparator common mode input range			VIN-0.45		VIN	V
PWM comparator						
Input threshold voltage (fosc = 125kHz)	Vt max	Duty cycle = DMAX	0.9	1.0	1.1	V
	Vt0	Duty cycle = 0%	0.4	0.5	0.6	V
Maximum ON duty	DMAX		80	85	90	%
Output block						
Output stage ON resistance (the upper side)	RONH			5		Ω
Output stage ON resistance (the under side)	RONL			5		Ω
Output stage ON current (the upper side)	IONH		240			mA
Output stage ON current (the under side)	IONL		240			mA
The whole device						
Standby current	ICCS	EN < 1V			10	μA
Mean consumption current	ICCA	EN > 3V		3		mA

Package Dimensions

unit : mm (typ)
3178B



Pin Assignment

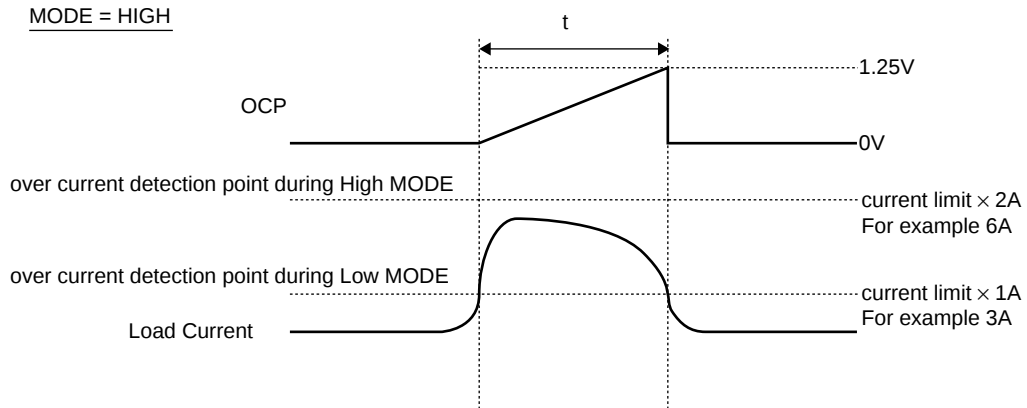


Timing Chart

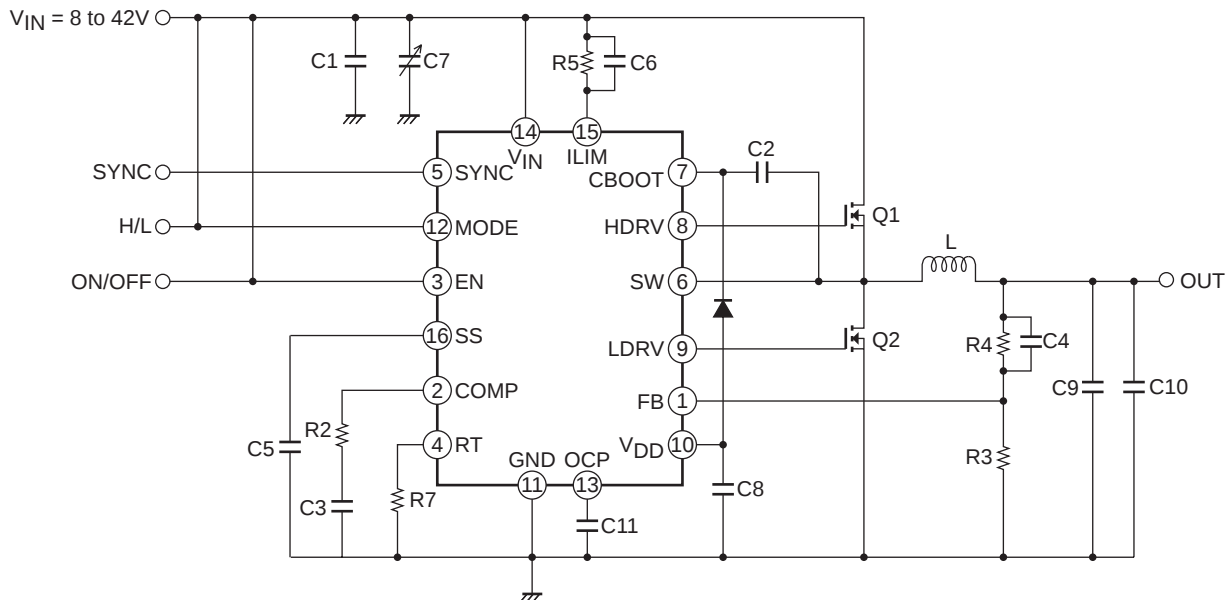
When the MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value.

Also, when the MODE pin is set to the low level, the point of over current detection remains an original value.

Timing chart of the over current detection point switching is as below.



Sample Application Circuit



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