NEC®

HIGH SPEED MASTER/SLAVE D FLIP-FLOP

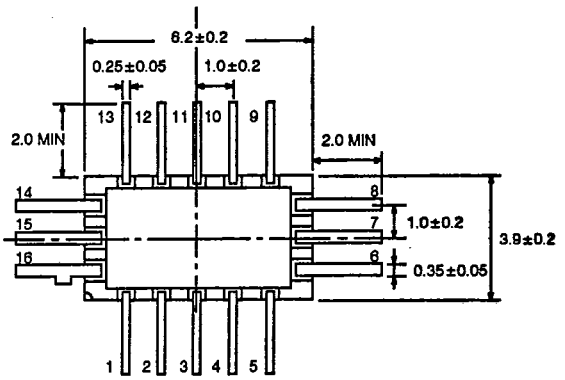
UPG706B-1 UPG706B-2

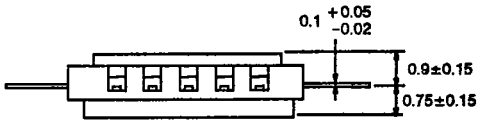
FEATURES

- **ECL COMPATIBLE**
- **ULTRA HIGH SPEED AND HIGH INPUT SENSITIVITY** f_{MAX} = 4 GHz MIN at ECL Input Level (UPG706B-1, -2)
- **HERMETICALLY SEALED CERAMIC PACKAGE ASSURES HIGH RELIABILITY**
- **UPG706B-1 MAX INPUT SENSITIVITY:** (V_{IN} = 200 mV_{P-P} at 2 GHz MIN.)
- **UPG706B-2 MAX INPUT SENSITIVITY:** (V_{IN} = 600 mV_{P-P} at 2 GHz MIN.)

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H16





PIN CONNECTION

1. V_{CS}	6. V_{CSB}	11. NC
2. Q	7. V_{DD}	12. NC
3. V_{SS1}	8. SET	13. D
4. $\overline{Q}$	9. CLK	14. Reset
5. NC	10. $\overline{CLK}$	15. V_{CSC}
		16. V_{SS2}

DESCRIPTION AND APPLICATIONS

UPG706B is a GaAs ultra high speed and high sensitivity master/slave D-type Flip-Flop. It is recommended as the data regeneration circuit in a high speed fiber optics communications receiver. It incorporates a high sensitivity amplifier and a high speed D-FF on a single GaAs substrate. This product is also available in chip form, (UPG706P).

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+4
V_{SS1}	Supply Voltage	V	V_{DD}-4
V_{SS2}	Supply Voltage	V	-8
V_{IN}	Input Voltage	V	V_{DD} - V_{SS2}
T_{STG}	Storage Temperature	°C	-65 to +175
$T_{C(OP)}$	Operating Case Temperature	°C	-65 to +125
P_T	Total Power Dissipation	mW	800

Notes:

1. V_{CS} and V_{CSB}, which are normally open, can also be used as bias adjusting terminals to optimize operating frequency or output waveform. V_{CS} and V_{CSB} are terminals to adjust the F/F circuit current and output waveform respectively. When V_{CSC}, which is an input logic threshold value adjusting terminal, is kept open, the optimum voltage is generated internally.
2. The metallized section on the back surface of the package, which is used as a heat sink, is shared with the V_{SS2} terminal (V_{SS} = -5.2 V normally). Do not ground the metallized section to GND (0 V) to prevent short circuit with V_{DD} (V_{DD} = 0 V normally) or some other terminals.
3. Take great care to prevent static electricity because the IC circuitry is composed of GaAs MES FETs.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER / PACKAGE OUTLINE				UPG706B-1, 706B-2 H16		
SYMBOLS	PARAMETERS	TEST CONDITIONS	UNITS	MIN	TYP	MAX
I_{SS2}	Supply Current	V_{DD} = 0 V V_{SS1} = -2 V V_{SS2} = -5.2 V	mA		110	
V_{OH}	High Level Output Voltage[1]		V	-1.0	-0.8	-0.6
V_{OL}	Low Level Output Voltage[1]		V	-2.0	-1.8	-1.6
V_{TH}	Threshold Voltage		V		-1.3	
I_{OH}	High Level Output Current		mA	0	4	
I_{OL}	Low Level Output Current		mA		26	
$f\phi_{MAX}$	Maximum Clock Frequency[2]		GHz	4		
$f\phi_{MAX}$	Maximum Clock Frequency[3]		GHz	2		
ϕ	Phase Margin		deg.		250	
T_{PD}	Propagation Delay		ps		400	600
T_R	Output Rise Time[5]		ps		100	
T_F	Output Fall Time[5]		ps		100	
ts	Set Up Time		ps		290	
tH	Hold Time		ps		-110	

Notes:
1. The value in case 50 Ω load resistance is connected between output and V_{TT} terminal.
   V_{TT} is the terminating voltage of the external 50 Ω load resistance and it becomes the high level voltage of the output waveform.
   The normal output waveform can be obtained even if V_{TT} is controlled from -1.5 V to 0 V.
   If V_{TT} is adjusted to -0.8 V, the ECL level output can be obtained.
2. ECL input level.
3. 200 mV_{P-P} input level (UPG706B-1)
   600 mV_{P-P} input level (UPG706B-2)
4. The time from 20% to 80% of output voltage amplitude.

TRUTH TABLE

INPUT				OUTPUT	
CLOCK	DATA	SET	RESET	Qn + 1	$\overline{Q}$n + 1
↗	L	L	L	L	H
↗	H	L	L	H	L
↘	X	L	L	Qn	$\overline{Q}$n
X	X	L	H	L	H
X	X	H	L	H	L
X	X	H	H		

H: High Level
L: Low Level
X: High or Low
Qn: The output before the clock pulse
Qn + 1: The output after the clock pulse

A. When it is open, each terminal has following voltage internally.
   D: ECL Reference Voltage
   $\overline{CK}$: ECL Reference Voltage
   CK: ECL Reference Voltage

   RESET: Low
   SET: Low

   Vcs, Vcsc and Vcsa: Appropriate voltage as needed.

B. Symmetric termination is required for Q and $\overline{Q}$ even when they are not used.

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