SPECIFICATION FOR COLOUR STN-LCM

(PRELIMINARY)

MODEL   NO.   TM128160EKCWF

TIANMA MICROELECTRONICS CO. LTD

Ver. 1.0

REVISION RECORD

Date	Ver.	Ref. Page	Revision No.	Revision Item

Ver. 1.0

CONTENTS

1. Display characteristics

Parameter	Specification
Resolution	128*(RGB)(W)*160(H)
Illumination mode	Transflective
Number of colors	65k
Number of gray scales	32
Normally white or black	black
Viewing direction	6:00
Backlight and color	LED,WHITE
Duty ratio	1/160
Application	MOBILE PHONE

2. Mechanical description

(1) Mechanical data

Parameter	Specifications	UNIT
Construction	COF	/
Overall dimension	40.8x49.5x3.4	mm
Viewing area	33.3x41.0	mm
Active area	31.2092x39.025	mm
Number of dots	128x3x160	Dots
Dot pitch	0.0813x0.244	mm
Dot size	0.0713x0.229	mm

Ver. 1.0

(2) Outline dimensions

NOTES:
1. DISPLAY TYPE: STN/COLOR
2. VIEWING DIRECTION: 6:00
3. POLARIZER MODE: TRANSFLECTIVE/NEGATIVE
4. DRIVE METHOD: 1/160 DUTY 1/11 BIAS
5. LCD OPERATING VOLTAGE: 16.2V
6. RECOMMEND VDD=3.0V
7. OPERATING TEMP.: -20°C~+70°C
8. STORAGE TEMP.: -30°C~+80°C
9. IC: HD66766RA1L
10. BACKLIGHT: LED(3.5VDC 45mA)
11. UNMARKED TOLERANCE: ±0.30mm

DOTS 128(X3)X160

DETAIL A:

DETAIL B:
PLASTIC BOX

CONDUCTIVE SIDE
BLACK SILICINE

RDW1(COM160)
RDW159(COM2)
SEG396
RDW160(COM1)
RDW2(COM159)
SEG1

TIAN-MA MICROELECTRONICS CO.

6/F., CASTIC Building, Shennan Road, Central, Shenzhen, China

DRAWN	BY:	
CHECKED	BY:	
APPROVED	BY:	
CONFIRMED BY:		

TITLE: TM128160EKCwF
DWG NO: G-1
DWG NAME: TM128160EKCwFG-1
SHEET NO: OF
UNIT: mm
SCALE

ICI/D

Pin	Name
1	NC
2	VC1
3	VC1OUT
4	C11-
5	C11+
6	C12-
7	C12+
8	VOUT
9	VSH
10	VM
11	VREFM
12	BIASC
13	VREFL
14	TEST1
15	TEST2
16	IM0/D
17	IM1
18	IM2
19	OSC1
20	OSC2
21	RESET2
22	AGND
23	GND
24	AGND
25	AVCC
26	VCC
27	CS
28	RS
29	E/WR
30	RW/RD
31	DB0
32	DB1
33	DB2
34	DB3
35	DB4
36	DB5
37	DB6
38	DB7
39	DB8
40	DB9
41	DB10
42	DB11
43	DB12
44	DB13
45	DB14
46	DB15
47	VCB2
48	C21-
49	C21+
50	C22-
51	C22+
52	C23-
53	C23+
54	C24-
55	C24+
56	VCH
57	VCL
58	CBM
59	CBP
60	RESET1

3.Limiting values (absolute maximum rating system)

Subclause	Parameters	Symbol	Value		Unit
			Min.	Max.	
3.1	Operating ambient temperature	Top	-20	70	
3.2	Storage temperature	Tstg	-30	80	
3.3	Supply voltage(s) (select either the pair of 3.3.1 and 3.3.2 or 3.3.3				
3.3.1	Supply voltage for logic drive	V_{DD}-V_{SS}	-0.3	4.0	V
3.3.2	Supply voltage for LCD drive	V_{DD}-V_{EE} or V_{EE}-V_{SS} or V_{DD}-V_{o} or V_{O}-V_{SS}	-0.3	18.0	V
3.3.3	Supply voltage(s) for module	V_{MDL} or V_{MDL1}, V_{MDL2},etc.	-0.3	4.0	V
3.4	Input signal voltage	V_{IN}	-0.4	V_{DD}+0.3	V
3.5	Voltage of integrated light source (where appropriate)			4.0	V
3.6	Operation humidity		20	65	%RH
	Storage humidity		10	80	%RH

Ver. 1.0

4. Operating range and electrical and optical characteristics

4.1 Recommended operating range

| Subclause	Parameters (Characteristics at Top=25 unless otherwise spectified)	Symbol	Value		Unit
			Min.	Max.	
4.1.1	Operating voltage range of supply voltage(s) (select either the pair of 4.1.1and 4.1.2,or 4.1.3)				
4.1.1.1	Supply voltage for logic drive	V_{DD}-V_{SS}	1.8	3.3	V
4.1.1.2	Supply voltage for LCD drive	V_{DD}-V_{EE} Or V_{EE}-V_{SS} Or V_{DD}-V_O Or V_O-V_{SS}	-	-	V
4.1.1.3	Supply voltage(s) for module	V_{MDL} Or V_{MDL1},V_{MDL2},etc	2.4	3.3	V
4.1.2	Operating voltage range of input signal voltages	V_{IN}			
4.1.2.1	Input signal voltage,high	V_{INH}	$0.8V_{DD}$	V_{DD}	V
4.1.2.2	Input signal voltage,low	V_{INL}	-0.3	$0.2V_{DD}$	V
4.1.3	Operating voltage range of analogue light source(where appropriate)		3.3	3.7	V
4.1.4	Operating frequency range(s) (where appropriate)	F_{OP}			Hz
4.1.4.1 and/or	Operating frame frequency range	f_{FRM}	-	-	Hz
4.1.4.2	Oscillator frequency range(Line rate)	f_{OSC}	28	36	KHz

4.2 Electrical and optical characteristics

| Subclasses	Characteristics at Top=25 unless otherwise specified	Symbol	Unit	Value	
				Min.	Max.
4.2.1	Supply current at specified frame frequency, specified operating supply voltage, with an adequate display pattern and other electrical driving conditions chosen in order to achieve extreme supply current	I_{tot} or I_{DD} and/or I_{EE}	mA		2.5
4.2.2	Operating current of integrated light source at its specified operating voltage(where appropriate)	(optional) I_{cs}	mA		60
4.2.3	Contrast ratio :Top=25 , x=0, y=0 VLCD=Vop	CR_{dir} and/or CR_{diff}		15	
4.2.4.1	Operating display luminance at specified viewing direction and measuring point(s) (where appropriate)	L	cd/m2	30	
4.2.4.2	Luminance uniformity (where appropriate)	L_{uni}	%		60
4.2.5	Viewing angle range (Cr 2.0)	θ_x and θ_y	deg deg	-40 -30	35 30
4.2.6.1	Rise time at 25	t_{on}	ms		200
4.2.6.2	Fall time at 25	t_{off}	ms		200
4.2.8.1	Chromaticity of white (x, y) (where appropriate)	X_W, Y_W	-	TBD	-
4.2.8.2	Chromaticity of red (x, y) (where appropriate)	X_R, Y_R	-	TBD	-
4.2.8.3	Chromaticity of blue (x,y) (where appropriate)	X_B, Y_B	-	TBD	-
4.2.8.4	Chromaticity of green (x, y) (where appropriate)	X_G, Y_G	-	TBD	-

4.3 Definition of optical characteristics
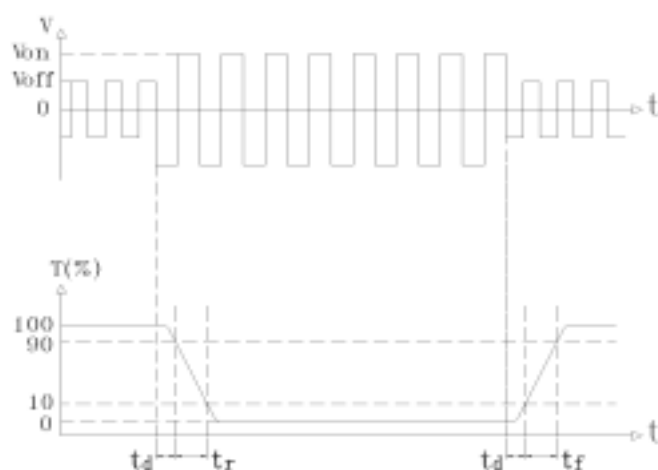
4.3.1 Definition of Viewing Angle
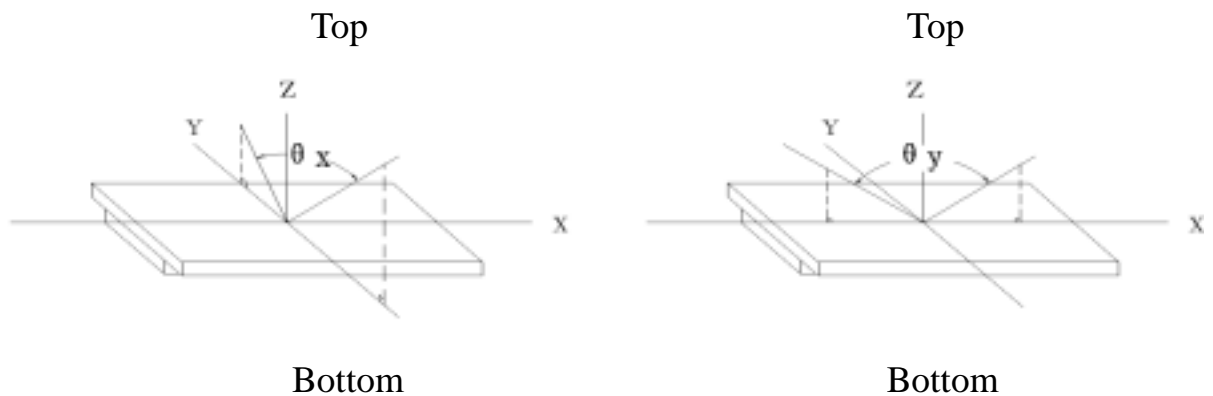
4.3.2 Definition of contrast ratio
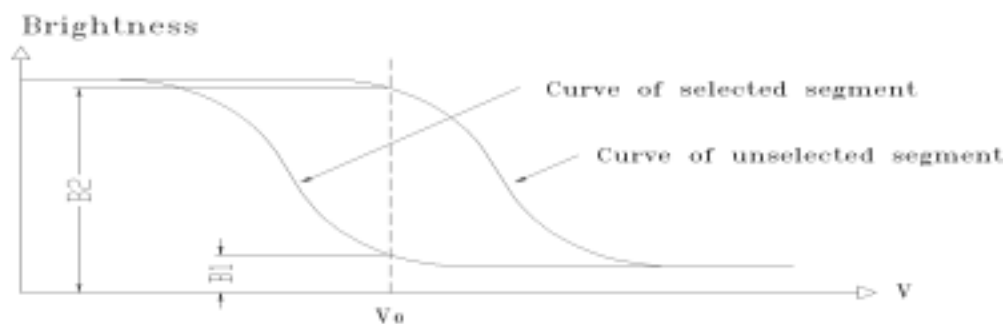
$$\text{Contrast Ratio} = \text{B2/B1} = \frac{\text{unselected state brightness}}{\text{selected state brightness}}$$

Measuring Conditions:

1) Ambient Temperature: 25   2) Frame frequency: 70.0Hz

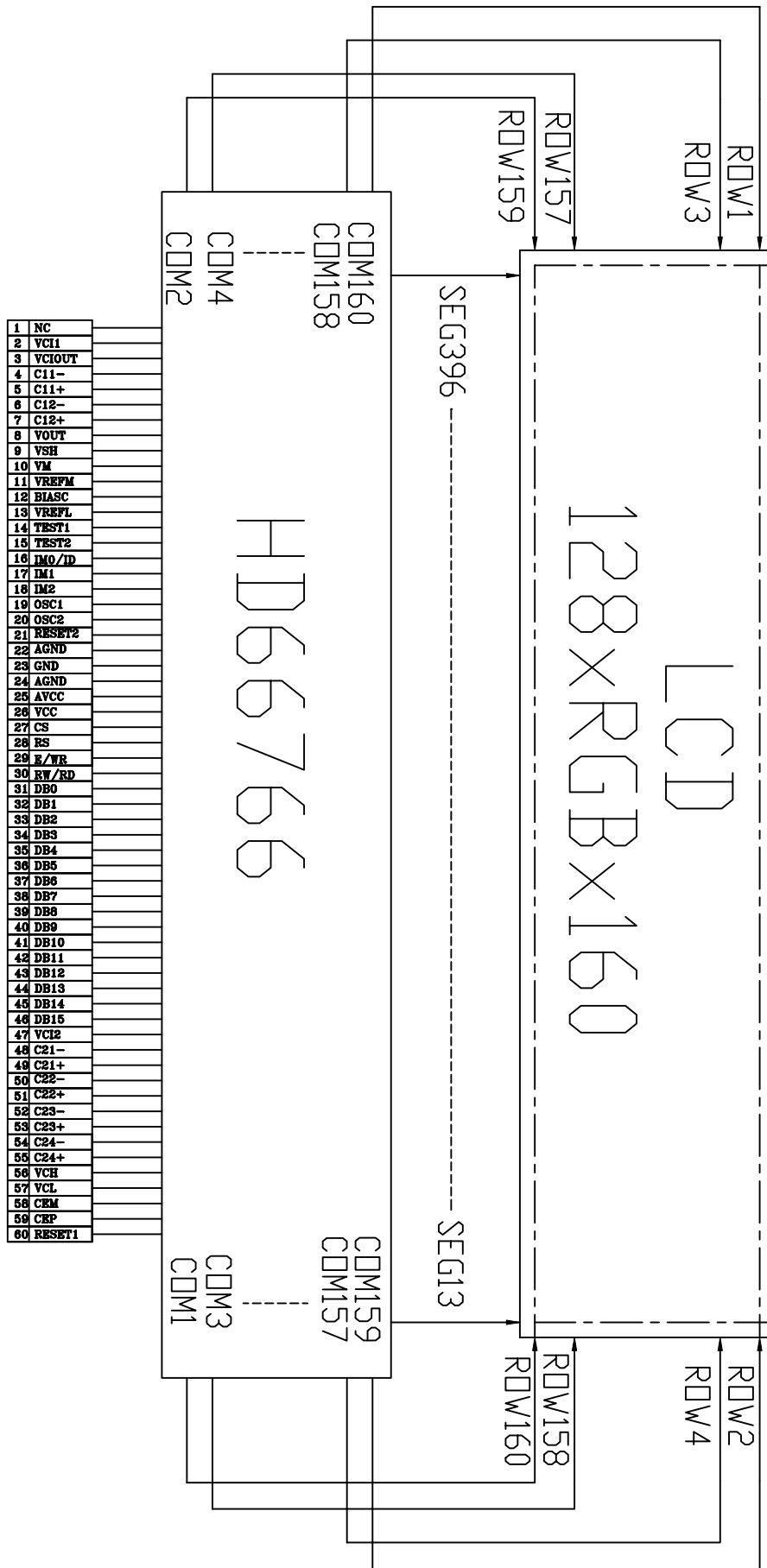### 4.3.3 Definition of Response time

Turn on time: $t_{on} = t_d + t_r$ Turn off time: $t_{off} = t_d + t_f$

Measuring Condition:

1) Operating Voltage: 16.2V   2) Frame frequency: 70.0Hz
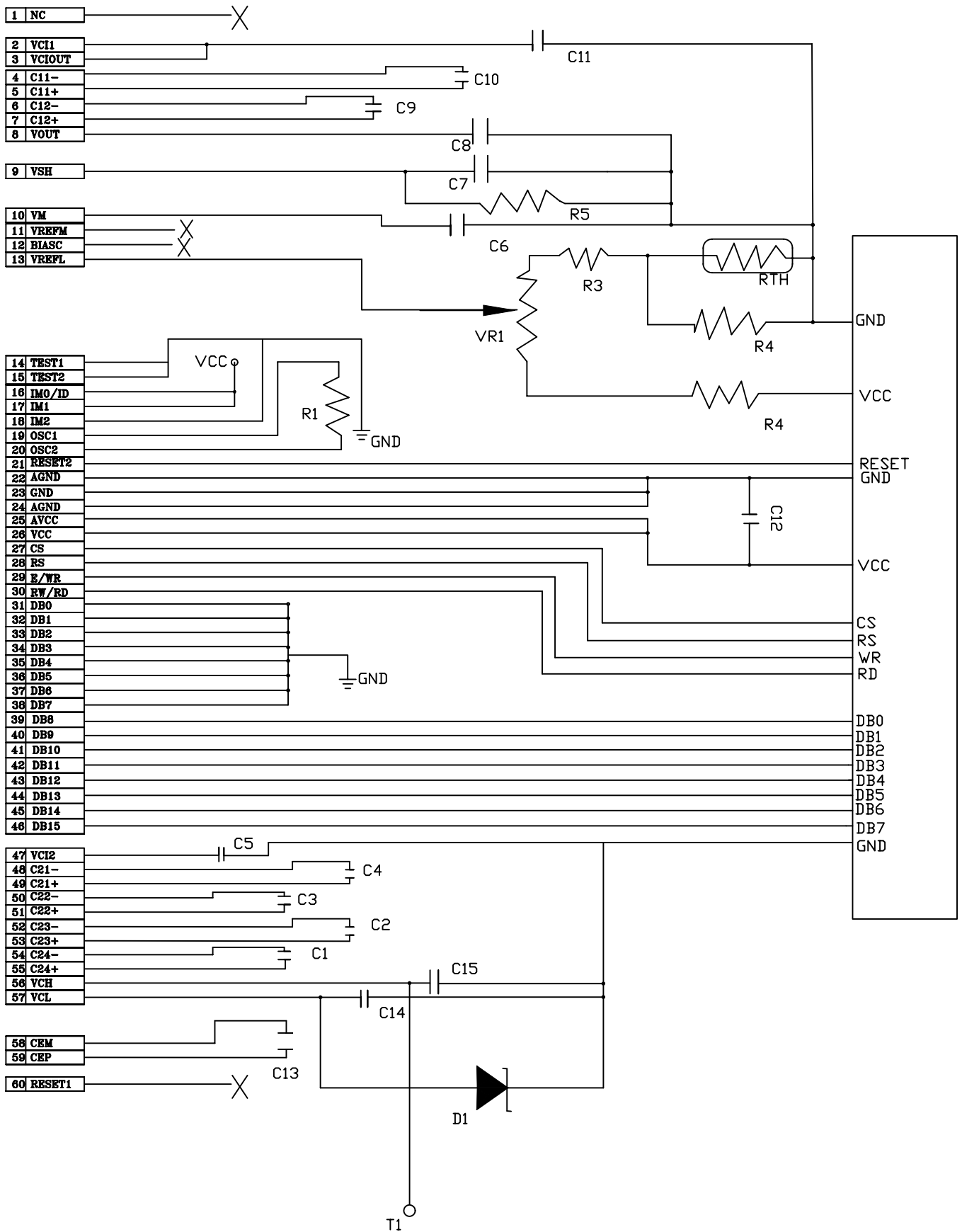
Ver. 1.0

5. Circuit block diagram

ROW1
ROW3
ROW157
ROW159

COM160
COM158
COM4
COM2

SEG396

LCD
128×RGB×160

1	NC
2	VCI1
3	VCIOUT
4	C11−
5	C11+
6	C12−
7	C12+
8	VOUT
9	VSH
10	VM
11	VREFM
12	BIASC
13	VREFL
14	TEST1
15	TEST2
16	IM0/ID
17	IM1
18	IM2
19	OSC1
20	OSC2
21	RESET2
22	AGND
23	GND
24	AGND
25	AVCC
26	VCC
27	CS
28	RS
29	E/WR
30	RW/RD
31	DB0
32	DB1
33	DB2
34	DB3
35	DB4
36	DB5
37	DB6
38	DB7
39	DB8
40	DB9
41	DB10
42	DB11
43	DB12
44	DB13
45	DB14
46	DB15
47	VCI2
48	C21−
49	C21+
50	C22−
51	C22+
52	C23−
53	C23+
54	C24−
55	C24+
56	VCH
57	VCL
58	CEM
59	CEP
60	RESET1

HD66766

COM159
COM157
COM3
COM1

SEG13

ROW2
ROW4
ROW158
ROW160

6. Interface signal

6.1 Pin Assignment

Pin No.	Symbol	Level	Description
1	NC	-	Not connect
2	VCI1	-	Voltage-input pin for step-up circuit 1
3	VCIOUT	-	Outputs a regulated voltage derived from Vcc
4	C11-	-	When step-up circuit is used, connect a step-up
5	C11+	-	capacitor
6	C12-	-	When step-up circuit is used, connect a step-up
7	C12+	-	capacitor
8	VOUT	-	A voltage that doubles or triples the voltage between Vci1 and GND is output here.
9	VSH	-	Selection level for the segment signal
10	VM	-	Non-selection level for the common signal
11	VREFM	-	Connect capacitor for stabilization for internal power
12	BIASC	-	supply
13	VREFL	-	Inputs reference voltage for LCD drives power supply
14	TEST1	-	Test pin. Must be fixed at GND level.
15	TEST2	-	Test pin. Must be fixed at GND level.
16	IM0/ID	H/L	Selects the MPU interface mode
17	IM1	H/L	
18	IM2	H/L	
19	OSC1	-	Connect an external resistor for R-C oscillation
20	OSC2	-	Connect an external resistor for R-C oscillation
21	RESET2	H/L	2 RESET pins, use one pin and open unused pin
22	AGND	0	GND for power supply circuit.
23	GND	0	GND Logic 0 V
24	AGND	0	GND for power supply circuit.
25	AVCC	-	VCC for power supply circuit
26	VCC	-	Power supply VCC: + 2.2 V to + 3.6 V
27	CS	H/L	Selects the HD66766R,L: HD66766R is selected
28	RS	H/L	Selects the register,L: Index/status H: Control
29	E/WR	H/L	For 68-system bus interface, serves as enable signal For 80-system bus interface, serves as a write strobe

Pin Assignment(Continue)

Pin No.	Symbol	Level	Description
30	RW/RD	H/L	For 68-system select data read/write operation
			For 80-system bus interface, serves as a read strobe
31	DB0	H/L	For a clock-synchronous serial interface,DB0 serves
32	DB1	H/L	as the serial data input pin (SDI). The input level is
33	DB2	H/L	read on the rising edge of the SCL signal.
34	DB3	H/L	For a clock-synchronous serial interface, DB1 serves
35	DB4	H/L	as a serial data output pin (SDO). Successive bit
36	DB5	H/L	values are output on the falling edge of the SCL
37	DB6	H/L	signal.
38	DB7	H/L	
39	DB8	H/L	For a synchronous clock interface, E/WR
40	DB9	H/L	serves as the synchronous clock signal:SCL
41	DB10	H/L	
42	DB11	H/L	DB2-DB15 Serves as a 16-bit bi-directional data bus.
43	DB12	H/L	For an 8-bit bus interface, data transfer uses
44	DB13	H/L	DB15-DB8; fix unused DB7-DB0 to the Vcc or GND
45	DB14	H/L	level. For a synchronous clock interface or unused
46	DB15	H/L	pins, fixed to the Vcc or GND level.
47	VCI2	-	Connect capacitor for stabilization
48	C21-	-	When step-up circuit is used, connect a step-up
49	C21+	-	capacitor
50	C22-	-	When step-up circuit is used, connect a step-up
51	C22+	-	capacitor
52	C23-	-	When step-up circuit is used, connect a step-up
53	C23+	-	capacitor
54	C24-	-	When step-up circuit is used, connect a step-up
55	C24+	-	capacitor
56	VCH	-	Selection level for the common signal
57	VCL	-	Selection level for the common signal
58	CEM	-	Connect a step-up capacitor to generate VCL level
59	CEP	-	Connect a step-up capacitor to generate VCL level
60	RESET1	H/L	2 RESET pins, use one pin and open unused pin

6.2 Example of external Circuit(8080 Mode)

| Pin	Signal
1	NC
2	VCI1
3	VCIOUT
4	C11−
5	C11+
6	C12−
7	C12+
8	VOUT
9	VSH
10	VM
11	VREFM
12	BIASC
13	VREFL
14	TEST1
15	TEST2
16	IM0/ID
17	IM1
18	IM2
19	OSC1
20	OSC2
21	RESET2
22	AGND
23	GND
24	AGND
25	AVCC
26	VCC
27	CS
28	RS
29	E/WR
30	RW/RD
31	DB0
32	DB1
33	DB2
34	DB3
35	DB4
36	DB5
37	DB6
38	DB7
39	DB8
40	DB9
41	DB10
42	DB11
43	DB12
44	DB13
45	DB14
46	DB15
47	VCI2
48	C21−
49	C21+
50	C22−
51	C22+
52	C23−
53	C23+
54	C24−
55	C24+
56	VCH
57	VCL
58	CEM
59	CEP
60	RESET1

7. Interface Timing Chart

AC CHARACTERISTICS
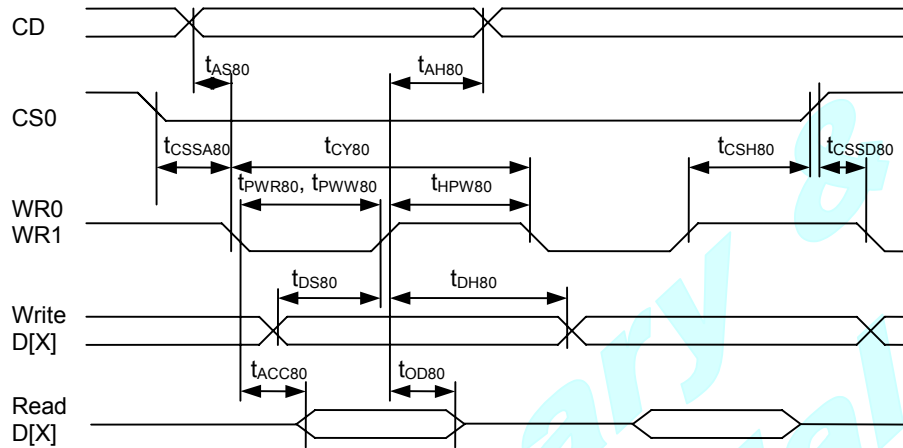
FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	– 	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 128 128 128	– 	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 35	– 	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	– 	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 35 35	– 	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	– 	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 210 120 120 120	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		100 55	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		55 55	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 100 55 55 55	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 10		ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

                    Ver. 1.0
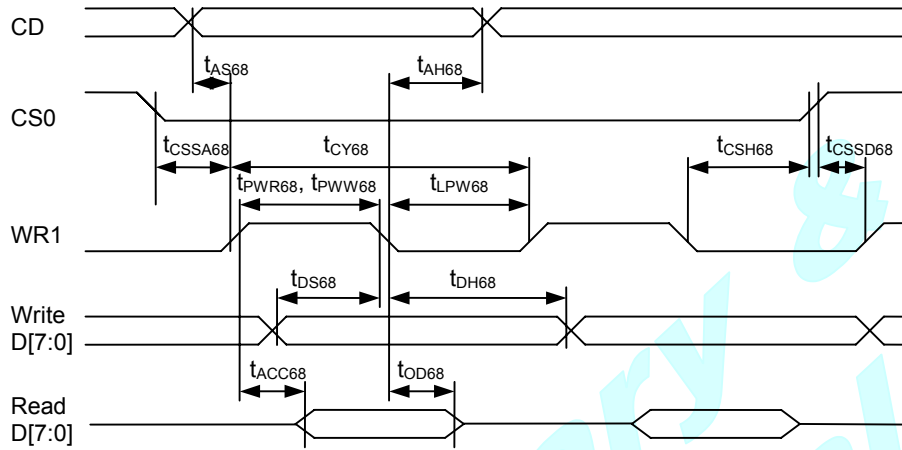
FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	– 	ns

T_{CY68}		System cycle time
		   8 bits bus (read)
		              (write)
		   4 bits bus (read)
		              (write)
				
				140
				128
				128
				128
					–
					
						ns

t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 35	– 	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	– 	ns

t_{LPW68}		Low pulse width
		   8 bits bus (read)
		              (write)
		   4 bits bus (read)
		              (write)
				
				65
				35
				35
				35
					–
					
						ns

t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	– 	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

$(V_{DD}=1.8V$ to $2.5V$, $Ta= -30$ to $+85^{o}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	ns

T_{CY68}		System cycle time
		    8 bits bus (read)
		                        (write)
		    4 bits bus (read)
		                        (write)
				
				210
				120
				120
				120
					–	ns

t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		100 55	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		55 55	–	ns

t_{LPW68}		Low pulse width
		    8 bits bus (read)
		                        (write)
		    4 bits bus (read)
		                        (write)
				
				100
				55
				55
				55
					–	ns

t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	$C_L = 100pF$	- 10		ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns
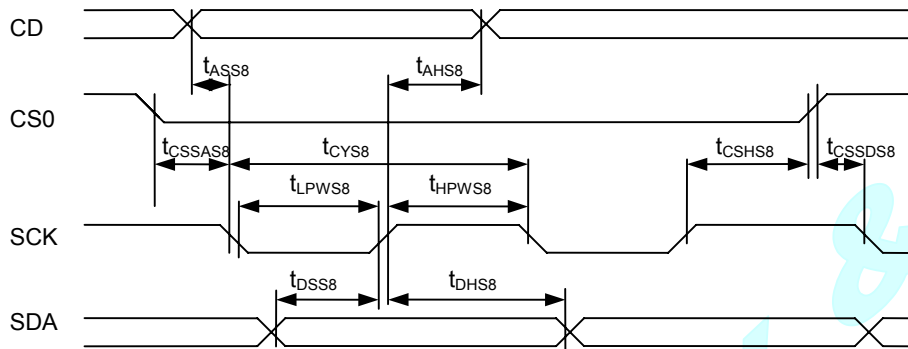
FIGURE 17: Serial Bus Timing Characteristics (for S8)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		40	–	ns
t_{CYS8}		System cycle time		135	–	ns
t_{LPWS8}	SCK	Low pulse width		65	–	ns
t_{HPWS8}		High pulse width		65	–	ns
t_{DSS8}	SDA	Data setup time		30	–	ns
t_{DHS8}		Data hold time		10		
t_{CSSAS8}				10		ns
t_{CSSDS8}	CS1/CS0	Chip select setup time		10		
t_{CSHS8}				20		

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		60	–	ns
t_{CYS8}		System cycle time		200	–	ns
t_{LPWS8}	SCK	Low pulse width		95	–	ns
t_{HPWS8}		High pulse width		95	–	ns
t_{DSS8}	SDA	Data setup time		30	–	ns
t_{DHS8}		Data hold time		10		
t_{CSSAS8}				10		ns
t_{CSSDS8}	CS1/CS0	Chip select setup time		10		
t_{CSHS8}				20		

Ver. 1.0
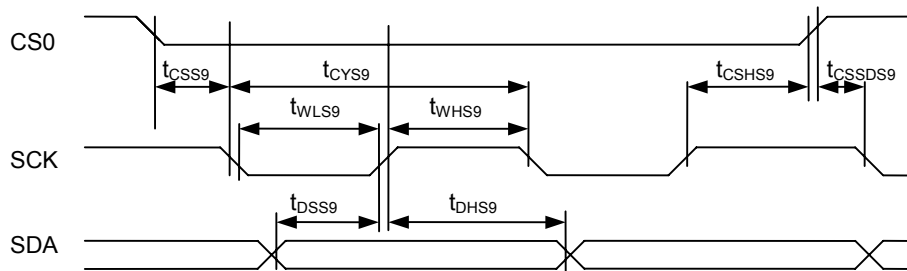
FIGURE 18: Serial Bus Timing Characteristics (for S9)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		135	–	ns
t_{LPWS9}		Low pulse width		65	–	ns
t_{HPWS9}		High pulse width		65	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		200	–	ns
t_{LPWS9}		Low pulse width		95	–	ns
t_{HPWS9}		High pulse width		95	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		ns
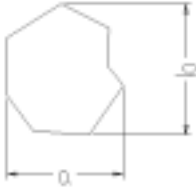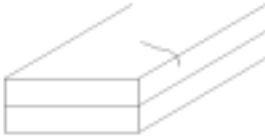
8. Test of reliability Ta=25
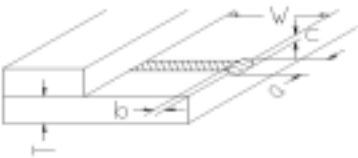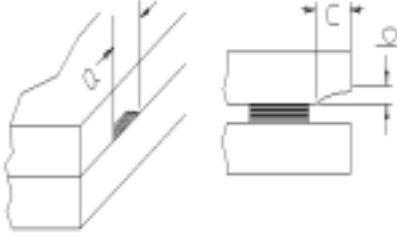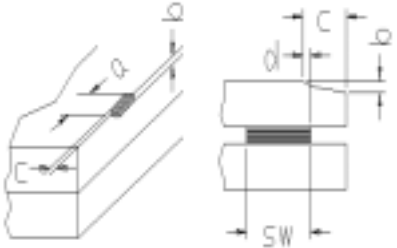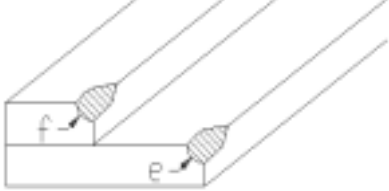
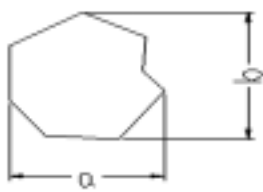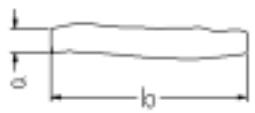| No.	Test Item	Content of Test	Test condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	80 240H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-30 240H restore 4H
3	High Temperature Operation	Endurance test applying the electric stress (voltage current) and the thermal stress to the element for a long time	70 240H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-20 240H
5	High Temperature /Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time	60 95%RH 240H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle -30 25 80 25 30min 5min 30min 5min 1 cycle	-30 /80 10 cycles
7	Vibration Test (package state)	Endurance test applying the vibration during transportation	10Hz~500Hz, 100m/s^2, 120min
8	Shock Test (package state)	Endurance test applying the shock during transportation	Half- sine wave, 300m/s^2, 18ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	25kPa 16H

9. Inspection requirement
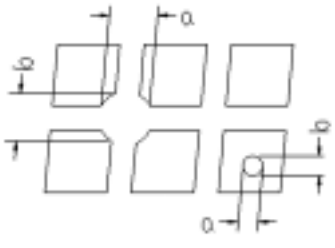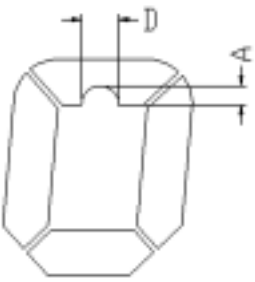
9.1 Inspection items and criteria for appearance defects

Items	Contents	Criteria		
Protective Glue		No clear defects		
Cover tape		Covering all of the chip and no clear crimple		
Leakage		Not permitted		
Rainbow		According to the limit specimen		
Polarizer	Wrong polarizer attachment	Not permitted		
	Bubble between polarizer and glass	Not counted	Max. 3 defects allowed	
		φ<0.3mm	0.3mm φ 0.5mm	
	Scratches of polarizer	According to the limit specimen		
Black spot (in viewing area)		Not counted	Max. 3 spots allowed	Max. 3 spots (lines) allowed
		X<0.20mm	0.20mm X 0.5mm	
		X=(a+b)/2		
Black line (in viewing area)		Not counted	Max. 3 lines allowed	
		a<0.02mm	0.02mm a 0.05mm b 2.0mm	
Progressive cracks		Not permitted		
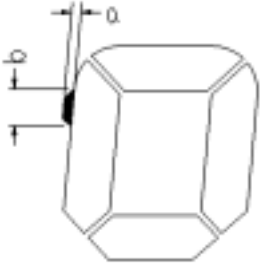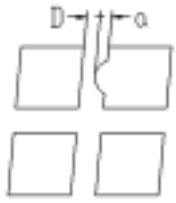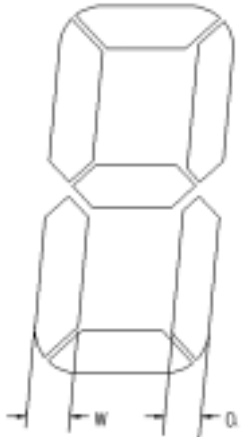
Inspection item and criteria for appearance defects (continued)

Items	Contents	Criteria				
Glass Cracks	Cracks on pads	a	b	c	Max. 2 Cracks allowed	Max. 5 cracks allowed
		3mm	W/5	T/2		
		2mm	W/5	T/2<C<T		
	Cracks on contact side	a		b	Max. 2 cracks allowed	
		3mm		T/2		
		2mm		T/2<b<T		
		C shall be not reach the seal area				
	Cracks on non-contact side	a		b		
		3mm		T/2		
		2mm		T/2<b<T		
		C 0.5mm				
		d SW/3				
	Corner cracks	$e<2.0\text{mm}^2$ $f<2.0\text{mm}^2$			Max. 3 cracks allowed	

9.2Inspection items and criteria for display defects

Items		Contents	Critera		
Open segment or open common			Not permitted		
Short			Not permitted		
Wrong viewing angle			Not permitted		
Contrast radio uneven			According to the limit specimen		
Crosstalk			According to the limit specimen		
Pin holes and cracks in segment (DOT)		Not counted	Max.3 dots allowed	Max.3 dots allowed
		X<0.1mm	0.1mm X 0.2mm	
		X=(a+b)/2		
		Not counted	Max.2 dots allowed	
		A<0.1mm	0.1mm A 0.2mm D<0.25mm	
Black spot (in viewing area)		Not counted	Max.3 spots allowed	Max.3 spots (lines) allowed
		X<0.1mm	0.1mm X 0.2mm	
		X=(a+b)/2		
Black line (in viewing area)		Not counted	Max.3 lines allowed	
		a<0.02mm	0.02mm a 0.05mm b 0.5mm	

Inspection items and criteria for display defects (continued)

Items	Content	Critera		
		Not counted	Max. 2 defects allowed	
		x 0.1mm	0.1mm x 0.2mm	
		$x=(a+b)/2$		
		Not counted	Max. 1 defects allowed	
		a 0.1mm	0.1mm a 0.2mm D>0	Max.3
Transfor- mation of segment		Max.2 defects allowed 0.8W a 1.2W a=measured value of width W=nominal value of width		

Ver. 1.0

10. Quality level

Examination or Test	At T_{amb}=25 (unless otherwise stated)	Inspection				
		Min.	Max.	Unit	IL	AQL
External Visual Inspection	Under normal illumination and eyesight condition, the distance between eyes and LCD is 25cm.	See 9.1			II	Major 1.0 Minor 2.5
Display Defects	Under normal illumination and eyesight condition, display on inspection.	See 9.2			II	Major 1.0 Minor 2.5
Note: Major defects: Open segment or common, Short, Serious damages, Leakage Miner defects: Others Sampling standard conforms to GB2828						

11. Precautions for Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

 — Isopropyl alcohol
 — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

 — Water
 — Ketone
 — Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

 a. Be sure to ground the body when handling the LCD Modules.

 b. Tools required for assembly, such as soldering irons, must be properly ground.

 c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

 d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature :   0   40

Relatively humidity: 80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.