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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC590

8-bit Binary Counter/Register (with 3-state outputs)

ADE-205-512 (Z)
1st. Edition
Sep. 2000

Description

This device each contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register, Internal circuitry prevents clocking from the clock enable.

Features

- High Speed Operation: t_{pd} (RCK to Q) = 18.5 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max (Ta = 25°C)

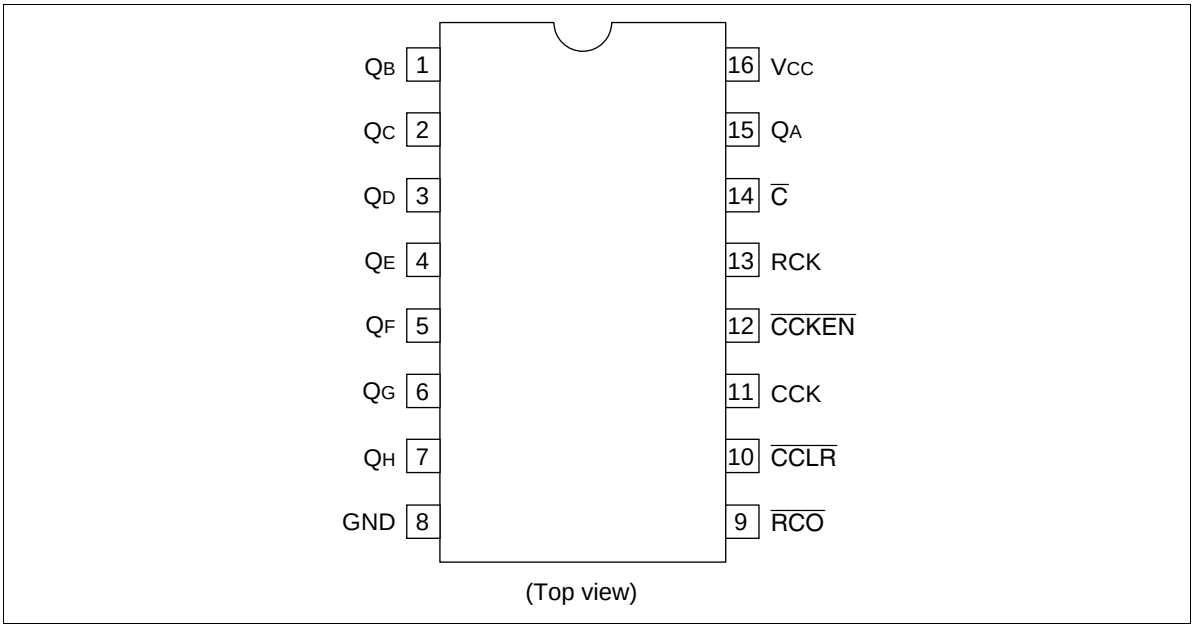
Function Table

Inputs

$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	Function
H	X	X	X	X	Q output disabled
L	X	X	X	X	Q output enabled
X	↑	X	X	X	Contents of counter stored to register
X	↓	X	X	X	No change in register
X	X	L	X	X	Counter clear
X	X	H	L	↑	Count up
X	X	H	L	↓	No count
X	X	H	H	X	No count

$\overline{RCO}$ = QA'•QB'•QC'•QD'•QE'•QF'•QG'•QH'• $\overline{(\overline{CCKEN})}$ (QA' to QH': Output of Internal Counter)

Pin Arrangement

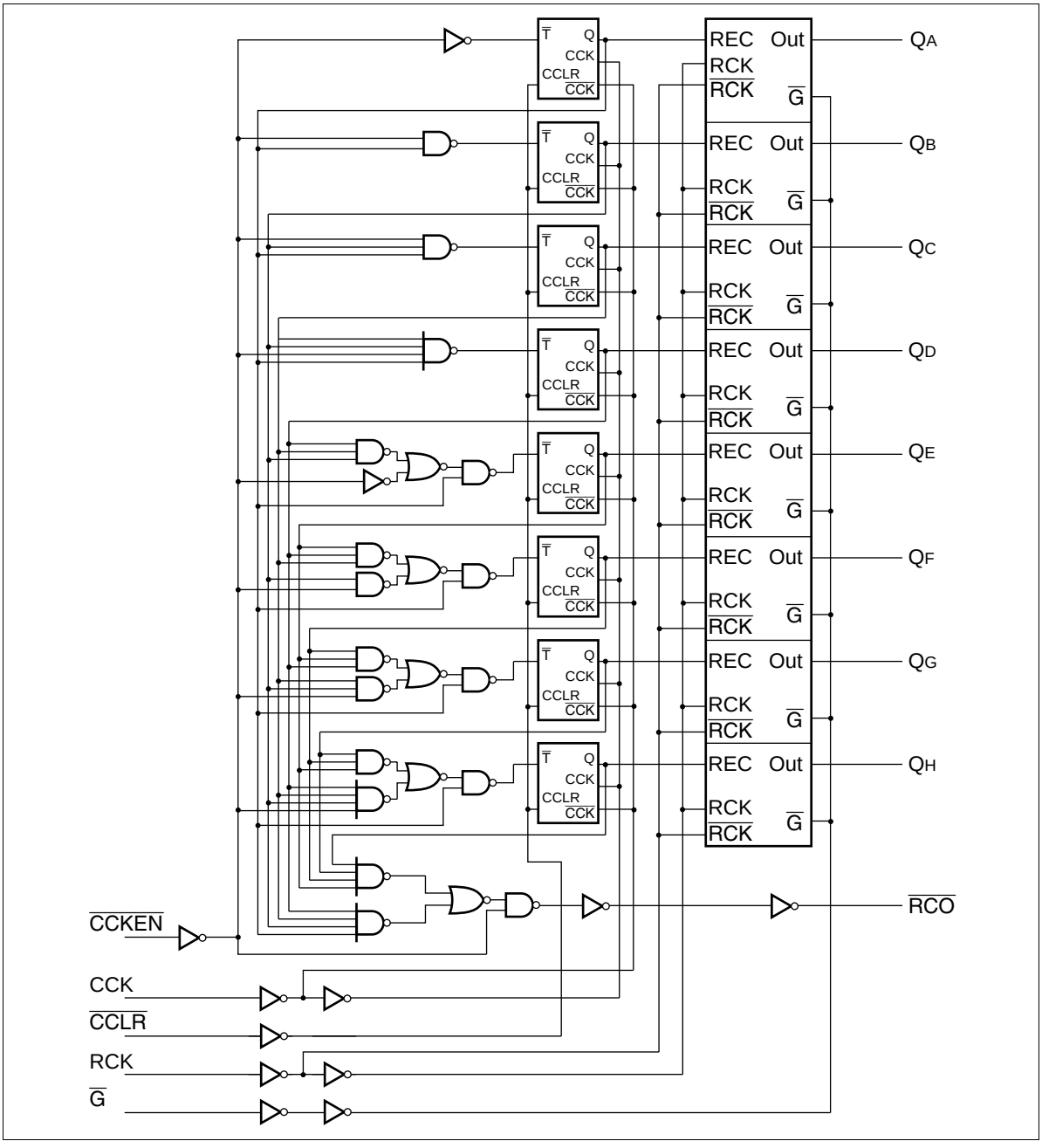


(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V
Output current	I_{OUT}	±35	mA
DC current drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power Dissipation per package	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Logic Diagram



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Q_A to Q_H	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		Vin = V_{IH} or V_{IL}	
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Q_A to Q_H	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		Vin = V_{IH} or V_{IL}	
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 7.8 mA
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$\overline{RCO}$	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		Vin = V_{IH} or V_{IL}	
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$\overline{RCO}$	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		Vin = V_{IH} or V_{IL}	
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

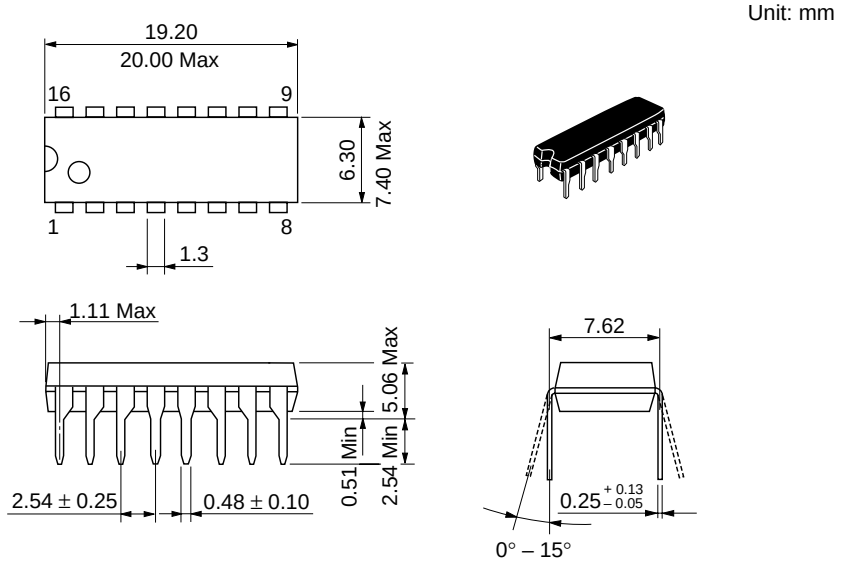
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	CCK to $\overline{RCO}$
		4.5	—	18	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	250	—	315	ns	$\overline{CCLR}$ to $\overline{RCO}$
		4.5	—	17	50	—	63		
		6.0	—	—	43	—	54		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	RCK to Q
		4.5	—	18	40	—	50		
		6.0	—	—	34	—	43		
Output enable time	t_{ZL} t_{ZH}	2.0	—	—	150	—	190	ns	
		4.5	—	16	30	—	39		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ} t_{HZ}	2.0	—	—	150	—	190	ns	
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	5	—	—	5	—	ns	$\overline{CCLR}$ to CCK
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	$\overline{CCKEN}$ to CCK
		4.5	20	–3	—	25	—		
		6.0	17	—	—	21	—		
		2.0	200	—	—	250	—	ns	CCK to RCK
		4.5	40	10	—	50	—		
		6.0	34	—	—	43	—		

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Hold time	t_h	2.0	5	—	—	5	—	ns	$\overline{\text{CCKEN}}$ to CCK
		4.5	5	—	—	5	—		CCK to RCK
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	Q
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
	t_{TLH}	2.0	—	—	75	—	95	ns	$\overline{\text{RCO}}$
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

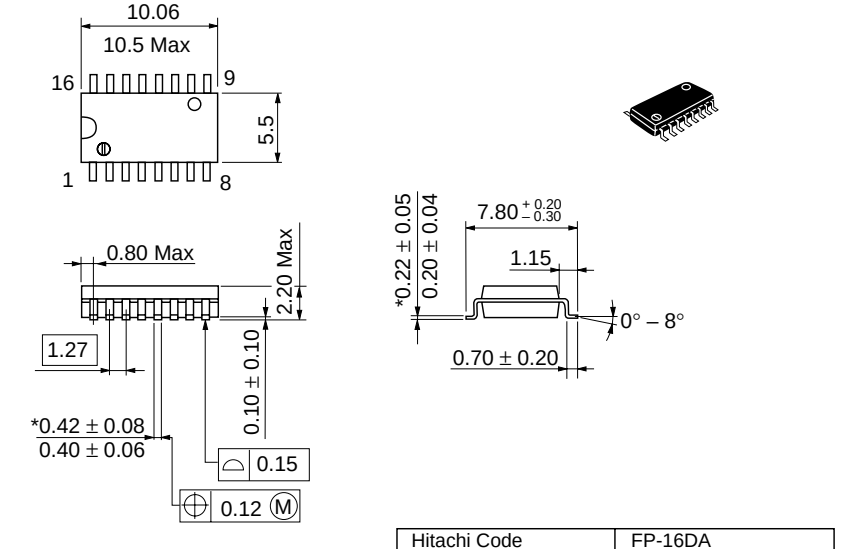
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

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