AU9380
USB Flash Disk Controller
Technical Reference Manual

Revision 2.2

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1.0 Introduction

1.1 Description

The AU9380 is a highly integrated single chip USB flash disk controller. It provides the most cost effective bridge between USB enabled PC and NAND type flash memory. AU9380 can be used as a removable storage disk in enormous data exchange applications between PC, Macintosh, laptop and workstation. It can also be configured as a bootable disk for system repairing .

The AU9380 can work with 1 to 4 NAND type flash memory chip with the combination of any popular flash memory type - 8M, 16M, 32M, 64M and 128M. Additional features include write protection switch, activity LED and password protected security .

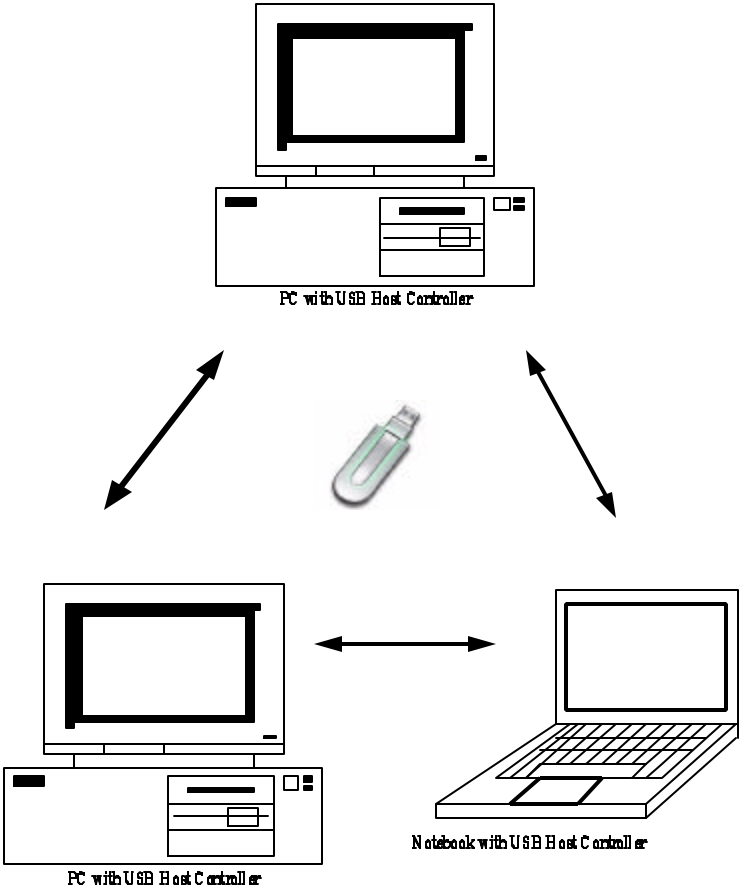
The AU9380 integrated 48MHz PLL, 3.3V regulator, power on reset circuit and a power switch for flash memory power control.

1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98se is supported by vendor driver from Alcor.
- Multiple FIFO implementation for concurrent bus operation
- Support up to 4 NAND Flash memory chips with write-protected capability
- Support total flash memory size up to 256 MB
- Support mixed different size NAND Flash
- Vendor ID, product ID and strings can be customized by utility software from Alcor
- Can be configured to support dual partitions with dynamic logic disk space allocation.
- Security function supported with password protection
- LED for bus activity monitoring
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- Built-in power switch and power management circuit to achieve 500uA suspend current required by USB specification.
- Built-in power on reset circuit
- Dedicated DMA engine to ensure highest throughput in read and write
- 48-pin TQFP package as standard package; 44-pin LQFP package is also available

2.0 Application Block Diagram

Following is the application diagram of a typical flash disk product with AU9380. By connecting the flash disk to a desktop or notebook PC through USB bus, AU9380 is implemented as a bus-powered, full speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.



3.0 Pin Assignment

The AU9380 is packed in 48-pin LQFP form factor. The figure on the following page shows the signal names for each of the pins on the chip. Accompanying the figure is the table that describes each of the pin signals.

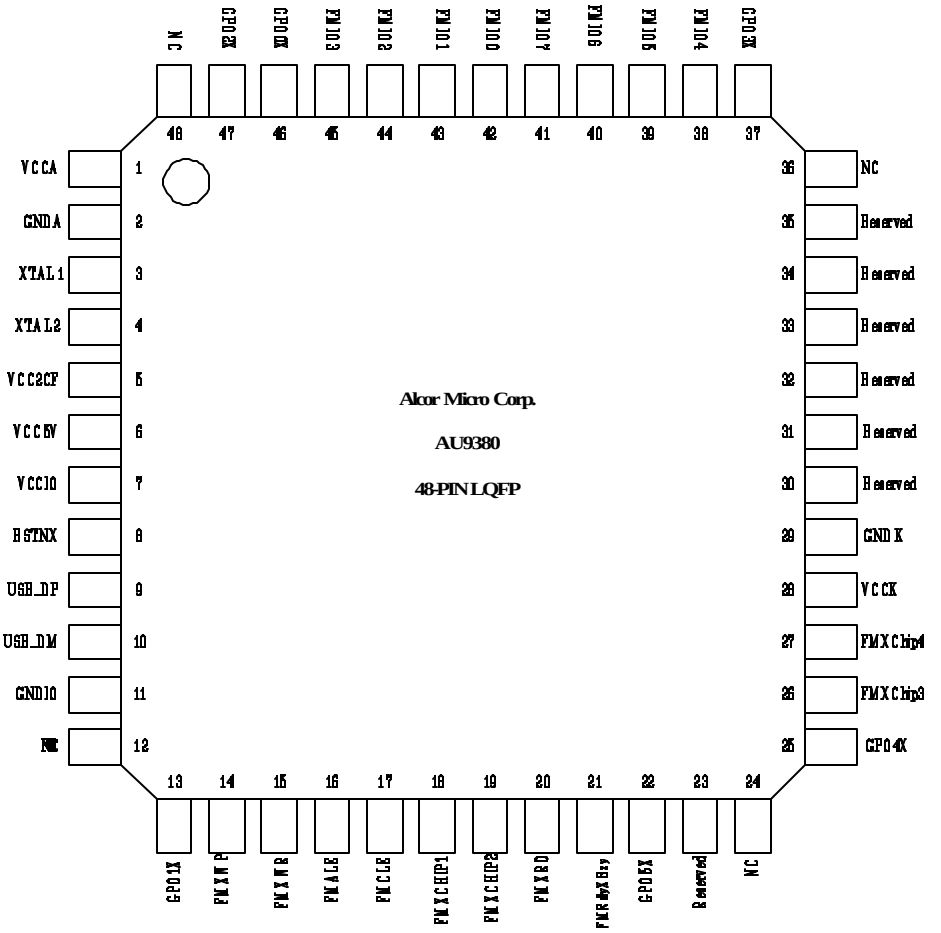


Table 3-1. Pin Descriptions

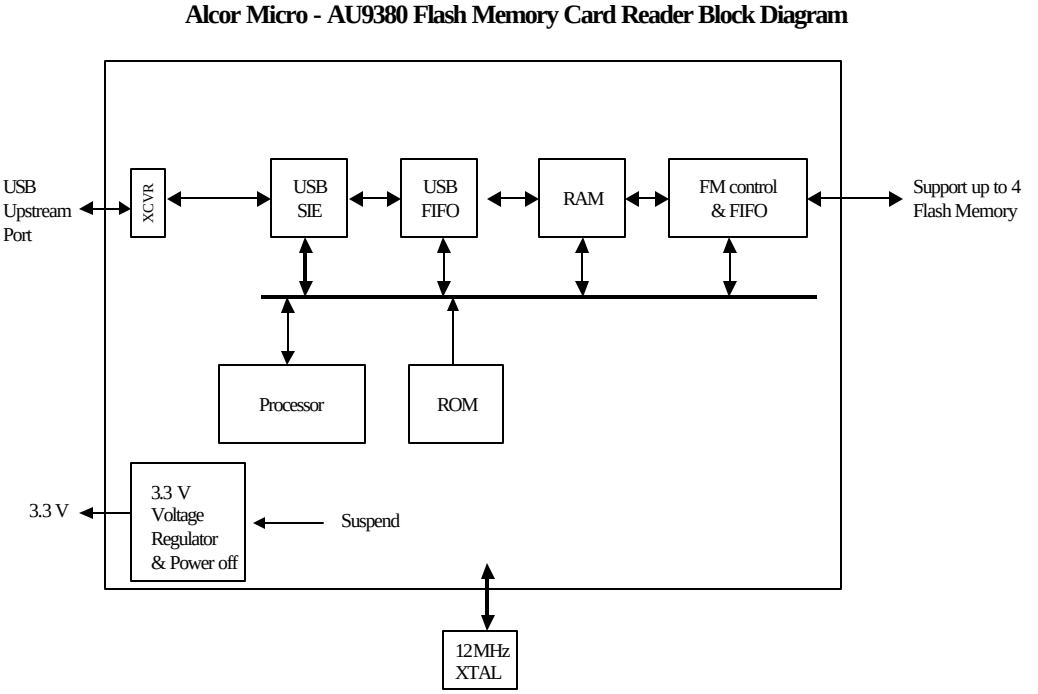
Pin#	Pin Name	I/O Type	Description
1	VCCA	PWR	3.3V input for PLL
2	GNDA	PWR	Ground
3	XTAL1	I	Crystal Oscillator Input (12MHz)
4	XTAL2	O	Crystal Oscillator Output (12MHz)
5	VCC2FM	O	Connect to Flash Memory VCC
6	VCC5V	PWR	5V power supply
7	VCCIO	PWR	Regulator 3.3V output/ IO 3.3V input
8	RSTNX	I	Hardware reset (Active Low)
9	USB_DP	I/O	USB D+
10	USB_DM	I/O	USB D-
11	GNDIO	PWR	Ground
12	NC		
13	GPO1X	O	General Purpose Output pin, used as activity LED
14	FMXWP	I	Connect to Flash Memory Write Protect
15	FMXWr	O	Connect to Flash Memory Write Enable
16	FMALE	O	Connect to Flash Memory Address Latch Enable
17	FMCLE	O	Connect to Flash Memory Command Latch Enable
18	FMXChip1	O	Connect to Flash Memory Chip1 Enable
19	FMXChip2	O	Connect to Flash Memory Chip2 Enable
20	FMXRd	O	Connect to Flash Memory Read Enable
21	FMRdyXBzy	I	Connect to Flash Memory Ready/Busy Output
22	GPO5X	O	General Purpose Output pin, used as activity LED
23	Reserved		
24	NC		
25	GPO4X	O	General Purpose Output pin, used as activity LED
26	FMXChip3	O	Connect to Flash Memory Chip3 Enable

27	FMXChip4	O	Connect to Flash Memory Chip4 Enable

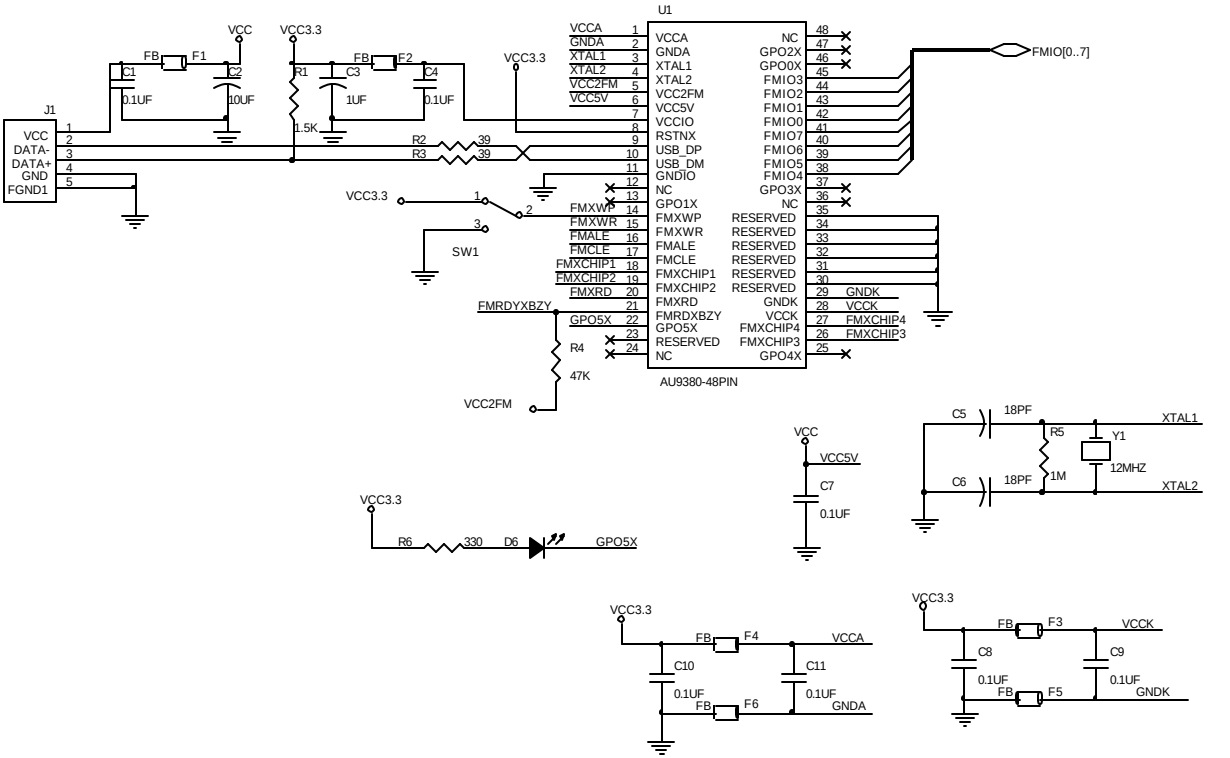
28	VCCK	PWR	Core 3.3V Input
29	GNDK	PWR	Ground
30	RESERVED		
31	RESERVED		
32	RESERVED		
33	RESERVED		
34	RESERVED		
35	RESERVED		
36	NC		
37	GPO3X	O	General Purpose Output pin, used as activity LED
38	FMIO4	I/O	Connect to Flash Memory Data IO4
39	FMIO5	I/O	Connect to Flash Memory Data IO5
40	FMIO6	I/O	Connect to Flash Memory Data IO6
41	FMIO7	I/O	Connect to Flash Memory Data IO7
42	FMIO0	I/O	Connect to Flash Memory Data IO0
43	FMIO1	I/O	Connect to Flash Memory Data IO1
44	FMIO2	I/O	Connect to Flash Memory Data IO2
45	FMIO3	I/O	Connect to Flash Memory Data IO3
46	GPO0X	O	General Purpose Output pin, used as activity LED
47	GPO2X	O	General Purpose Output pin, used as activity LED
48	NC		

4.0 System Architecture and Reference Design

4.1 AU9380 Block Diagram

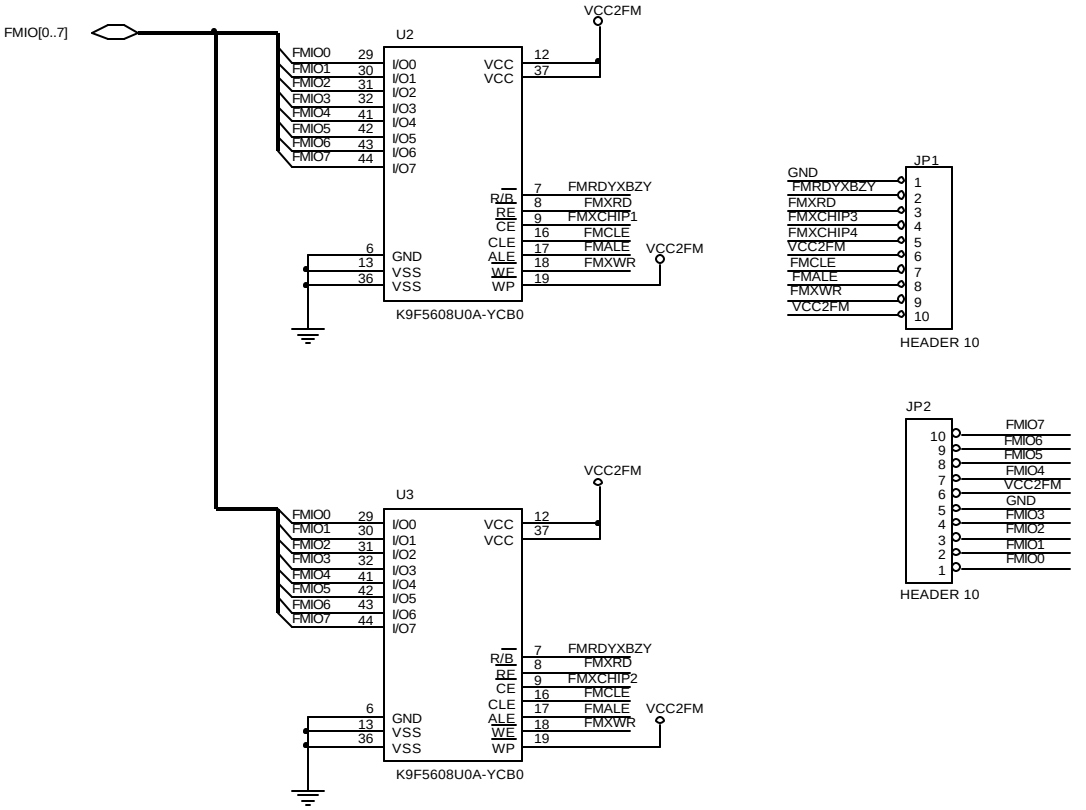


4.2 Sample Schematics



Disclaimer: This schematic is for reference only. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

Size	Document Number	Rev
A	Au9380 demostartion schematic	*1.0a*
Date: Tuesday, September 10, 2002	Sheet 1 of 1	



Size A	Document Number Au9380 demostartion schematic		Rev ***1.0a***
Date: Tuesday, September 10, 2002	Sheet 1 of 1		

5.0 Electrical Characteristics

5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	^{O}C
T_{STG}	Storage Temperature	-40		125	^{O}C

5.2 General DC Characteristics

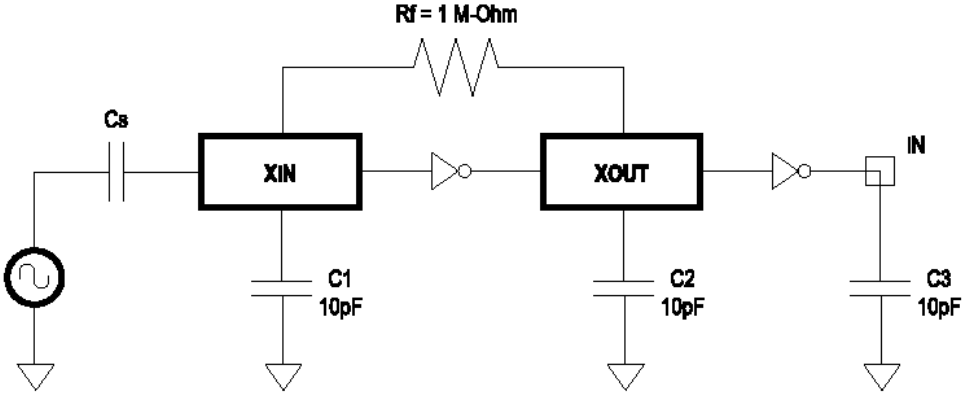
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	?A
I_{IH}	Input high current	no pull-up or pull-down	-1		1	?A
I_{OZ}	Tri-state leakage current		-10		10	?A
C_{IN}	Input capacitance			5		?F
C_{OUT}	Output capacitance			5		?F
C_{BID}	Bi-directional buffer capacitance			5		?F

5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	I_{OL}=4mA, 16mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4mA,16mA	2.4			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		10k/200k		K?

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.5 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- ✍✍ Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- ✍✍ Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

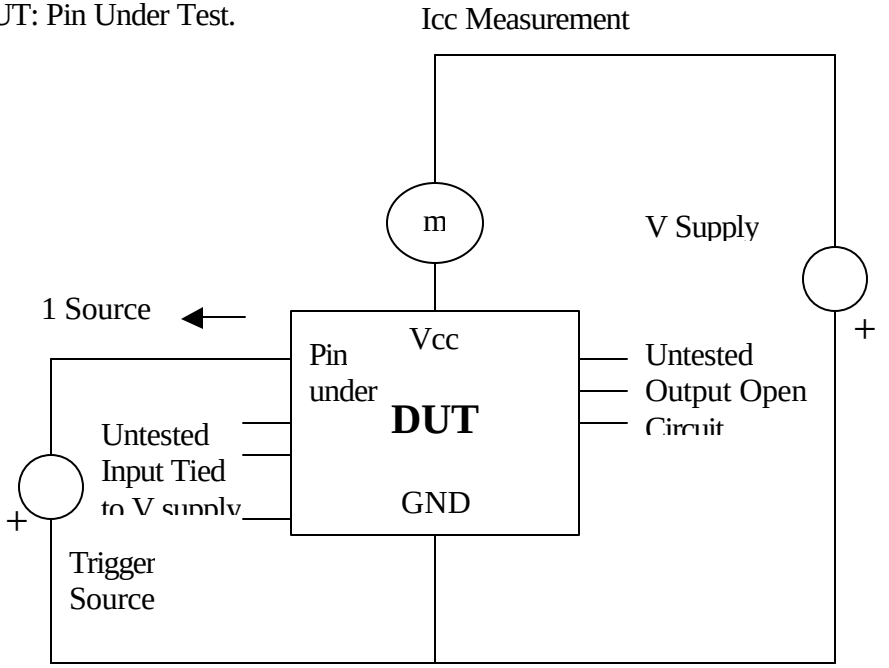
- ✍✍ Zap Interval : 1 second
- ✍✍ Number of Zaps : 3 positive and 3 negative at room temperature
- ✍✍ Critera : I-V Curve Tracing

Model	**Model**	**S/S**	**TARGET**	**Results**
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

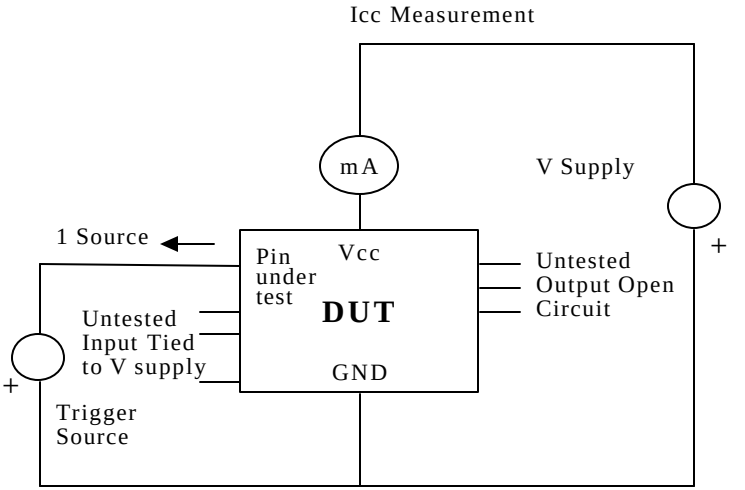
5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.
Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

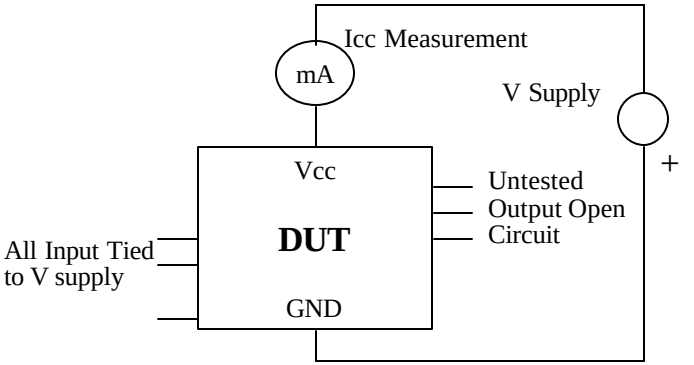
Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent

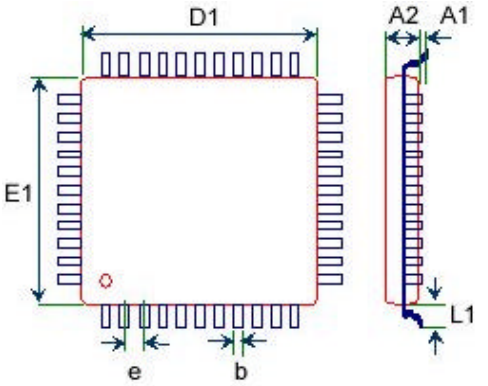


Supply Voltage test

Latch–Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

6.0 Mechanical Information



body size		lead count	A1	A2	L1	b	c	e
D1	E1							
7	7	32	0.1	1.4	1	0.35	0.127	0.8
7	7	44	0.1	1.4	1	0.2	0.127	0.5
7	7	48	0.1	1.4	1	0.2	0.127	0.5
10	10	44	0.1	1.4	1	0.3	0.127	0.8
10	10	64	0.1	1.4	1	0.2	0.127	0.5
10	10	80	0.1	1.4	1	0.16	0.127	0.4
12	12	80	0.1	1.4	1	0.2	0.127	0.5
12	12	100	0.1	1.4	1	0.16	0.127	0.4
14	14	64	0.1	1.4	1	0.35	0.127	0.8
14	14	80	0.1	1.4	1	0.3	0.127	0.65
14	14	100	0.1	1.4	1	0.2	0.127	0.5
14	14	120	0.1	1.4	1	0.16	0.127	0.4
14	14	128	0.1	1.4	1	0.16	0.127	0.4
14	20	100	0.1	1.4	1	0.3	0.127	0.65
14	20	128	0.1	1.4	1	0.2	0.127	0.5
20	20	144	0.1	1.4	1	0.2	0.127	0.5
20	20	160	0.1	1.4	1	0.16	0.127	0.4
24	24	160	0.1	1.4	1	0.2	0.127	0.5
24	24	176	0.1	1.4	1	0.16	0.127	0.4
24	24	216	0.1	1.4	1	0.16	0.127	0.4
28	28	160	0.1	1.4	1	0.3	0.127	0.65
28	28	208	0.1	1.4	1	0.2	0.127	0.5
28	28	256	0.1	1.4	1	0.16	0.127	0.4

A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch