GENERAL DESCRIPTION

The CM6510C is the Green-Mode PFC controller for High Density AC Adapter. For the power supply less than 200Watt, it's input current shaping PFC performance could be very close to the performance of the CM6800 or ML4800 leading edge modulation average current topology.

CM6510C offers the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply fully compliant to IEC1000-3-2 specifications. The CM6510C includes circuits for the implementation of a leading edge, input current shaping technique "boost" type PFC.

The CM6510C's PFC operate at the same frequency, 67.5kHz. A PFC OVP comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting for enhanced system reliability.

PFC has the Green Mode Functions.
When the load is below GMth, Green Mode Threshold, PFCOUT is turned off. The GMth can be programmed by the designer.
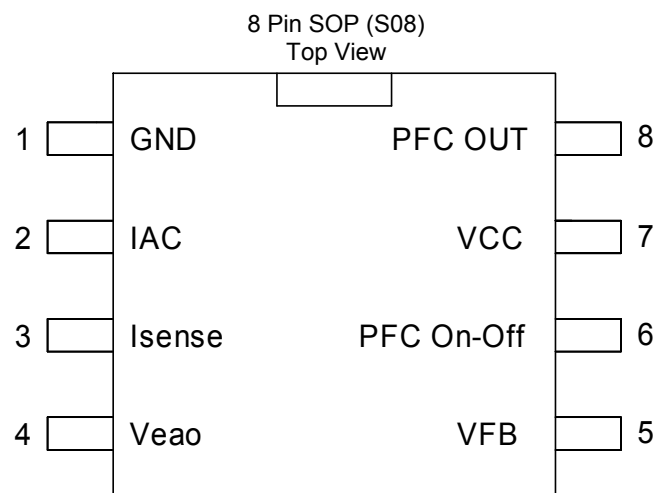
FEATURES

◆ Patent Filed #5,565,761, #5,747,977, #5,742,151, #5,804,950, #5,798,635
◆ PFC has the Green Mode to meet blue angel and energy star spec.
◆ 8-Pin SOIC package
◆ Use RAC as the Startup resistor which can be > 2000K or higher at IAC pin
◆ It can use the HV bipolar to start up the chip and it helps green mode.
◆ Easy to configure into Boost Follower
◆ Enable lowest BOM for power supply with PFC
◆ Patented slew rate enhanced voltage error amplifier with advanced input current shaping technique
◆ Universal Line Input Voltage
◆ CCM boost or DCM boost with leading edge modulation PFC using Input Current Shaping Technique
◆ Feedforward IAC pin to do the automatic slope compensation
◆ PFCOVP, VCCOVP, Precision -1V PFC ILIMIT, PFC PFC On-Off Detect comparator to meet UL1950
◆ Low supply currents; start-up: 100uA typical, operating current: 2mA typical.
◆ UVLO, REFOK, and brownout protection

APPLICATIONS

◆ AC Adaptor
◆ Open Frame

PIN CONFIGURATION

8 Pin SOP (S08)
Top View

1	GND	PFC OUT	8
2	IAC	VCC	7
3	Isense	PFC On-Off	6
4	Veao	VFB	5

PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	GND	Ground				
2	IAC	Feedforward input to do slope compensation and to start up the system. During the start up, IAC is connected to VCC until VCC is greater than 13V.	0		1	V
3	I_{SENSE}	Current sense input to the PFC current limit comparator	-5		0.7	V
4	VEAO	PFC transconductance voltage error amplifier output	0		6	V
5	V_{FB}	PFC transconductance voltage error amplifier input	0	2.5	3	V
6	PFC On-Off	It can turn off PFC stage when it is below (VCC-1.4V)/2.	0		VCC	V
7	VCC	Positive supply	10		18	V
8	PFC OUT	PFC driver output	0		VCC	V

ORDERING INFORMATION

Part Number	Operation Frequency	Initial Accuracy (KHz)			Temperature Range	Package
		Min	Typ	Max		
CM6510CXIS*	Fpwm = Fpfc = 67.5Khz	60	67	74	-40℃ to 125℃	8 Pin SOP(S08)

Note:
1. X : Suffix for Halogen Free and PB Free Product
2. Initial Accuracy : T_A=25℃

BLOCK DIAGRAM

PROTECTED BY PATENT
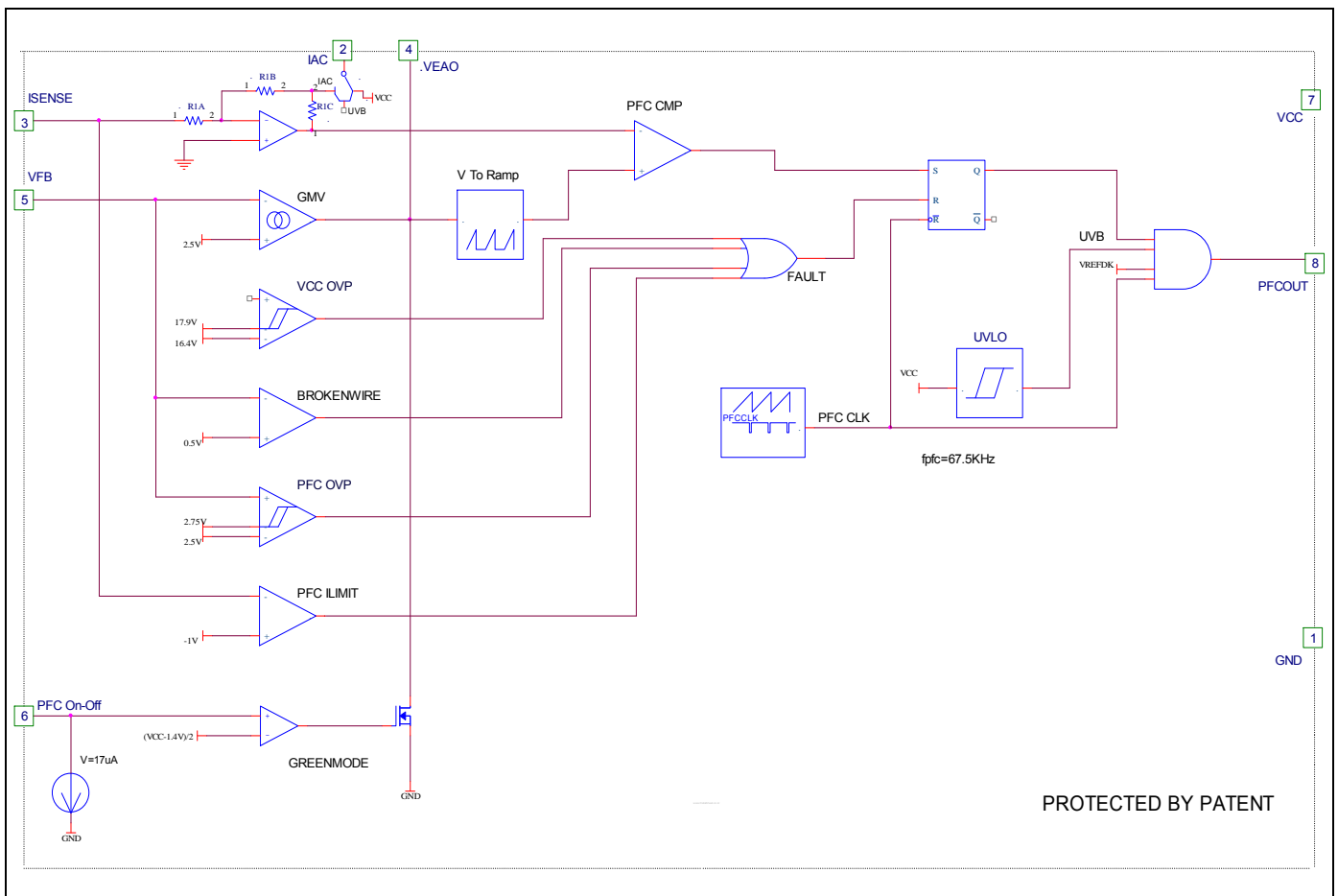
ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC} MAX		20	V
IAC (before start up)	GND-0.3	VCC + 0.3	V
IAC (after start up)	GND-0.3	1.0	V
I_{SENSE} Voltage	-5	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
VEAO	0	6.3	V
Voltage on Any Other Pin	GND-0.3	VCC + 0.3	V
Peak PFC OUT Current, Source or Sink		0.5	A
PFC OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA})		80	℃/W

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc=+14V, T$_A$=Operating Temperature Range (Note 1)

| Symbol	Parameter	Test Conditions	CM6510C			Unit
			Min.	Typ.	Max.	
Voltage Error Amplifier (g$_{mv}$)						
	Input Voltage Range		0		5	V
	Transconductance	V$_{NONINV}$ = V$_{INV}$, VEAO = 3.75V	30	65	90	μmho
	Feedback Reference Voltage		2.43	2.5	2.56	V
	Input Bias Current	Note 2		-0.5	-1.0	μA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V$_{FB}$ = 3V, VEAO = 6V		-35	-20	μA
	Source Current	V$_{FB}$ = 1.5V, VEAO = 1.5V	30	40		μA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	11V < V$_{CC}$ < 16.5V	50	60		dB
IAC						
	Input Impedance	ISENSE = 0V, T$_A$=25℃	35	40	45	K
VCC OVP Comparator						
	Threshold Voltage		17.3	17.9	18.5	V
	Hysteresis		1.3	1.5	1.75	V
PFC OVP Comparator						
	Threshold Voltage		2.64	2.77	2.85	V
	Hysteresis		230		300	mV
PFC I$_{LIMIT}$ Comparator						
	Threshold Voltage		-1.1	-1	-0.9	V
	Delay to Output			150	300	ns
V$_{IN}$ OK Comparator						
	Threshold Voltage		2.30	2.45	2.55	V
	Hysteresis		1.65	1.75	1.85	V
PFC On-Off Detect Comparator						
	Fault Detect HIGH		2.70	2.77	2.85	V
	Time to Fault Detect HIGH	V$_{FB}$=V$_{FAULT\ DETECT\ LOW}$ to V$_{FB}$ = OPEN, 470pF from V$_{FB}$ to GND		2	4	ms
	Fault Detect LOW		0.4	0.5	0.6	V

ELECTRICAL CHARACTERISTICS

(Conti.)Unless otherwise stated, these specifications apply Vcc=+14V, T$_A$=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6510C			Unit
			Min.	Typ.	Max.	
Oscillator						
	Voltage Stability	10V < V$_{CC}$ < 15V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	60	67	74.5	kHz
	PFC Dead Time (Note 2)		0.3	0.45	0.65	us
PFC						
	Minimum Duty Cycle	I$_{AC}$=100uA,V$_{FB}$=2.55V, I$_{SENSE}$ = 0V			1	%
	Maximum Duty Cycle	I$_{AC}$=0uA,V$_{FB}$=2.0V, I$_{SENSE}$ = 0V	90	95		%
	Output Low Rdson			15	22.5	ohm
	Output Low Voltage	I$_{OUT}$ = -100mA		0.8	1.5	V
		I$_{OUT}$ = -10mA, V$_{CC}$ = 8V		0.4	0.8	V
	Output High Rdson			30	45	ohm
	Output High Voltage	I$_{OUT}$ = 100mA, V$_{CC}$ = 15V	13.5	14.2		V
	Rise/Fall Time (Note 2)	C$_L$ = 1000pF		50		ns
Supply						
	Start-Up Current	V$_{CC}$ = 11V, C$_L$ = 0		100	150	uA
	Operating Current	V$_{CC}$ = 15V, C$_L$ = 0		2	4.0	mA
	Undervoltage Lockout Threshold		12.35	13	13.65	V
	Undervoltage Lockout Hysteresis		2.7	3	3.3	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Guaranteed by design, not 100% production test.

TYPICAL PERFORMANCE CHARACTERISTIC
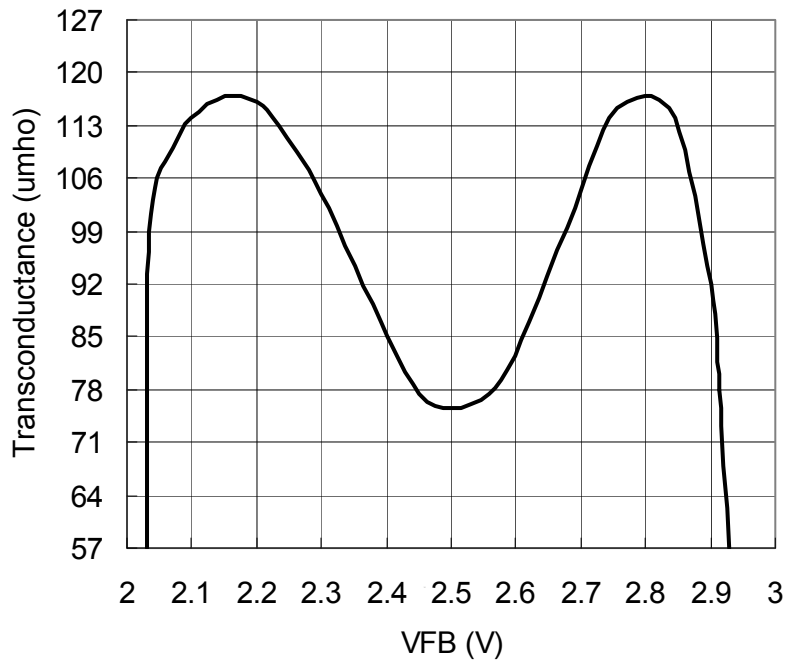
Voltage Error Amplifier (g_{mv}) Transconductance

Functional Description

The CM6510C consists of an ICST (Input Current Shaping Technique), CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) boost PFC (Power Factor Correction) front end and a synchronized PWM (Pulse Width Modulator) back end. The CM6510C is designed to replace FAN6803 (8 pin SOP package), which is the second generation of the ML4803 with 8 pin package. It is distinguished from earlier combo controllers by its low count, innovative input current shaping technique, and very low start-up and operating currents. It uses conventional trailing-edge modulation, while the PFC uses leading-edge modulation. This patented Leading Edge/Trailing Edge (LETE) modulation technique helps to minimize ripple current in the PFC DC buss capacitor.

The main improvements from ML4803 are:
1. Add Green Mode Functions for PFC
2. Remove the one pin error amplifier and add back the slew rate enhancement gmv, which is using voltage input instead of current input. This transconductance amplifier will increase the transient response 5 to 10 times from the conventional OP
3. VFB PFC OVP comparator
4. PFC PFC On-Off Detect for UL1950 compliance and enhanced safety
5. A feedforward signal from IAC pin is added to do the automatic slope compensation. This increases the signal to noise ratio during the light load; therefore, THD is improved at light load and high input line voltage.
6. CM6510C does not require the bleed resistor and it uses the more than 800k ohm resistor between IAC pin and rectified line voltage to feed the initial current before the chip wakes up.
7. A 10mS digital PWM soft start circuit is added
8. 10 pin SOP package
9. No internal Zener but with VCCOVP comparator

The CM6510C operates PFC sections at 67kHz.
Several protection features have been built into the CM6510C. These include soft-start, redundant PFC overvoltage protection, PFC PFC On-Off Detect, VINOK, peak current limiting, duty cycle limiting, under-voltage lockout, reference ok comparator and VCCOVP.

Detailed Pin Descriptions
IAC (Pin 2)
Typically, it has a feedforward resistor, RAC, 2KK~10KK ohm resistor connected between this pin and rectified line input voltage.
This pin serves 2 purposes:
1.) During the startup condition, it supplies the startup current; therefore, the system does not requires additional bleed resistor to start up the chip.
2.) The current of RAC will program the automatic slope compensation for the system. This feedforward signal can increase the signal to noise ratio for the light load condition or the high input line voltage condition.

Optional Resistor between IAC and VCC:
This resistor is about 100K ohm, it can improve the THD of the input current at high line and light load

ISENSE (Pin 3)
This pin ties to a resistor which senses the PFC input current. This signal should be negative with respect to the IC ground. It internally feeds the pulse-by-pulse current limit comparator and the current sense feedback signal. The ILIMIT trip level is $-1V$. The ISENSE feedback is internally multiplied by a gain of four and compared against the internal programmed ramp to set the PFC duty cycle. The intersection of the boost inductor current downslope with the internal programming ramp determines the boost off-time.

It requires a RC filter between ISENSE and PFC boost sensing resistor.

VEAO (Pin 4)
This is the PFC slew rate enhanced transconductance amplifier output which needs to connected with a compensation network Ground.

VFB (Pin 5)
Besides this is the PFC slew rate enhanced transconductance input, it also tie to a couple of protection comparators, PFCOVP, and PFC PFC On-Off Detect

PFC On-Off (Pin 6)
Current information, the optocouple goes into PFC On-Off pin. Therefore, it is the SUM Amplifier input.
Soft Start can be triggered by the following conditions:
1.) During the startup (VCC is less than 10V)
2.) DC to DC short (PFC On-Off is greater thanVCC-0.7V)

VCC (Pin 7)

VCC is the power input connection to the IC. The VCC start-up current is 100uA. The no-load ICC current is 2mA. VCC quiescent current will include both the IC biasing currents and the PFC output current. Given the operating frequency and the MOSFET gate charge (Qg), average PFC and PWM output currents can be calculated as IOUT = Qg x F. The average magnetizing current required for any gate drive transformers must also be included. The VCC pin is also assumed to be proportional to the PFC output voltage. Internally it is tied to the VCC OVP comparator (17.9V) providing redundant high-speed over-voltage protection (OVP) of the PFC stage. VCC also ties internally to the UVLO circuitry and VREFOK comparator, enabling the IC at 13V and disabling it at 10V. VCC must be bypassed with a high quality ceramic bypass capacitor placed as close as possible to the IC. Good bypassing is critical to the proper operation of the CM6510C.

VCC is typically produced by an additional winding off the boost inductor or PFC Choke, providing a voltage that is proportional to the PFC output voltage. Since the VCC OVP max voltage is 17.9V, an internal shunt limits VCC overvoltage to an acceptable value. An external clamp, such as shown in Figure 1, is desirable but not necessary.
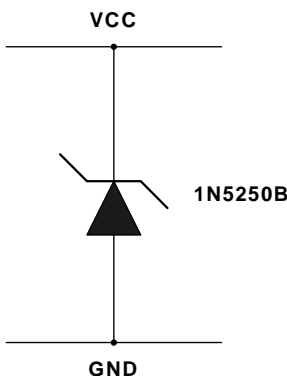

Figure 1. Optional VCC Clamp

This limits the maximum VCC that can be applied to the IC while allowing a VCC which is high enough to trip the VCC OVP. An RC filter at VCC is required between boost trap winding and VCC.

PFCOUT (Pin 8)

PFC OUT is the high-current power driver capable of directly driving the gate of a power MOSFET with peak currents up to -1A and +0.5A. Both outputs are actively held low when VCC is below the UVLO threshold level which is 15V or VREFOK comparator is low.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6510C uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero.

By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VFB, to allow for a high line of 270VAC$_{rms}$. The other condition is that the current that the converter is allowed to draw from the line at any given instant must be proportional to the line voltage.

PFC Control: Leading Edge Modulation with Input Current Shaping Technique (I.C.S.T.)

The only differences between the conventional PFC control topology and I.C.S.T. is:
the current loop of the conventional control method is a close loop method and it requires a detail understanding about the system loop gain to design. With I.C.S.T., since the current loop is an open loop, it is very straightforward to implement it.

The end result of the any PFC system, the power supply is like a pure resistor at low frequency. Therefore, current is in phase with voltage.
In the conventional control, it forces the input current to follow the input voltage. In CM6510C, the chip thinks if a boost converter needs to behave like a low frequency resistor, what the duty cycle should be.

The following equations is CM6510C try to achieve:

$$R_e = V_{in}\big/I_{in} \tag{1}$$

$$\bar{I}_l = I_{in} \tag{2}$$

Equation 2 means: average boost inductor current equals to input current.

$$\therefore V_{in} \times \bar{I}_l \approx V_{out} \times \bar{I}_d \tag{3}$$

Therefore, input instantaneous power is about to equal to the output instantaneous power.

For steady state and for the each phase angle, boost converter DC equation at continuous conduction mode is:

$$V_{out}\big/V_{in} = 1\big/(1-d) \tag{4}$$

Rearrange above equations, (1), (2),(3), and (4) in term of Vout and d, boost converter duty cycle and we can get average boost diode current equation (5):

$$\bar{I}_d = (1-d)^2 \times V_{out}\big/R_e \tag{5}$$

Also, the average diode current can be expressed as:

$$\bar{I}_d = \frac{1}{T_{sw}} \int_0^{T_{off}} I_d(t) \cdot dt \tag{6}$$

If the value of the boost inductor is large enough, we can assume $I_d(t) \sim I_d$. It means during each cycle or we can say during the sampling, the diode current is a constant.

Therefore, equation (6) becomes:

$$\bar{I}_d = I_d \times t_{off}\big/T_{sw} = I_d \times d' = I_d \times (1-d) \tag{7}$$

Combine equation (7) and equation (5), and we get:

$$I_d \times d' = (d')^2 \times V_{out}\big/R_e$$

$$\therefore I_d = d' \times V_{out}\big/R_e \tag{8}$$

$$\therefore I_d = \frac{V_{out}}{R_e} \times \frac{t_{off}}{T_{sw}}$$

From this simple equation (8), we implement the PFC control section of the CM6510C.

Leading/Trailing Modulation

Conventional Pulse Width Modulation techniques employ trailing edge modulation in which the switch will turn ON right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 2 shows a typical trailing edge control scheme.

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch. Figure 3 shows a leading edge control scheme.
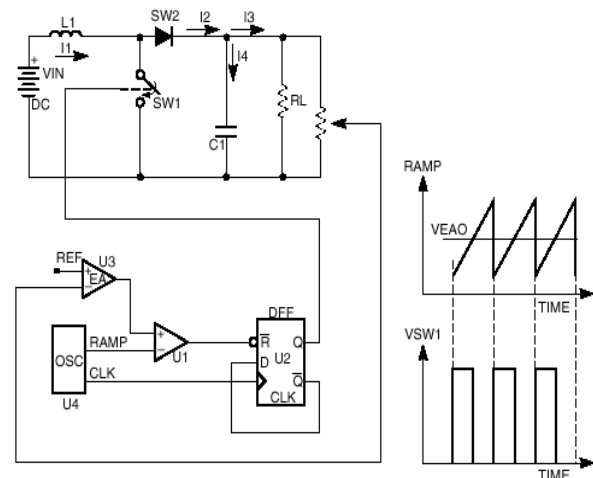

Figure 2. Typical Trailing Edge Control Scheme.

One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns OFF and switch 2 (SW2) turns ON at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method, substantially reducing dissipation in the high-voltage PFC capacitor.

Typical Applications
PFC Section:
PFC Voltage Loop Error Amp, VEAO
The ML4803 utilizes an one pin voltage error amplifier in the PFC section (VEAO). In the CM6510C, it is using the slew rate enhanced transconductance amplifier, which is the same as error amplifier in the CM6800. The unique transconductance profile can speed up the conventional transient response by 10 times. The internal reference of the VEAO is 2.5V. The input of the VEAO is VFB pin.

PFC Voltage Loop Compensation
The voltage-loop bandwidth must be set to less than 120Hz to limit the amount of line current harmonic distortion. A typical crossover frequency is 30Hz.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GM_V: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

ΔV_{EAO}: This is the necessary change of the VEAO to deliver the designed average input power. The average value is 6V-3V=3V since when the input line voltage increases, the delta VEAO will be reduced to deliver the same to the output. To over compensate, we choose the delta VEAO is 3V.

Internal Voltage Ramp
The internal ramp current source is programmed by way of VEAO pin voltage. When VEAO increases the ramp current source is also increase. This current source is used to develop the internal ramp by charging the internal 30pF +12/-10% capacitor. The frequency of the internal programming ramp is set internally to 67kHz.

Design PFC ISENSE Filtering
ISENSE Filter, the RC filter between Rs and ISENSE:

There are 2 purposes to add a filter at ISENSE pin:
1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs, which is the sensing resistor of the PFC boost converter. It requires the ISENSE Filter to attenuate the energy.
2.) Reduce L, the Boost Inductor: The ISENSE Filter also can reduce the Boost Inductor value since the ISENSE Filter behaves like an integrator before going ISENSE which is the input of the current error amplifier, IEAO.
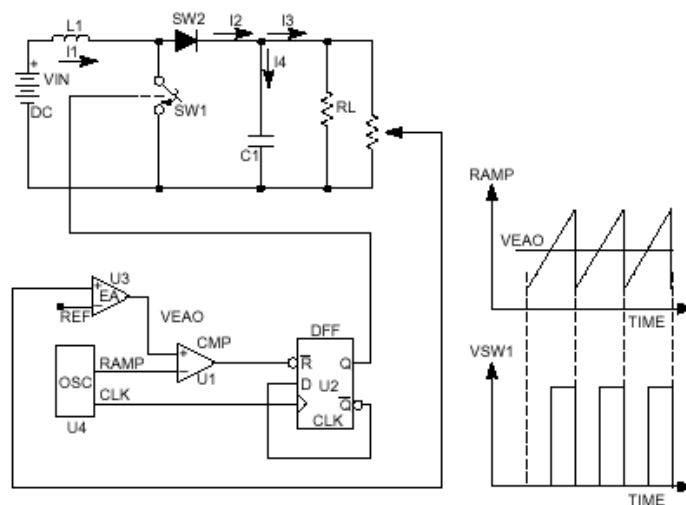

Figure 3 Typical Leading Edge Control Scheme

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm. By selecting R_{FILTER} equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 283nF.

IAC, R_{AC}, Automatic Slope Compensation, DCM at high line and light load, and Startup current

There are 4 purposes for IAC pin:
1.) For the leading edge modulation, when the duty cycle is less than 50%, it requires the similar slope compensation, as the duty cycle of the trailing edge modulation is greater than 50%. In the CM6510C, it is a relatively easy thing to design. Use an more than 2KK ohm resistor, R_{AC} to connect IAC pin and the rectified line voltage. It will do the automatic slope compensation. If the input boost inductor is too small, the R_{AC} may need to be reduced more.
2.) During the startup period, Rac also provides the initial startup current, 100uA;therefore, the bleed resistor is not needed.
3.) Since IAC pin with R_{AC} behaves as a feedforward signal, it also enhances the signal to noise ratio and the THD of the input current.
4.) It also will try to keep the maximum input power to be constant. However, the maximum input power will still go up when the input line voltage goes up.

Start Up of the system, UVLO, VREFOK and Soft Start

During the Start-up period, R_{AC} resistor will provide the start up current~100uA from the rectified line voltage to IAC pin. Inside of CM6510C during the start-up period, IAC is connected to VCC until the VCC reaches UVLO voltage which is 13V (UVB) and internal reference voltage is stable, it will disconnect itself from VCC. During the Start up, the soft start function is triggered and the duration of the soft start will last around 10mS.

PFC section wakes up after Start up period

After Start up period, PFC section will softly start since VEAO is zero before the start-up period. Since VEAO is a slew rate enhanced transconductance amplifier (see figure 3), VEAO has a high impedance output like a current source and it will slowly charge the compensation net work which needs to be designed by using the voltage loop gain equation.
Before PFC boost output reaches its design voltage, it is around 380V and VFB reaches 2.5V, PWM section is off.

PFC OVP Comparator

PFC OVP Comparator sense VFB pin which is the same the voltage loop input. The good thing is the compensation network is connected to VEAO. The PFC OVP function is a relative fast OVP. It is not like the conventional error amplifier which is an operational amplifier and it requires a local feedback and it make the OVP action becomes very slow.
The threshold of the PFC OVP is 2.5V+10% =2.75V with 250mV hysteresis.

PFC On-Off Detect Comparator

To improve power supply reliability, reduce system component count, and simplify compliance to UL1950 safety standards, the CM6510C includes PFC On-Off Detect. This feature monitors VFB (Pin 5) for certain PFC fault conditions.

In case of a feedback path failure, the output of the PFC could go out of safe operating limits. With such a failure, VFB will go outside of its normal operating area. Should VFB go too low, too high, or open, PFC On-Off Detect senses the error and terminates the PFC output drive.

PFC On-Off detect is an entirely internal circuit. It requires no external components to serve its protective function.

VCC OVP and generate VCC

For the CM6510C system, if VCC is generated from a source that is proportional to the PFC output voltage and once that source reaches 17.9V, PFCOUT, PFC driver will be off.

The VCC OVP resets once the VCC discharges below 16.4V, PFC output driver is enabled. It serves as redundant PFC OVP function.
Typically, there is a bootstrap winding off the boost inductor. The VCC OVP comparator senses when this voltage exceeds 17.9V, and terminates the PFC output drive. Once the VCC rail has decreased to below 16.4V the PFC output drive be enabled. Given that 16V on VCC corresponds to 380V on the PFC output, 17.9V on VCC corresponds to an OVP level of 460V.
It is a necessary to put RC filter between bootstrap winding and VCC. For VCC=15V, it is sufficient to drive either a power MOSFET or a IGBT.

UVLO

The UVLO threshold is 13V providing 3V hysteresis.

PFCOUT

PFCOUT is CMOS drivers. It has adaptive anti-shoot through to reduce the switching loss. Its pull-up is a 30ohm PMOS driver and its pull-down is a 15ohm NMOS driver. It can source 0.5A and sink 1A if the VCC is above 15V.

PFC On-Off

When PFC On-Off is less than (VCC-1.4V)/2, CM6510C will turn off PFC. Usually; it means load has been reduced to a level, which is the level of the Green Mode threshold. Usually, we set the Green Mode threshold around 20% of the full load.

After turning off PFC, the efficiency will be increased due to the input voltage is higher and less switching events.
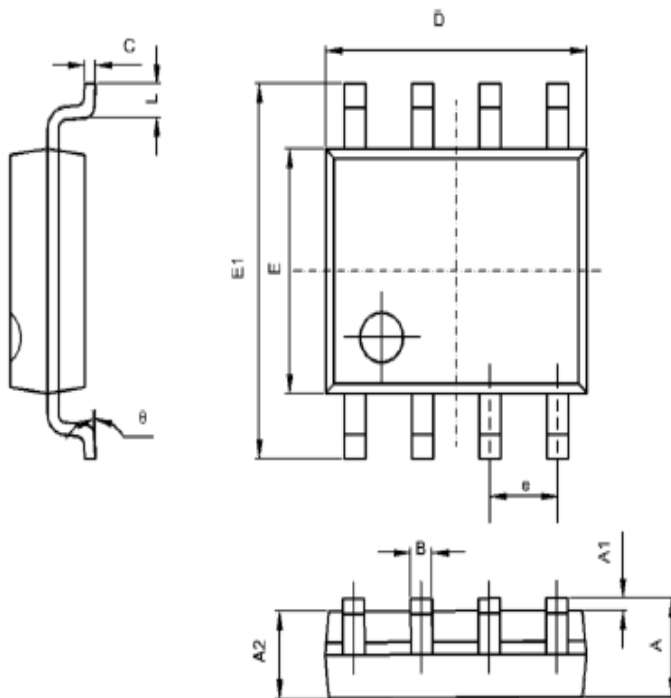
Component Reduction

Components associated with the VRMS and IEAO pins of a typical PFC controller such as the CM6800 have been eliminated. The PFC power limit and bandwidth does vary with line voltage.

APPLICATION CIRCUIT
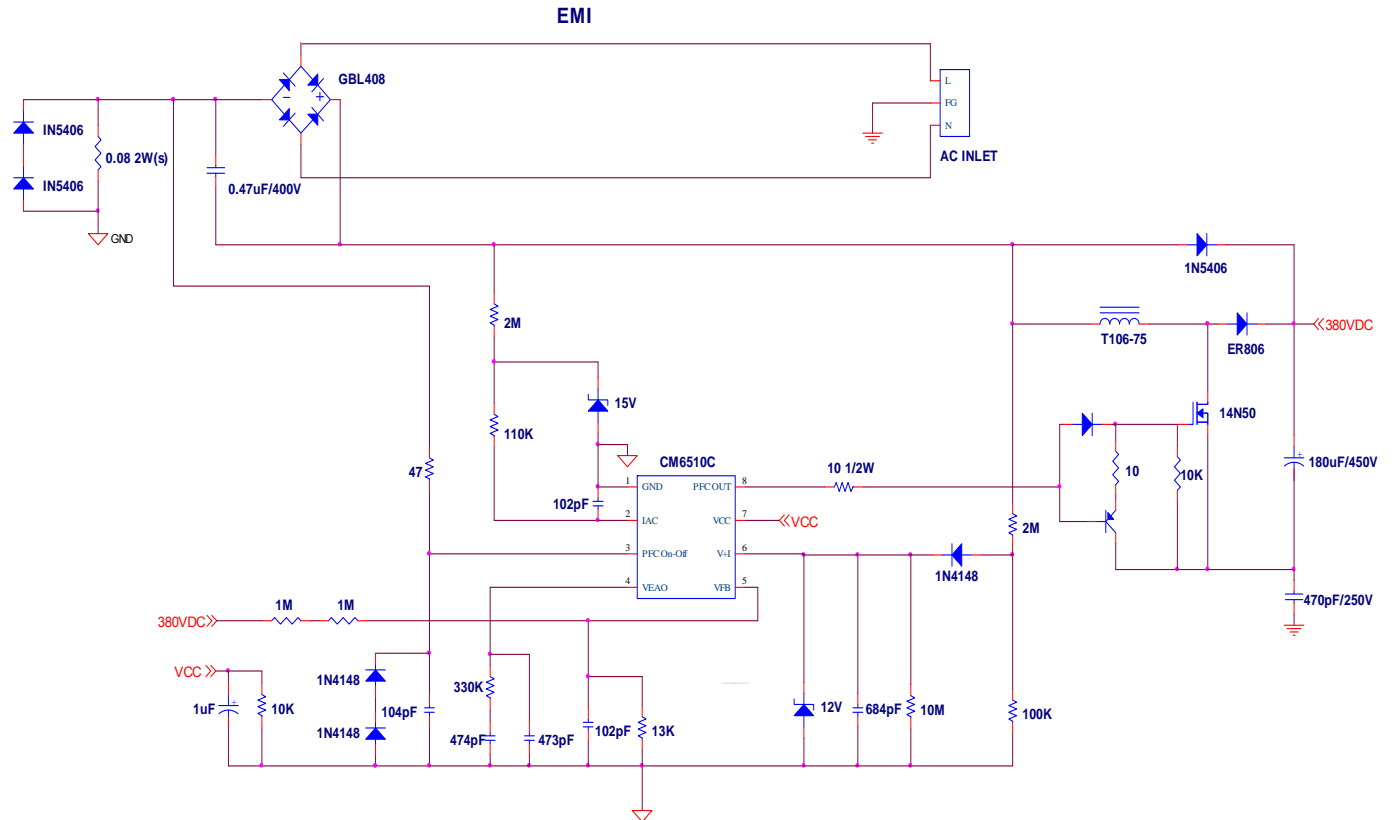
PACKAGE DIMENSION

8-PIN SOP (S08)

SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE

Champion Microelectronic Corporation (CMC) reserves the right to make changes to its products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage.   CMC integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications.   Use of CMC products in such applications is understood to be fully at the risk of the customer.   In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

HsinChu Headquarter

5F, No. 11, Park Avenue II,
Science-Based Industrial Park,
HsinChu City, Taiwan

T E L : +886-3-567 9979
F A X : +886-3-567 9909
http://www.champion-micro.com

Sales & Marketing

21F., No. 96, Sec. 1, Sintai 5th Rd., Sijhih City,
Taipei County 22102,
Taiwan, R.O.C.

T E L : +886-2-2696 3558
F A X : +886-2-2696 3559