MP8775

CMOS
20 MSPS, 8-Bit, High Speed
Analog-to-Digital Converter

March 1999-4

FEATURES

- 8-Bit Resolution
- 20 MHz Sampling Rate
- DNL = ±1/2 LSB, INL = ±1 LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 85 mW typ. (excluding reference)
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- Power Down Available: MP8776
- 3 V Version: MP87L75
- Small 20 Pin SOIC Package

APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD s Based Systems
- Hardware Scanners
- Video Capture Boards

GENERAL DESCRIPTION

The MP8775 is an 8-bit Analog-to-Digital Converter in a small 20 pin SOIC package. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

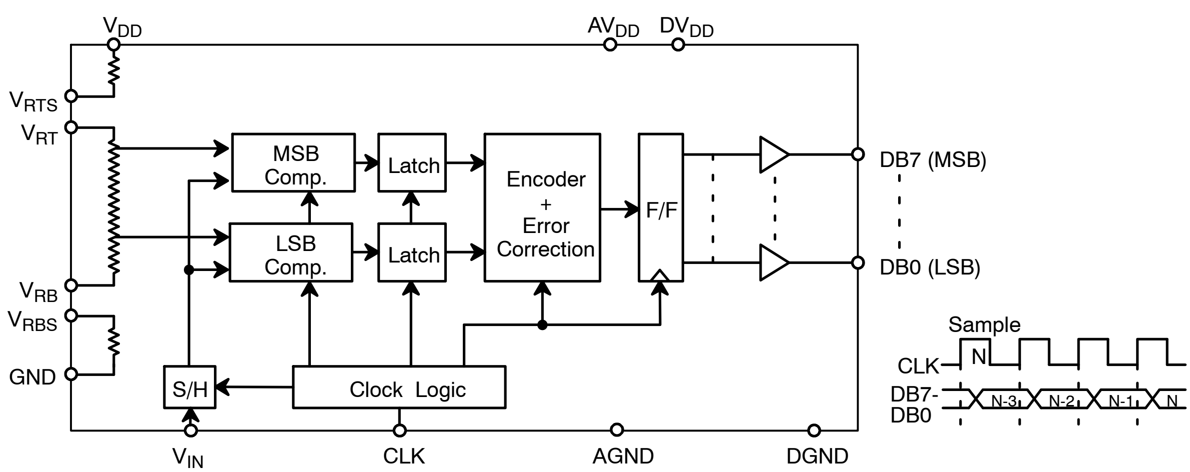
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8775 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces kickback and eases the requirements of the buffer/amplifier used to drive the MP8775.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 V supply. Power consumption is 85 mW at F_s = 20 MHz.

Specified for operation over the commercial / industrial (−40 to +85°C) temperature range, the MP8775 is available in Surface Mount (SOIC), Shrunk Small Outline (SSOP) and Plastic dual-in-line (PDIP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



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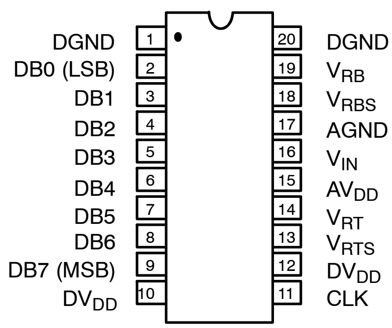
ORDERING INFORMATION

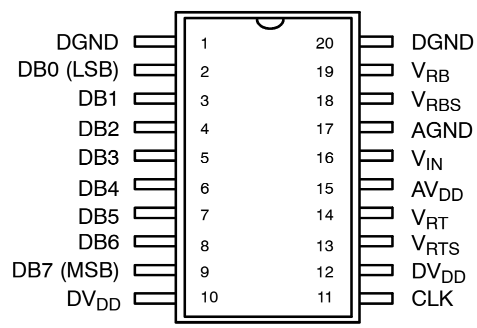
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP8775AS	±3/4	±1 1/2
PDIP	–40 to +85°C	MP8775AN	±3/4	±1 1/2
SSOP	–40 to +85°C	MP8775AQ	±3/4	±1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300)



20 Pin SOIC (Jedec, 0.300)
20 Pin SSOP

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Generates 2.6 V if tied to V_{RT}
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Generates 0.6 V if tied to V_{RB}
19	V_{RB}	Bottom Reference
20	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, FS = 15 MHz (50% Duty Cycle), $V_{RT} = 2.6$ V, $V_{RB} = 0.6$ V, $T_A = 25°C$

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Maximum Sampling Rate	FS	15	20		MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±3/4	LSB	@ 15 MHz
Differential Non-Linearity	DNL			±1/2	LSB	@ 10 MHz
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±3		LSB	
Full Scale Error	EFS		±3		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	550	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.6		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		2		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		2.3		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		50		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}		10		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4.0			V	
Logical "0" Voltage	V_{IL}			1.0	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		μA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS	50			ns	
High Pulse Width	t_{PWH}	25			ns	
Low Pulse Width	t_{PWL}	25			ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Data Valid Delay[2, 8]	t_{DL}		20	25	ns	
Data Hold Time	t_{HL}		12	15	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT D)

Description	Symbol	Min	25°C Typ	Max	Units	Conditions
AC PARAMETERS						
Differential Gain Error	d_G		2		%	FS = 4 x NTSC
Differential Phase Error	d_{PH}		1		°	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		17	25	mA	Does not include ref. current

Notes:

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (Figure 2.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 3.). Accuracy is a function of the sampling rate (FS).*

2 *Guaranteed. Not tested.*

3 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

4 *−1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} input equivalent circuit (Figure 4.). Switched capacitor analog input requires driver with low output resistance.*

6 *All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.*

7 *t_R, t_F should be limited to >5 ns for best results.*

8 *Depends on the RC load connected to the output pin.*

9 *AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . 7 V
V_{RT} & V_{RB} . . . . V_{DD} +0.5 to GND −0.5 V
V_{IN} . . . . V_{DD} +0.5 to GND −0.5 V
All Inputs . . . . V_{DD} +0.5 to GND −0.5 V
All Outputs . . . . V_{DD} +0.5 to GND −0.5 V

Storage Temperature . . . . −65 to +150°C
Lead Temperature (Soldering 10 seconds) . . . . +300°C
Package Power Dissipation Rating @ 75°C
SOIC, SSOP, PDIP . . . . 700 mW
Derates above 75°C . . . . 9 mW/°C

Notes:

1 *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

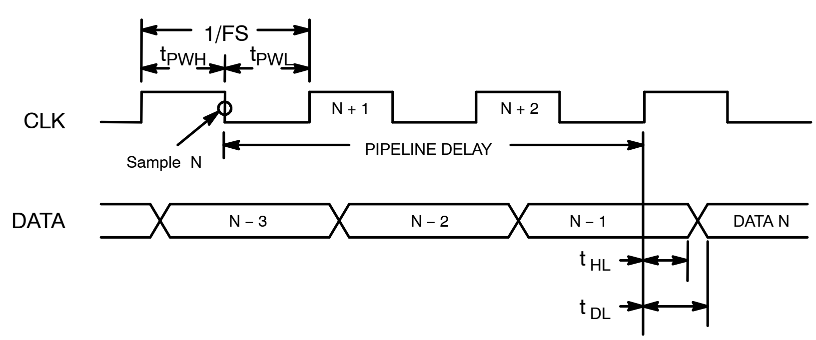
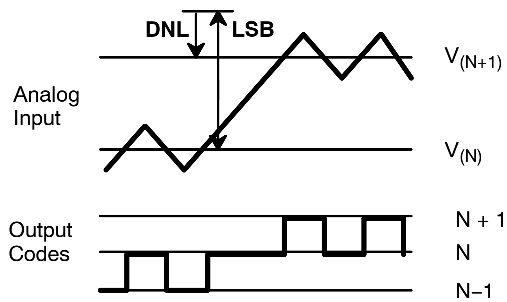


Figure 1. MP8775 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)}$ = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 2. DNL Measurement

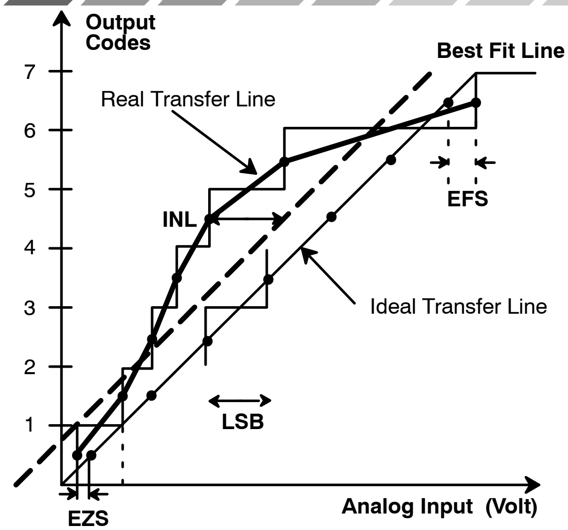


Figure 3. INL Error Calculation

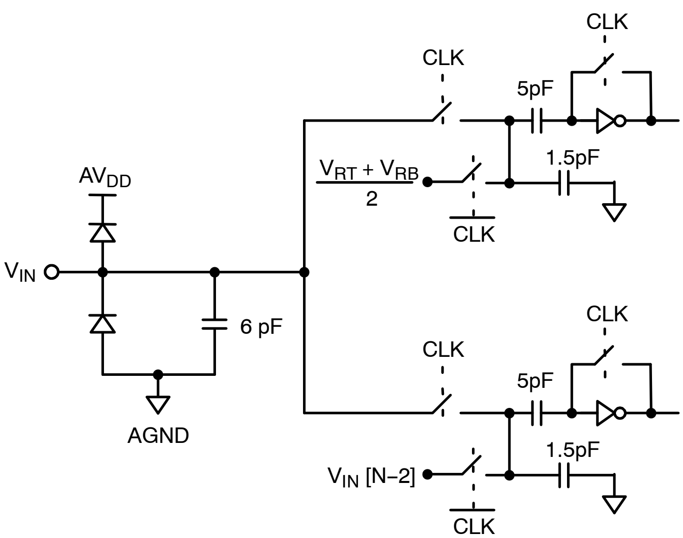


Figure 4. Equivalent Input Circuit

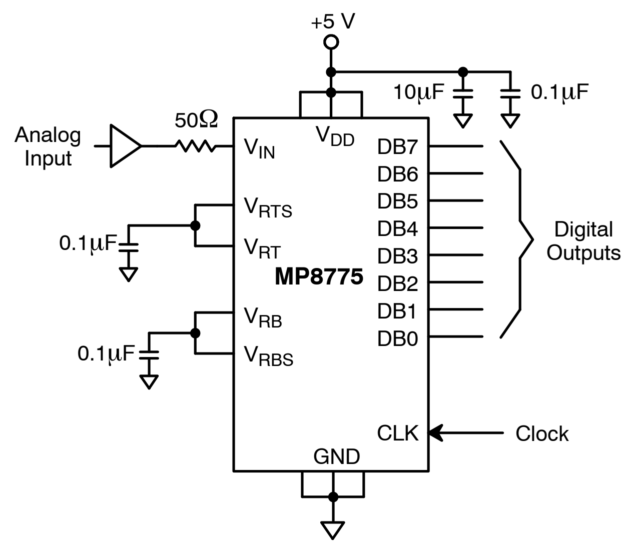


Figure 5. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V or DV_{DD} +0.5 V or DGND –0.5 V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

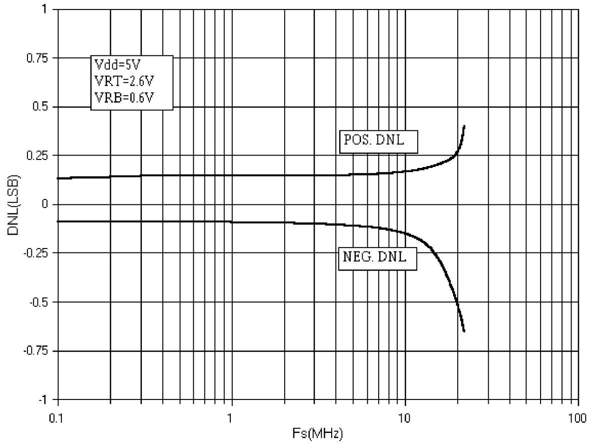
The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 14 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP8775 to other parts of the system.

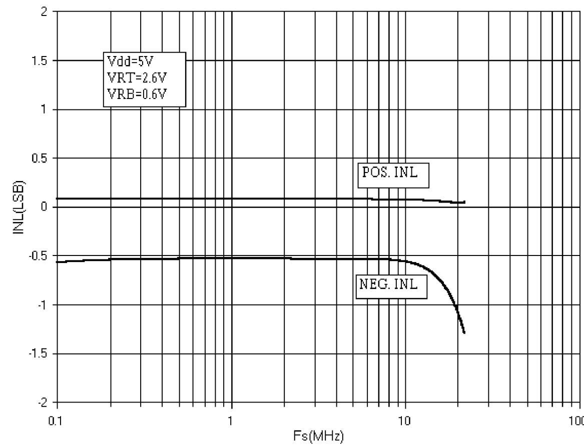
The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 5.).*

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

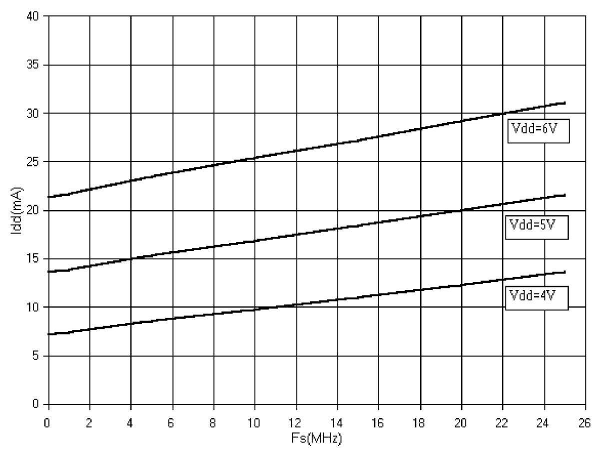
PERFORMANCE CHARACTERISTICS



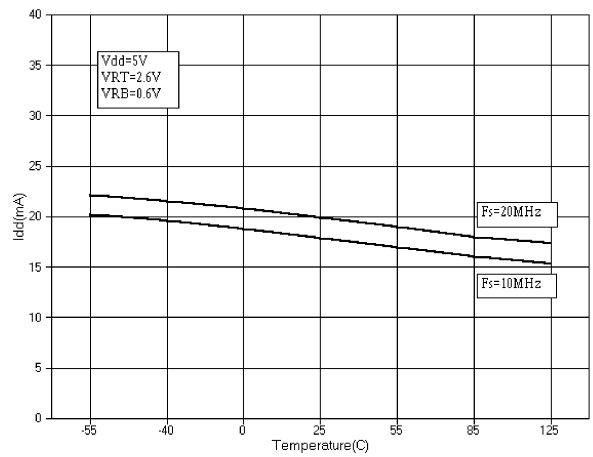
Graph 1. DNL vs. Sampling Frequency



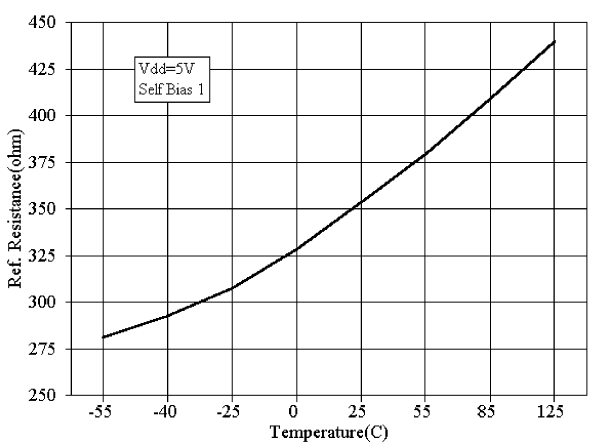
Graph 2. INL vs. Sampling Frequency



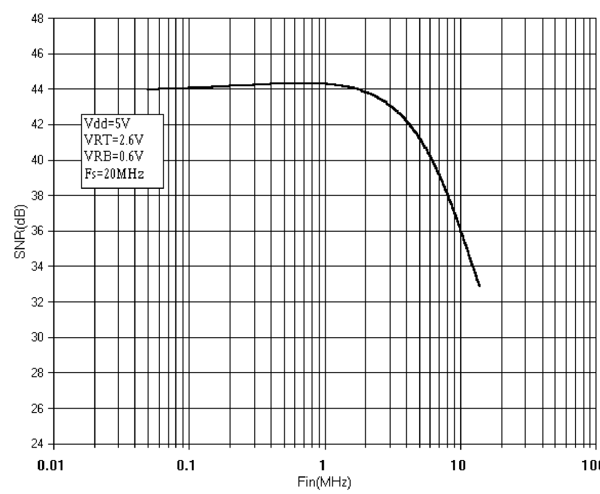
Graph 3. Supply Current vs. Sampling Frequency



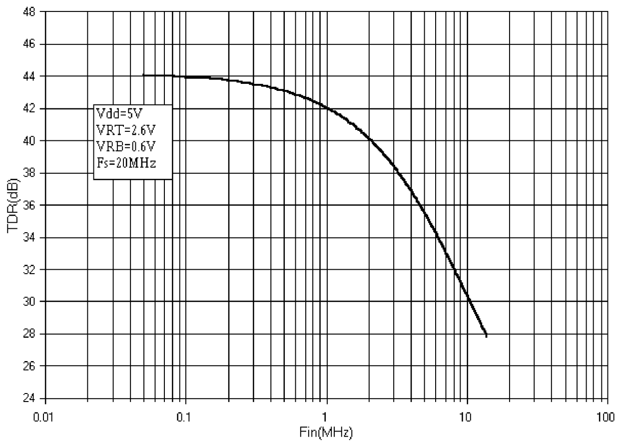
Graph 4. Supply Current vs. Temperature



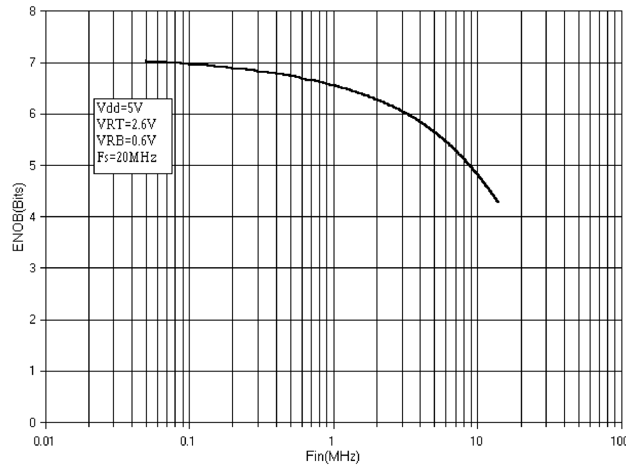
Graph 5. Reference Resistance vs. Temperature



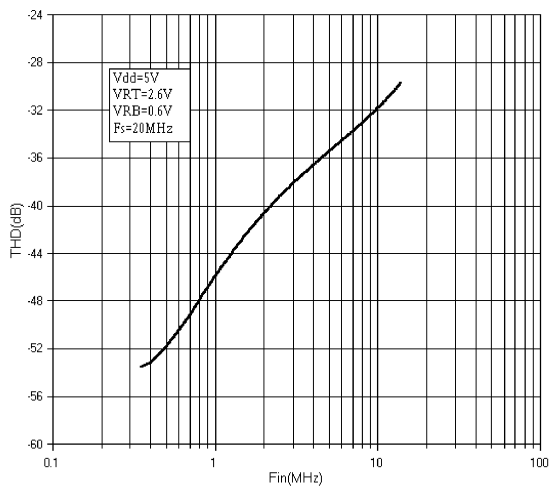
Graph 6. SNR vs. Input Frequency



Graph 7. SINAD vs. Input Frequency



Graph 8. ENOB vs. Input Frequency



Graph 9. THD vs. Input Frequency