FEDL9207-02
Issue Date: May 17, 2005

OKI Semiconductor

ML9207-xx

5 × 7 Dot Character × 24-Digit Display Controller/Driver with Character RAM

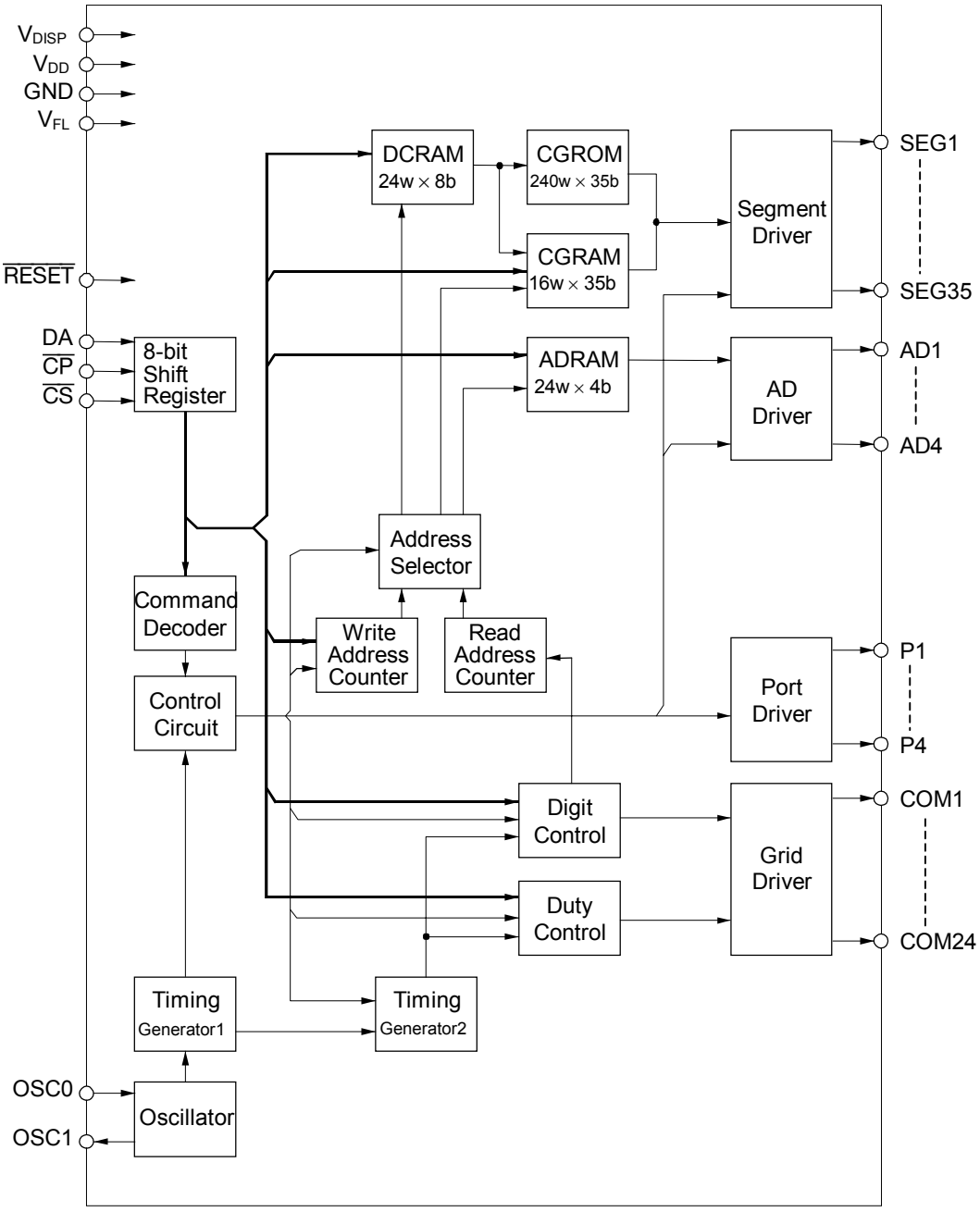
GENERAL DESCRIPTION

The ML9207-xx is a dot matrix vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols.
Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller.
A display system is easily realized by internal ROM and RAM for character display.
The ML9207-xx has low power consumption since it is made by CMOS process technology.
-01 is available as a general-purpose code.
Custom codes are provided on customer's request.

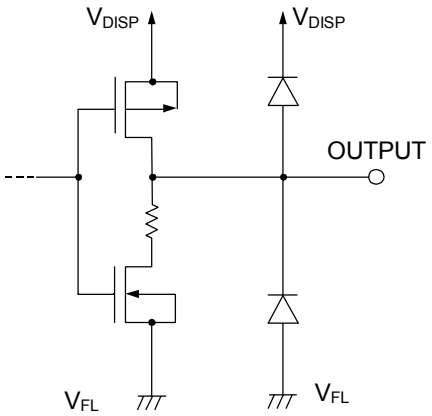
FEATURES

- Logic power supply (V_{DD}) : 3.3 V ±10% or 5.0 V ±10%
- Fluorescent display tube drive power supply (V_{DISP}) : 3.3 V ±10% or 5.0 V ±10%
- Fluorescent display tube drive power supply (V_{FL}) : –20 to –60 V
- VFD driver output current
  (VFD driver output can be connected directly to the fluorescent display tube. No pull-down resistor is required.)
  - Segment driver (SEG1 to SEG35) : –5.0 mA (V_{FL} = –60 V)
  - Segment driver (AD1 to AD4) : –10.0 mA (V_{FL} = –60 V)
  - Grid driver (COM1 to COM24) : –50.0 mA (V_{FL} = –60 V)
- General output port output current
  Output driver (P1 to P4) : ±1.0 mA (V_{DD} = 3.3 V±10%)
  ±2.0 mA (V_{DD} = 5.0 V±10%)
- Content of display
  - CGROM 5 × 7 dots : 240 types (character data)
  - CGRAM 5 × 7 dots : 16 types (character data)
  - ADRAM 24 (display digit) × 4 bits (symbol data)
  - DCRAM 24 (display digit) × 8 bits (register for character data display)
  - General output port 4 bits (static operation)
- Display control function
  - Display digit : 9 to 24 digits
  - Display duty (brightness adjustment) : 0/1024 to 960/1024
  - All lights ON/OFF
- 4 interfaces with microcontroller : DA, $\overline{CS}$, $\overline{CP}$, $\overline{RESET}$
- 1-byte instruction execution (excluding data write to RAM and Display duty set)
- Built-in oscillation circuit
  - Crystal oscillation or ceramic oscillation
- Package options:
  80-pin QFP package (QFP80-P-1414-0.65-K) (Product name : ML9207-xxGP)
  80-pin QFP package (QFP80-P-1420-0.80-BK) (Product name : ML9207-xxGA)
  xx indicates the code number.

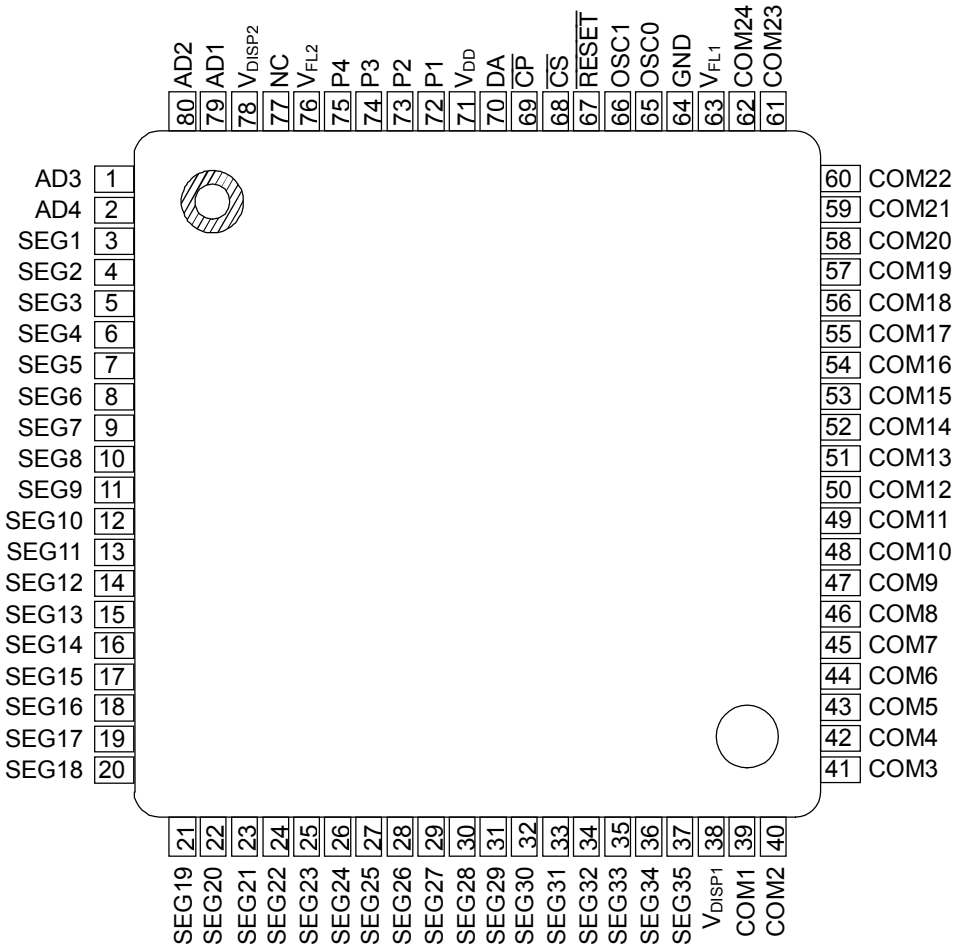
BLOCK DIAGRAM



SCHEMATIC DIAGRAM OF DRIVER OUTPUT CIRCUIT

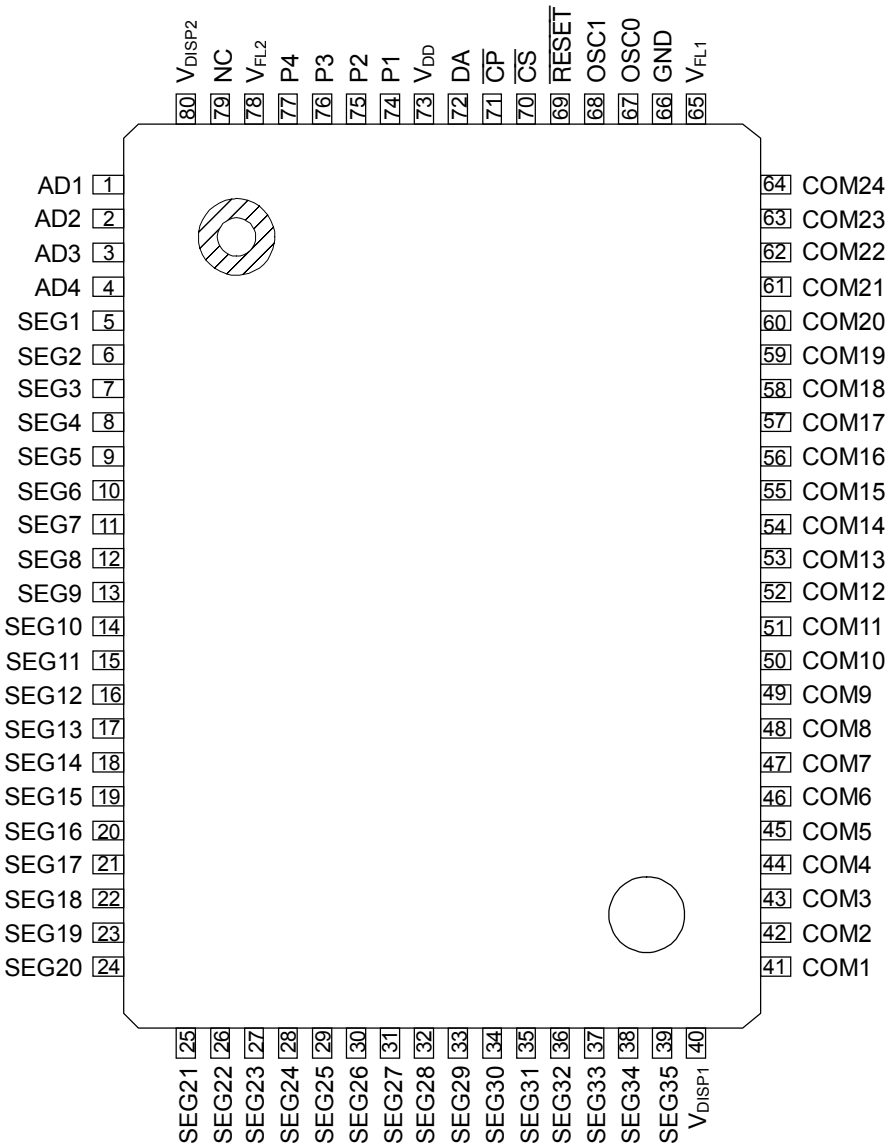


PIN CONFIGURATION (TOP VIEW)



NC: No connection

80-Pin Plastic QFP
(QFP80-P-1414-0.65-K)



NC: No connection

80-Pin Plastic QFP
(QFP80-P-1420-0.80-BK)

PIN DESCRIPTION

Pin		Symbol	Type	Connects to	Description
QFP-1 *	QFP-2*				
3 to 37	5 to 39	SEG1 to 35	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –5.0 mA
39 to 62	41 to 64	COM1 to 24	O	Fluorescent tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –50.0 mA
1, 2, 79, 80	1 to 4	AD1 to AD4	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –10.0 mA
72 to 75	74 to 77	P1 to P4	O	LED anode electrode	General port output. Output of these pins in static operation, so these pins can drive the LED. I_{OH} > –2.0 mA
71	73	V_{DD}	—	Power supply	V_{DD}-GND are power supplies for internal logic. V_{DISP}-V_{FL} are power supplies for driving fluorescent tubes. Use the same power supply for V_{DD} and V_{DISP}.
38, 78	40, 80	$V_{DISP1\ to\ 2}$			
64	66	GND			
63, 76	65, 78	$V_{FL1\ to\ 2}$			
70	72	DA	I	Microcontroller	Serial data input (positive logic). Input from LSB.
69	71	$\overline{CP}$	I	Microcontroller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
68	70	$\overline{CS}$	I	Microcontroller	Chip select input. Serial data transfer is disabled when $\overline{CS}$ pin is "H" level.
67	69	$\overline{RESET}$	I	Microcontroller	Reset input. "Low" initializes all the functions. Initial status is as follows. • Address of each RAM ... address "00"H • Data of each RAM ..... Content is undefined • Display digit ..... 24 digits • Brightness adjustment .. 0/1024 • All lights ON or OFF ..... OFF mode • All outputs ..... "Low" level
65	67	OSC0	I	Crystal or ceramic resonator	Pins for self-oscillation. (Do not apply external clocks to these pins.) Connect these pins to the crystal and capacitors or to the ceramic resonator and capacitors. The target oscillation frequency is 4.0 MHz. (Note that the device includes the feed back resistor of 1 MΩ) See Application Circuit.
66	68	OSC1	O		

* QFP1 : QFP80-P-1414-0.65-K
QFP2 : QFP80-P-1420-0.80-BK

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage (1)	V_{DD}	*1		–0.3 to +6.5	V
	V_{DISP}	*1		–0.3 to +6.5	V
Supply Voltage (2)	V_{FL}	—		–80 to V_{DISP}+0.3	V
Input Voltage	V_{IN}	—		–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta ≥ 25°C	QFP80-P-1414-0.65-K	637	mW
			QFP80-P-1420-0.80-BK	764	
Storage Temperature	T_{STG}	—		–55 to +150	°C
Output Current	I_{O1}	COM1 to COM24		–60 to 0.0	mA
	I_{O2}	AD1 to AD4		–20 to 0.0	
	I_{O3}	SEG1 to SEG35		–10 to 0.0	
	I_{O4}	P1 to P4		–4.0 to +4.0	

*1: Use the same power supply for V_{DD} and V_{DISP}.

RECOMMENDED OPERATING CONDITIONS

When the power supply voltage is 5V (typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}, V_{DISP}	—	4.5	5.0	5.5	V
Supply Voltage (2)	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.7 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.3 V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	Self-oscillation	3.5	4.0	4.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 24, Self-oscillation	142	163	183	Hz
Operating Temperature	T_{OP}	—	–40	—	+85	°C

When the power supply voltage is 3.3V (typ.)

Parameter	Symbol	Condition	Min.	Typ .	Max.	Unit
Supply Voltage (1)	V_{DD}, V_{DISP}	—	3.0	3.3	3.6	V
Supply Voltage (2)	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.2 V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	Self-oscillation	3.5	4.0	4.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 24, Self-oscillation	142	163	183	Hz
Operating Temperature	T_{OP}	—	–40	—	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics-1

(V_{DD}, V_{DISP} = 5.0 V ±10%, V_{FL} = –60V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.7 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.3 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH} = V_{DD}		–1.0	+1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V		–1.0	+1.0	µA
High Level Output Voltage	V_{OH1}	COM1 to 24	I_{OH1} = –50.0 mA		V_{DISP} –2.0	—	V
	V_{OH2}	AD1 to AD4	I_{OH2} = –10.0 mA		V_{DISP} –1.5	—	V
	V_{OH3}	SEG1 to 35	I_{OH3} = –5.0 mA		V_{DISP} –1.5	—	V
	V_{OH4}	P1 to P4	I_{OH4} = –2.0 mA		V_{DD} –1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1 to 24 AD1 to AD4 SEG1 to 35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1 to P4	I_{OL1} = 2 mA		—	1.0	V
Supply Current	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC}= 4 MHz, no load	Duty = 960/1024 Digit = 1 to 24 All output lights ON	—	6	mA
	I_{DD2}			Duty = 0/1024 Digit = 1 to 9 All output lights OFF	—	5	mA

DC Characteristics-2

(V_{DD}, V_{DISP} = 3.3 V ±10%, V_{FL} = –60 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.8 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.2 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH} = V_{DD}		–1.0	+1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V		–1.0	+1.0	µA
High Level Output Voltage	V_{OH1}	COM1 to 24	I_{OH1} = –50.0 mA		V_{DISP} –2.0	—	V
	V_{OH2}	AD1 to AD4	I_{OH2} = –10.0 mA		V_{DISP} –1.5	—	V
	V_{OH3}	SEG1 to 35	I_{OH3} = –5.0 mA		V_{DISP} –1.5	—	V
	V_{OH4}	P1 to P4	I_{OH4} = –1.0 mA		V_{DD} –1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1 to 24 AD1 to AD4 SEG1 to 35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1 to P4	I_{OL1} = 1 mA		—	1.0	V
Supply Current	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC} = 4 MHz, no load	Duty = 960/1024 Digit = 1 to 24 All output lights ON	—	5	mA
	I_{DD2}			Duty = 0/1024 Digit = 1 to 9 All output lights OFF	—	4	mA

AC Characteristics-1

(V_{DD}, V_{DISP} = 5.0 V ±10%, V_{FL} = –60 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	Self-oscillation		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	Self-oscillation		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller, etc. externally		250	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		t_{OSCON}	—	ns
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Output Slew Rate	t_R	C_I = 100 pF	t_R = 20% to 80%	—	2.0	µs
	t_F		t_F = 80% to 20%	—	2.0	µs
OSC Duty Ratio	du_{OSC}	—		40	60	%
Oscillation Start-up time	t_{OSCON}	—		*1		

*1 t_{OSCON} depends on the type of crystal or resonator.
Refer to characteristic data of crystal or resonator used.

AC Characteristics-2

(V_{DD}, V_{DISP} = 3.3 V ±10%, V_{FL} = –60 V, Ta = –40 to +85°C, unless otherwise specified)

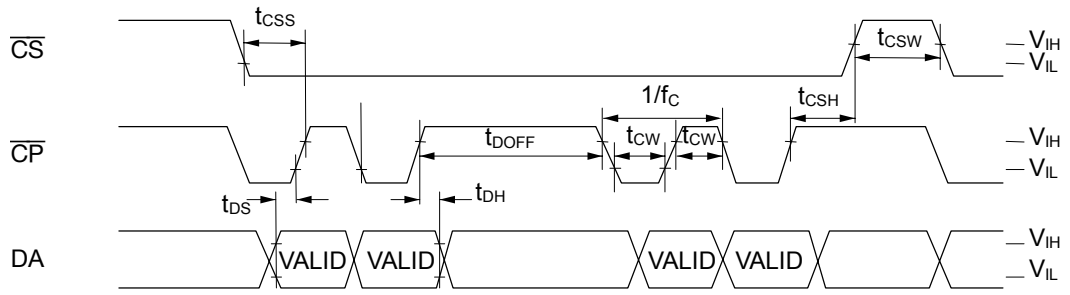
Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	Self-oscillation		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	Self-oscillation		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller, etc. externally		250	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		t_{OSCON}	—	ns
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Output Slew Rate	t_R	C_I = 100 pF	t_R = 20% to 80%	—	2.0	µs
	t_F		t_F = 80% to 20%	—	2.0	µs
OSC Duty Ratio	du_{OSC}	—		40	60	%
Oscillation Start-up time	t_{OSCON}	—		*1		

*1 t_{OSCON} depends on the type of crystal or resonator.
Refer to characteristic data of crystal or resonator used.

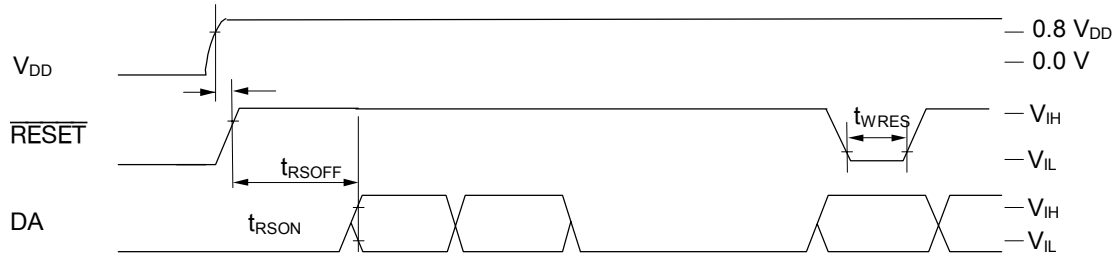
TIMING DIAGRAM

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

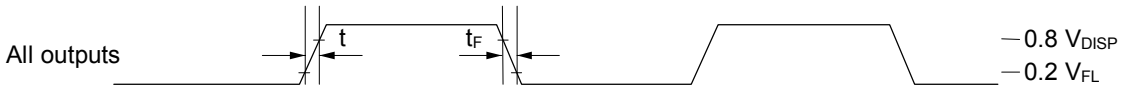
• Data Timing



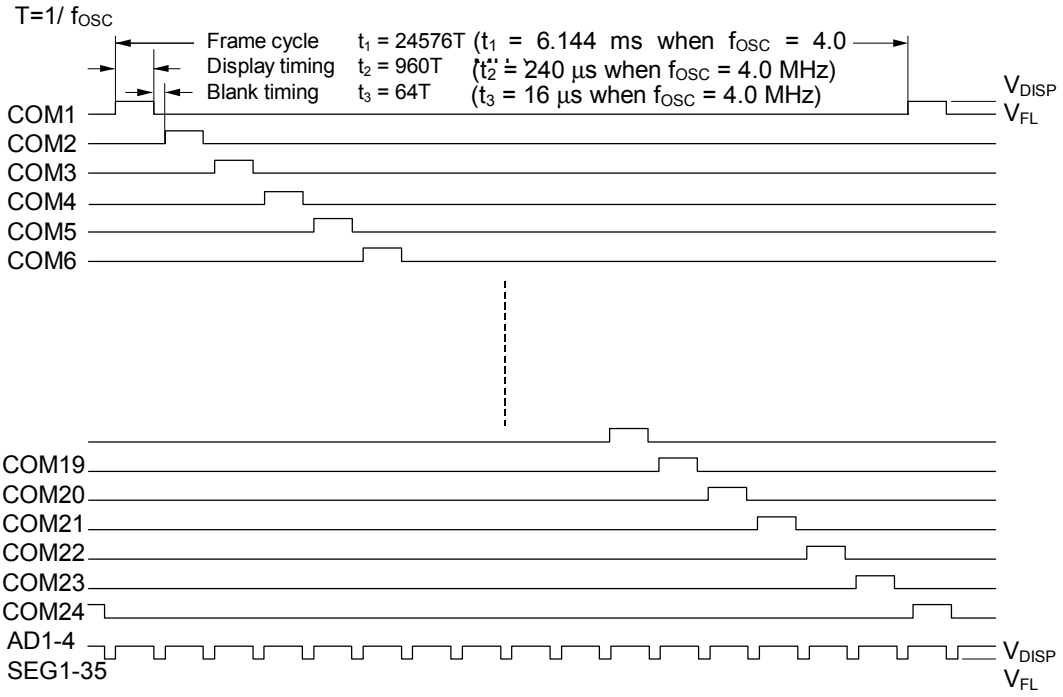
• Reset Timing



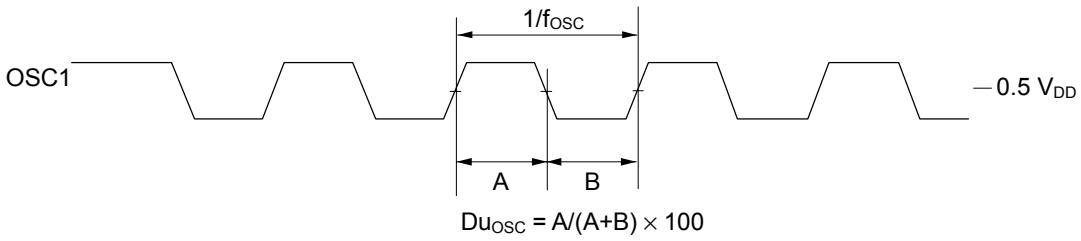
• Output Timing



• Digit Output Timing (for 24-digit display, at a duty of 960/1024)



• OSC Timing



$Du_{OSC} = A/(A+B) \times 100$

FUNCTIONAL DESCRIPTION

Command List

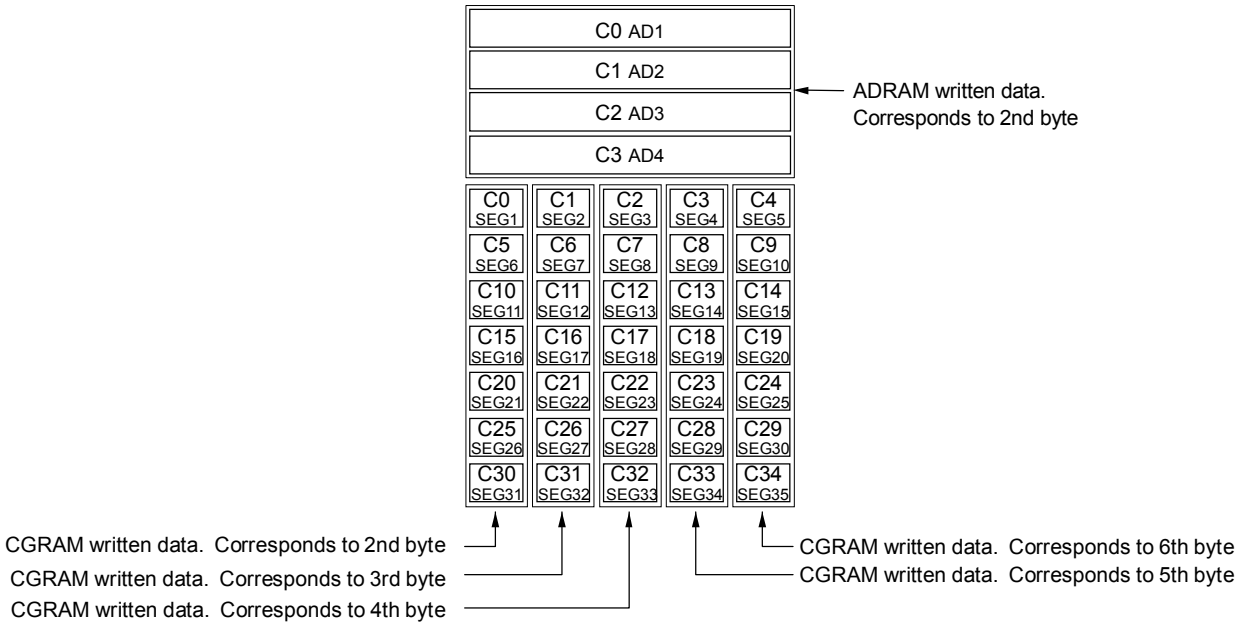
	Command	LSB			1st byte				MSB	LSB			2nd byte				MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM data write	X0	X1	X2	X3	X4	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM data write	X0	X1	X2	X3	*	0	1	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
3	ADRAM data write	X0	X1	X2	X3	X4	1	1	0	C0	C1	C2	C3	*	*	*	*	
4	General output port set	P1	P2	P3	P4	*	0	0	1									
5	Display duty set	D0	D1	*	*	*	1	0	1	D2	D3	D4	D5	D6	D7	D8	D9	
6	Number of digits set	K0	K1	K2	K3	*	0	1	1									
7	All lights ON/OFF	L	H	*	*	*	1	1	1									
	Test mode																	

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
Pn : General output port status specification
Dn : Display duty specification
Kn : Number of digits specification
H : All lights ON instruction
L : All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note : The test mode is used for inspection before shipment.
This is not a user function.

Positional Relationship Between SEGn and ADn (one digit)

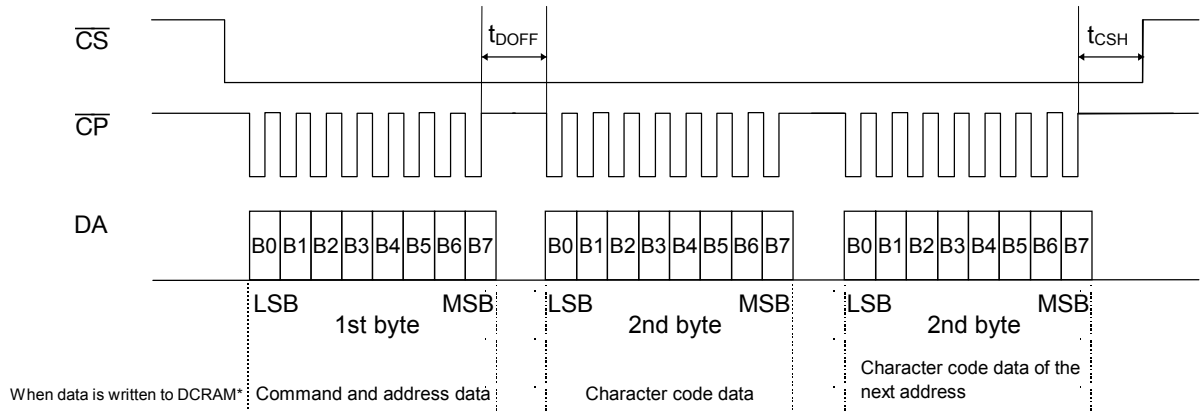


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example) and initializes all functions.
Initial status is as follows:
• Address of each RAM .....Address "00"H
• Data of each RAM.....All contents are undefined
• General output port .....All general output ports (P1 to P4) go "Low"
• Display digit.....24 digits
• Brightness adjustment 0/1024
• All display lights ON or OFF .....OFF mode
• Segment output .....All segment outputs (SEG1 to SEG35) go "Low"
• Common output.....All common outputs (COM1 to COM24) go "Low"
• AD output .....All AD outputs (AD1 to AD4) go "Low"
Please set the functions again according to "Setting Flowchart" after reset.

Description of Commands and Functions

1. DCRAM data write
   (Specifies the addresses 00H to 1FH of DCRAM and writes the character codes of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 5-bit address to store the character codes of CGROM and CGRAM.
The character code specified by DCRAM is converted to a 5 × 7 dot matrix character pattern via CGROM or CGRAM.
(The DCRAM can store 24 characters.)

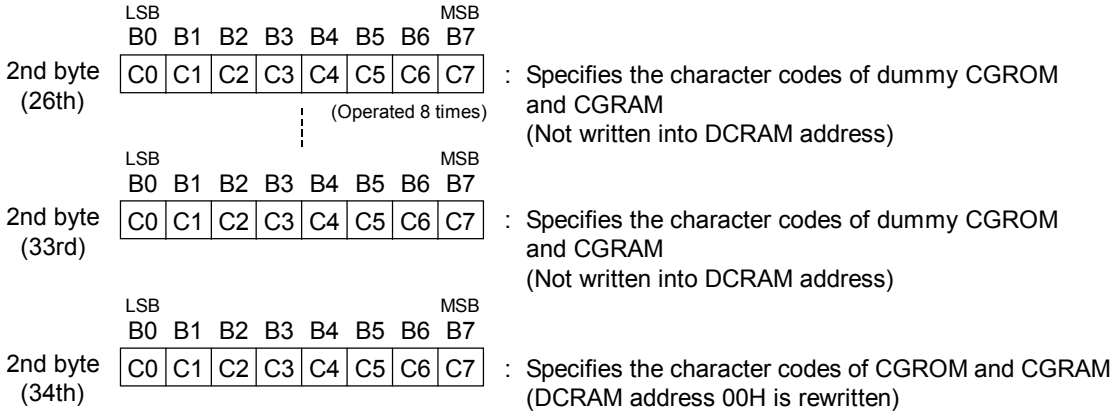
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	X4	1	0	0	: Selects DCRAM data write mode and specifies DCRAM address (Ex: Specifies DCRAM address 00H.)
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	: Specifies the character codes of CGROM and CGRAM (written into DCRAM address 00H)

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character codes as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (3rd)	C0	C1	C2	C3	C4	C5	C6	C7	: Specifies the character codes of CGROM and CGRAM (written into DCRAM address 01H)
2nd byte (4th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specifies the character codes of CGROM and CGRAM (written into DCRAM address 02H)
	⋮								
2nd byte (25th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specifies the character codes of CGROM and CGRAM (written into DCRAM address 17H)

The character code setting of CGROM and CGRAM up to 24 digits is completed.
To set a character code from DCRAM address 00H continuously.
Specify a dummy character code between DCRAM addresses 18H and 1FH.
(To increment the DCRAM address automatically and set it to 00H)



X0 (LSB) to X4 (MSB): DCRAM addresses (5 bits: 24 characters)
C0 (LSB) to C7 (MSB): Character codes of CGROM and CGRAM (8 bits: 256 characters)

[COM positions and set DCRAM addresses]

HEX	X0	X1	X2	X3	X4	COM position	HEX	X0	X1	X2	X3	X4	COM position
00	0	0	0	0	0	COM1	10	0	0	0	0	1	COM17
01	1	0	0	0	0	COM2	11	1	0	0	0	1	COM18
02	0	1	0	0	0	COM3	12	0	1	0	0	1	COM19
03	1	1	0	0	0	COM4	13	1	1	0	0	1	COM20
04	0	0	1	0	0	COM5	14	0	0	1	0	1	COM21
05	1	0	1	0	0	COM6	15	1	0	1	0	1	COM22
06	0	1	1	0	0	COM7	16	0	1	1	0	1	COM23
07	1	1	1	0	0	COM8	17	1	1	1	0	1	COM24
08	0	0	0	1	0	COM9	18	0	0	0	1	1	Not fixed
09	1	0	0	1	0	COM10	19	1	0	0	1	1	Not fixed
0A	0	1	0	1	0	COM11	1A	0	1	0	1	1	Not fixed
0B	1	1	0	1	0	COM12	1B	1	1	0	1	1	Not fixed
0C	0	0	1	1	0	COM13	1C	0	0	1	1	1	Not fixed
0D	1	0	1	1	0	COM14	1D	1	0	1	1	1	Not fixed
0E	0	1	1	1	0	COM15	1E	0	1	1	1	1	Not fixed
0F	1	1	1	1	0	COM16	1F	1	1	1	1	1	Not fixed

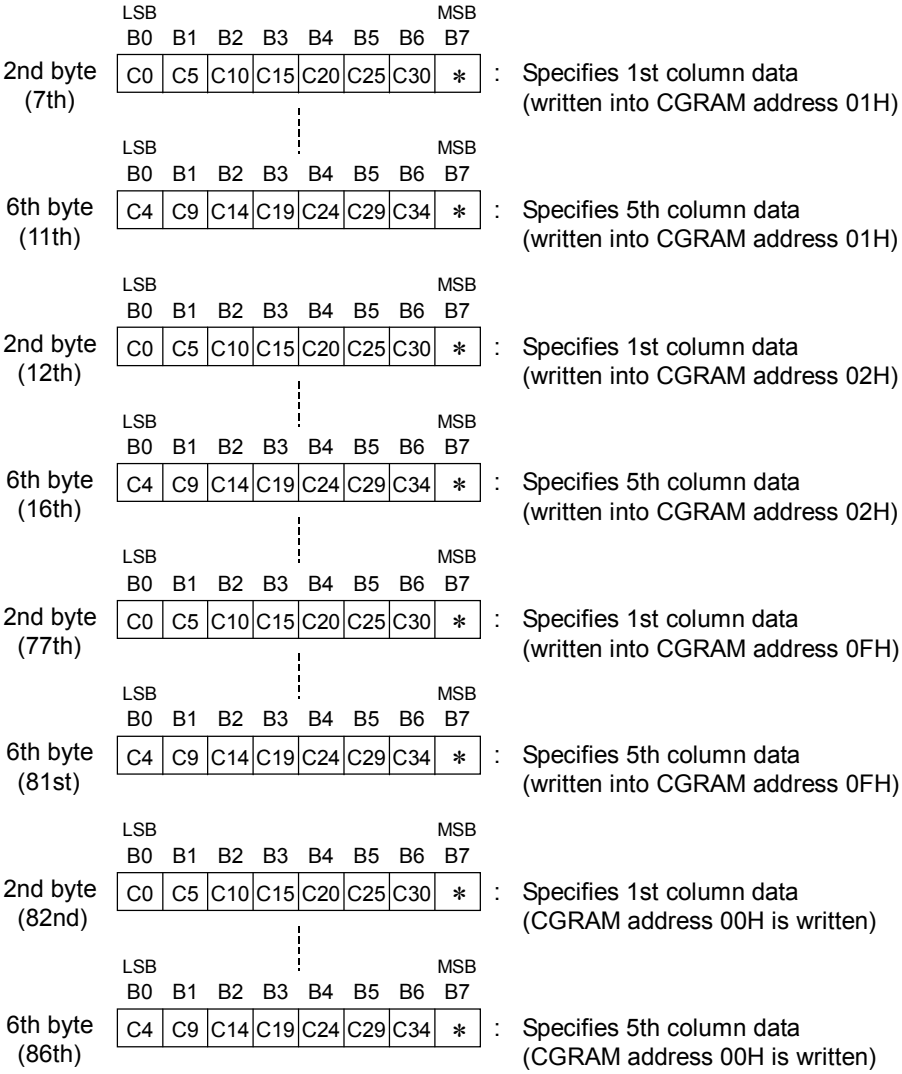
2. CGRAM data write
   (Specifies the addresses of CGRAM and writes character pattern data.)

   CGRAM (Character Generator RAM) has a 4-bit address to store 5 × 7 dot matrix character patterns.
   A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM.
   The address of CGRAM is assigned to 00H to 0FH. (All the other addresses are the CGROM addresses.)
   (The CGRAM can store 16 types of character patterns.)

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	X0	X1	X2	X3	*	0	1	0	:	Selects CGRAM data write mode and specifies CGRAM address. (Ex: Specifies CGRAM address 00H.)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	:	Specifies 1st column data (written into CGRAM address 00H)
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	:	Specifies 2nd column data (written into CGRAM address 00H)
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	:	Specifies 3rd column data (written into CGRAM address 00H)
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	:	Specifies 4th column data (written into CGRAM address 00H)
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	:	Specifies 5th column data (written into CGRAM address 00H)

To specify character pattern data continuously to the next address, specify only character pattern data as follows. The addresses of CGRAM are automatically incremented. Specification of an address is therefore unnecessary. The 2nd to 6th byte (character pattern data) are regarded as one data item, so 250 ns is sufficient for t_{DOFF} time between bytes.



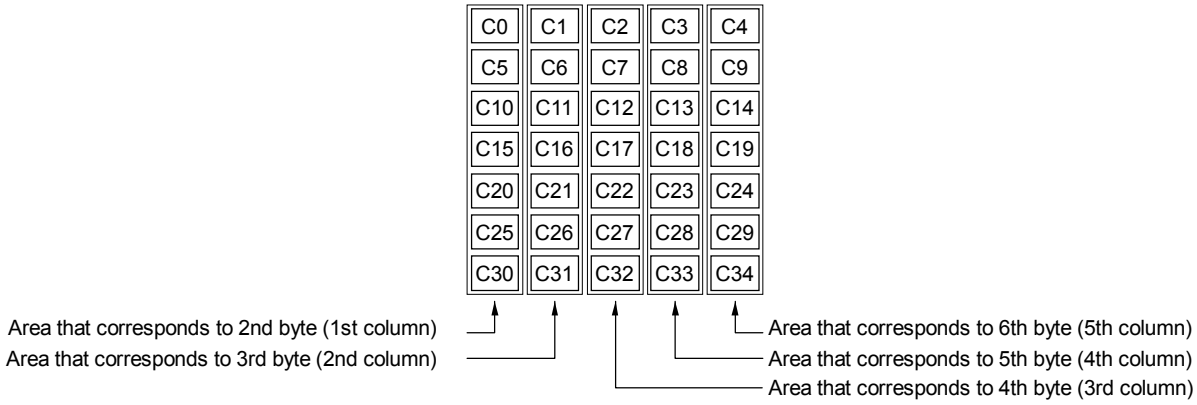
X0 (LSB) to X3 (MSB) : CGRAM addresses (4 bits: 16 characters)
C0 (LSB) to C34 (MSB) : Character pattern data (35 bits: 35 outputs per digit)
* : Don't care

[CGROM addresses and set CGRAM addresses]

Refer to ROMCODE table

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
00	0	0	0	0	RAM00(00000000B)	08	0	0	0	1	RAM08(00001000B)
01	1	0	0	0	RAM01(00000001B)	09	1	0	0	1	RAM09(00001001B)
02	0	1	0	0	RAM02(00000010B)	0A	0	1	0	1	RAM0A(00001010B)
03	1	1	0	0	RAM03(00000011B)	0B	1	1	0	1	RAM0B(00001011B)
04	0	0	1	0	RAM04(00000100B)	0C	0	0	1	1	RAM0C(00001100B)
05	1	0	1	0	RAM05(00000101B)	0D	1	0	1	1	RAM0D(00001101B)
06	0	1	1	0	RAM06(00000110B)	0E	0	1	1	1	RAM0E(00001110B)
07	1	1	1	0	RAM07(00000111B)	0F	1	1	1	1	RAM0F(00001111B)

Positional relationship between the output area of CGROM and that of CGRAM



Note: CGROM (Character Generator ROM) has an 8-bit address to generate 5 × 7 dot matrix character patterns.
CGRAM can store 240 types of character patterns.
General-purpose code -01 is available and custom codes are provided on customer's request.

3. ADRAM data write
(Specifies the addresses 00H to 1FH of ADRAM and writes symbol data.)

ADRAM (Additional Data RAM) has a 5-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store 4 types of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

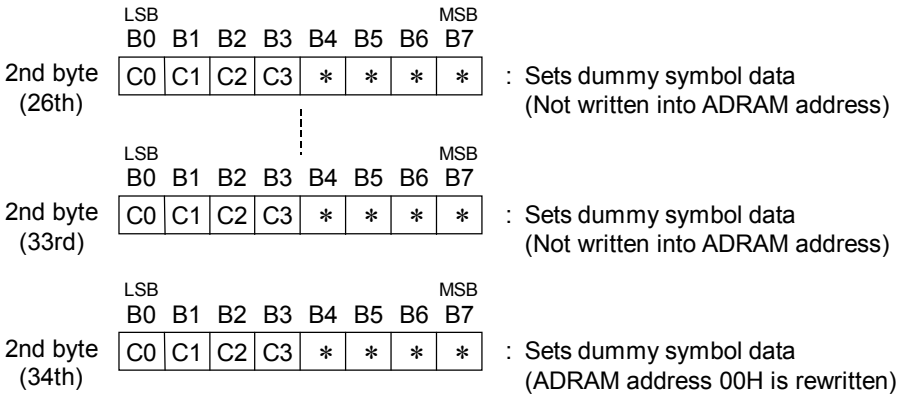
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	X4	1	1	0	: Selects ADRAM data write mode and specifies ADRAM address (Ex: Specifies ADRAM address 00H.)
2nd byte (2nd)	C0	C1	C2	C3	*	*	*	*	: Sets symbol data (written into ADRAM address 00H.)

To specify symbol data continuously to the next address, specify only symbol data as follows.
The address of ADRAM is automatically incremented. Specification of addresses is therefore unnecessary.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (3rd)	C0	C1	C2	C3	*	*	*	*	: Sets symbol data (written into ADRAM address 01H)
2nd byte (4th)	C0	C1	C2	C3	*	*	*	*	: Sets symbol data (written into ADRAM address 02H)
	⋮								
2nd byte (25th)	C0	C1	C2	C3	*	*	*	*	: Sets symbol data (written into ADRAM address 17H)

The symbol data setting up to 24 digits is completed.
To set symbol data from ADRAM address 00H continuously.
Specify a dummy symbol data between ADRAM addresses 18H and 1FH.
(To increment the ADRAM address automatically and set it to 00H)



X0 (LSB) to X4 (MSB) : ADRAM addresses (5 bits: 24 characters)
C0 (LSB) to C3 (MSB) : Symbol data (4 bits: 4-symbol data per digit)
* : Don't care

[COM positions and ADRAM addresses]

HEX	X0	X1	X2	X3	X4	COM position	HEX	X0	X1	X2	X3	X4	COM position
00	0	0	0	0	0	COM1	10	0	0	0	0	1	COM17
01	1	0	0	0	0	COM2	11	1	0	0	0	1	COM18
02	0	1	0	0	0	COM3	12	0	1	0	0	1	COM19
03	1	1	0	0	0	COM4	13	1	1	0	0	1	COM20
04	0	0	1	0	0	COM5	14	0	0	1	0	1	COM21
05	1	0	1	0	0	COM6	15	1	0	1	0	1	COM22
06	0	1	1	0	0	COM7	16	0	1	1	0	1	COM23
07	1	1	1	0	0	COM8	17	1	1	1	0	1	COM24
08	0	0	0	1	0	COM9	18	0	0	0	1	1	Not fixed
09	1	0	0	1	0	COM10	19	1	0	0	1	1	Not fixed
0A	0	1	0	1	0	COM11	1A	0	1	0	1	1	Not fixed
0B	1	1	0	1	0	COM12	1B	1	1	0	1	1	Not fixed
0C	0	0	1	1	0	COM13	1C	0	0	1	1	1	Not fixed
0D	1	0	1	1	0	COM14	1D	1	0	1	1	1	Not fixed
0E	0	1	1	1	0	COM15	1E	0	1	1	1	1	Not fixed
0F	1	1	1	1	0	COM16	1F	1	1	1	1	1	Not fixed

4. General output port set
   (Specifies the general output port status.)

   The general output port is an output for 4-bit static operation.
   When the $\overline{\text{RESET}}$ signal is input, the general output ports go “Low”. (See “Reset Function”)
   It is used to control other I/O devices and turn on LED. (static operation)
   When at the "High" level, this output becomes the V_{DD} voltage, and when at the "Low" level, it becomes the ground potential. Therefore, the fluorescent display tube cannot be driven.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	P1	P2	P3	P4	*	0	0	1	: Selects a general output port and specifies the output status

P1 to P4 : General output ports
* : Don't care

[Set data and set state of general output port]

Pn	Display state of general output port	
0	Sets the output to Low	(The state when $\overline{\text{RESET}}$ signal is input.)
1	Sets the output to High	

5. Display duty set
(Writes a display duty value to the duty cycle register.)

Display duty adjusts brightness in 960 stages (0/1024 to 960/1024) using 10-bit data.
When the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". (See "Reset Function") Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	D0	D1	*	*	*	1	0	1	: Selects display duty set and sets duty value (low-order 2 bits).
2nd byte (2nd)	D2	D3	D4	D5	D6	D7	D8	D9	: Sets duty value (high-order 8 bits).

D0 (LSB) to D9 (MSB) : Display duty data (10 bits: 0/1024 to 960/1024 stages)
* : Don't care

[Relation between setup data and controlled COM duty]

HEX	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	COM duty	
000	0	0	0	0	0	0	0	0	0	0	0/1024	← (The state when $\overline{\text{RESET}}$ signal is input.)
001	1	0	0	0	0	0	0	0	0	0	1/1024	
002	0	1	0	0	0	0	0	0	0	0	2/1024	
⋮											⋮	
3BE	0	1	1	1	1	1	0	1	1	1	958/1024	
3BF	1	1	1	1	1	1	0	1	1	1	959/1024	
3C0	0	0	0	0	0	0	1	1	1	1	960/1024	
3C1	1	0	0	0	0	0	1	1	1	1	960/1024	
⋮											⋮	
3FE	0	1	1	1	1	1	1	1	1	1	960/1024	
3FF	1	1	1	1	1	1	1	1	1	1	960/1024	

6. Number of digits set
(Writes the number of display digits to the display digit register.)

The number of digits set can display 9 to 24 digits using 4-bit data.
When the $\overline{\text{RESET}}$ signal is input, the number of digit register value is "0". (See "Reset Function") Always execute this instruction to change the number of digits before turning the display on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	*	0	1	1	: Selects the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB) : Number of digit data (4 bits: 16 digits)
* : Don't care

[Relation between setup data and controlled COM]

HEX	K0	K1	K2	K3	Number of digits of COM	HEX	K0	K1	K2	K3	Number of digits of COM
0	0	0	0	0	COM1 to 24	8	0	0	0	1	COM1 to 16
1	1	0	0	0	COM1 to 9	9	1	0	0	1	COM1 to 17
2	0	1	0	0	COM1 to 10	A	0	1	0	1	COM1 to 18
3	1	1	0	0	COM1 to 11	B	1	1	0	1	COM1 to 19
4	0	0	1	0	COM1 to 12	C	0	0	1	1	COM1 to 20
5	1	0	1	0	COM1 to 13	D	1	0	1	1	COM1 to 21
6	0	1	1	0	COM1 to 14	E	0	1	1	1	COM1 to 22
7	1	1	1	0	COM1 to 15	F	1	1	1	1	COM1 to 23

* The state when $\overline{\text{RESET}}$ signal is input.

7. All display lights ON/OFF set
   (Turns all display lights ON or OFF.)
   When the $\overline{\text{RESET}}$ signal is input, all segment, common and AD outputs go "Low". (See "Reset Function")
   All display lights ON is used primarily for display testing.
   All display lights OFF is primarily used for display blink and to prevent malfunction when power is turned on.
   This command cannot control the general output port.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	*	1	1	1	: Selects all display lights ON or OFF mode and specifies display operation

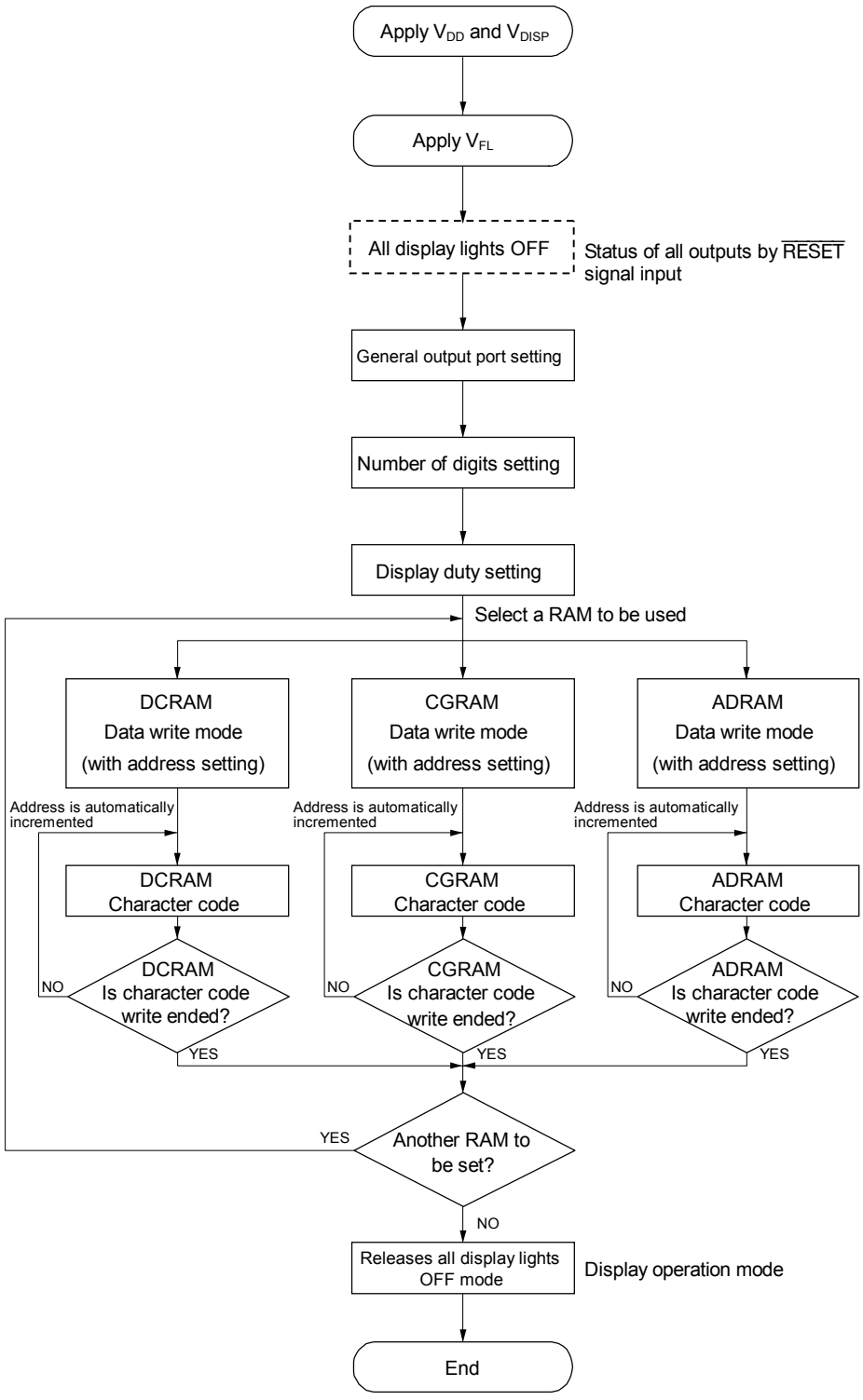
L and H: Display operation data
*: Don't care

[Set data and display state of SEG and AD]

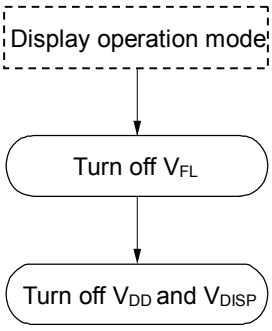
L	H	Display state of SEG and AD
0	0	Normal display
1	0	Sets all outputs to Low
0	1	Sets all outputs to High
1	1	Sets all outputs to High

(The state when $\overline{\text{RESET}}$ signal is input.)

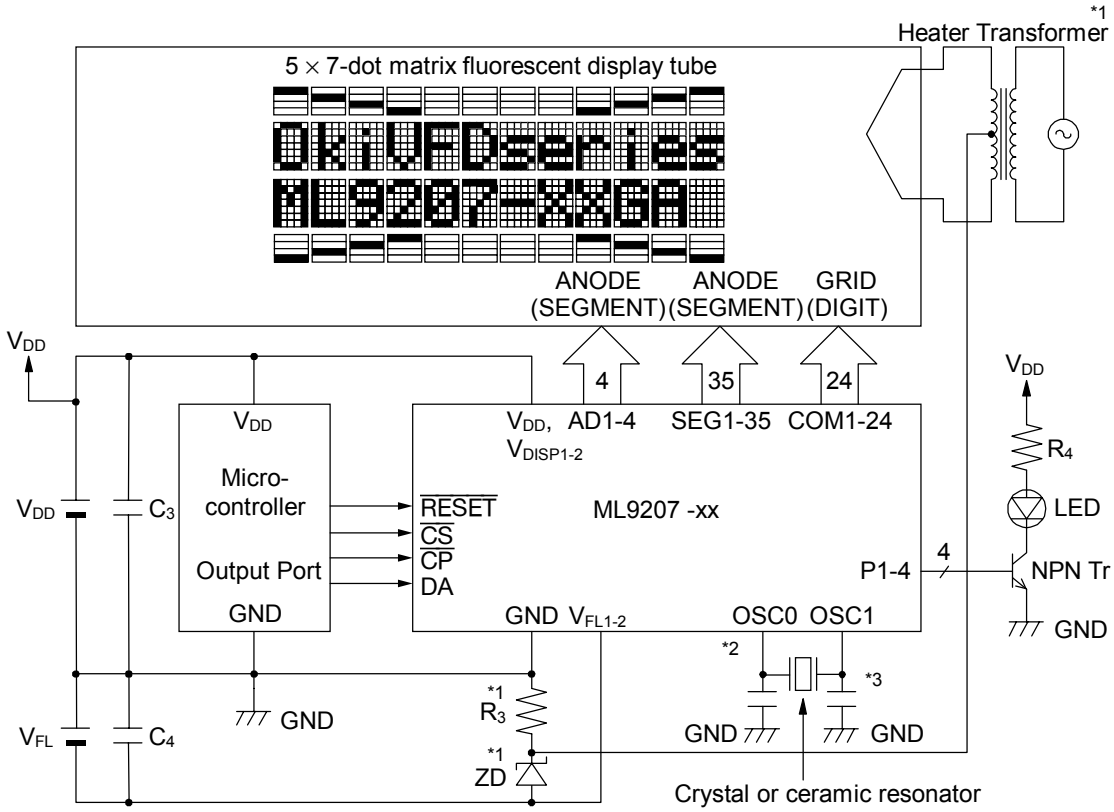
Setting Flowchart
(Power applying included)



Power-off Flowchart



APPLICATION CIRCUIT



Notes: *1. The application circuit indicates a circuit by which fluorescent display tube filaments are ac driven using a heater transformer. Contact fluorescent display tube manufacturers for the methods and circuits of driving fluorescent display tube filaments.

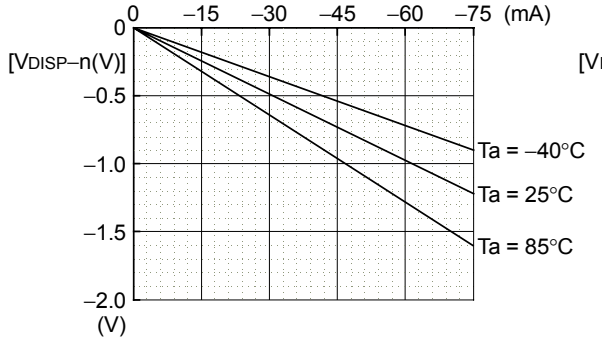
*2. Keep the wires between the OSC0 pin and the crystal or ceramic resonator as short as possible to avoid generating noise.

*3 For oscillation capacitor values, refer to data of the crystal or ceramic resonator used.

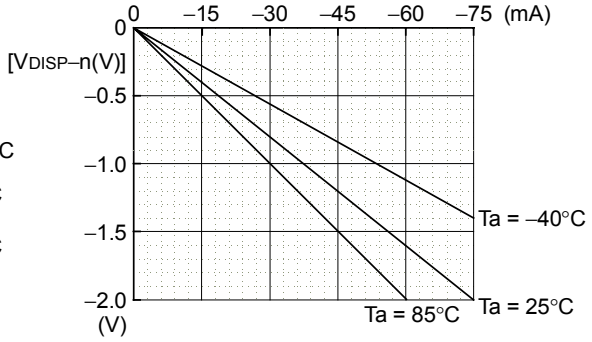
REFERENCE DATA

Graphs illustrating the V_{FL} versus driver output current capability relationship are shown below.
Care must be taken not to use the total power in excess of allowable power dissipation.

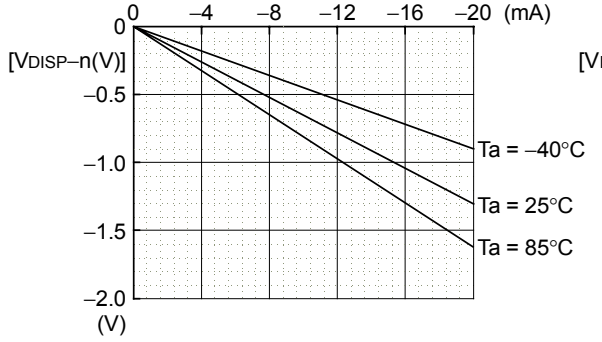
[Driver output current versus output drop voltage]
V_{FL} = –60V, COMn
[Output current (mA)]



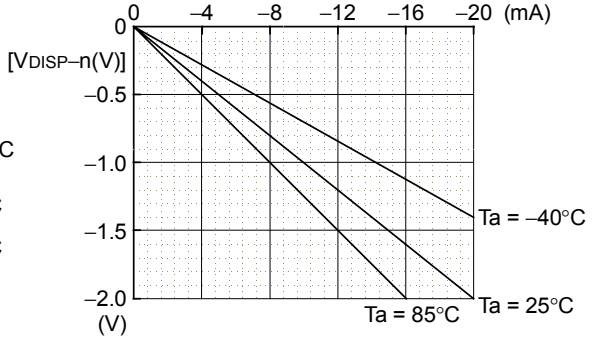
[Driver output current versus output drop voltage]
V_{FL} = –20V, COMn
[Output current (mA)]



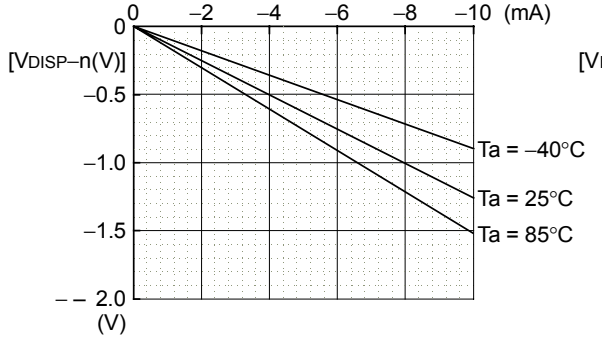
[Driver output current versus output drop voltage]
V_{FL} = –60V, ADn
[Output current (mA)]



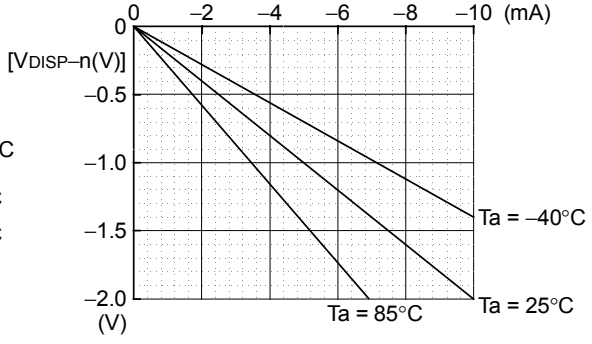
[Driver output current versus output drop voltage]
V_{FL} = –20V, ADn
[Output current (mA)]



[Driver output current versus output drop voltage]
V_{FL} = –60V, SEGn
[Output current (mA)]

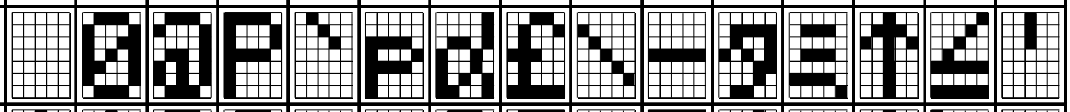
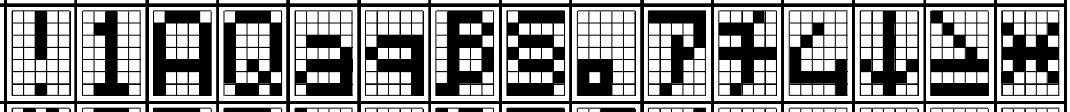
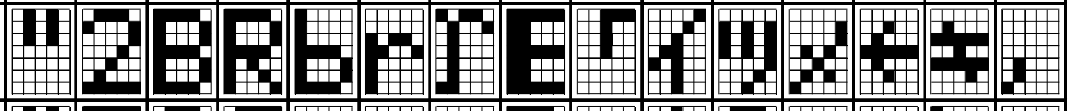
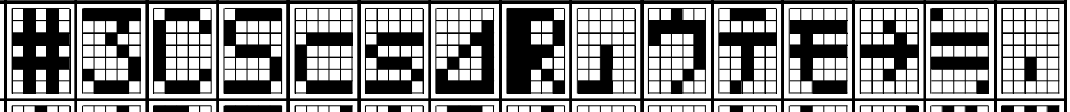
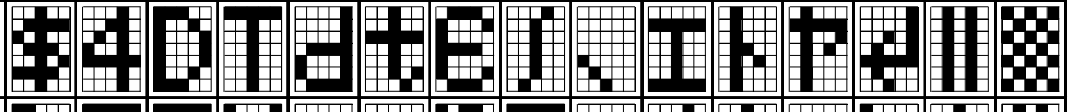
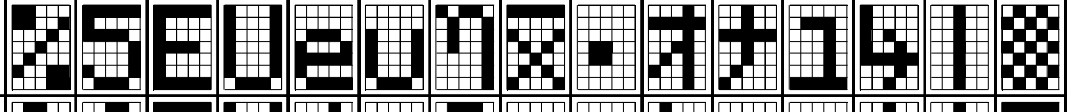
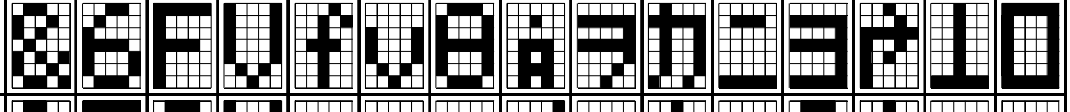
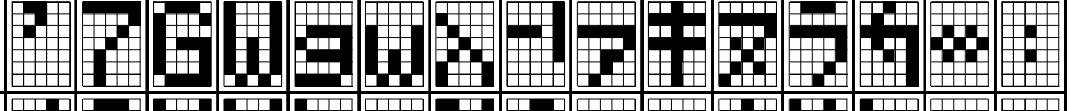
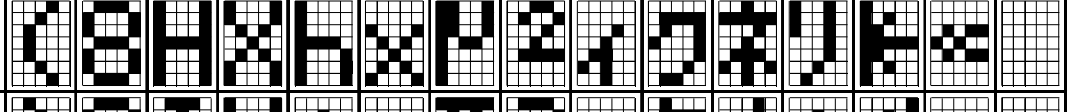
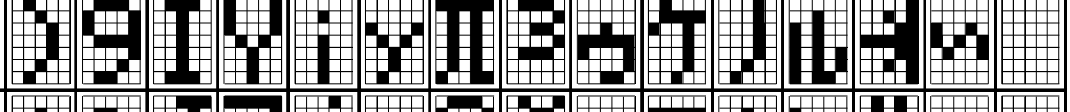
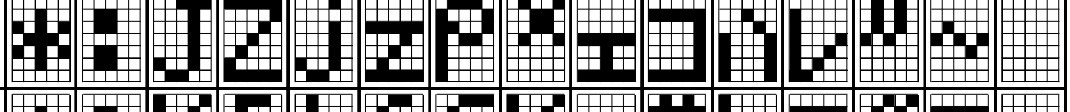
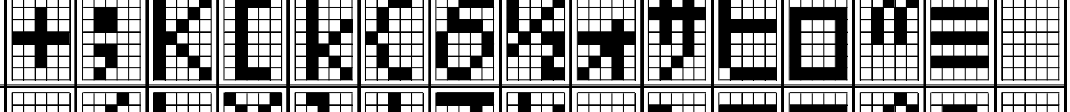
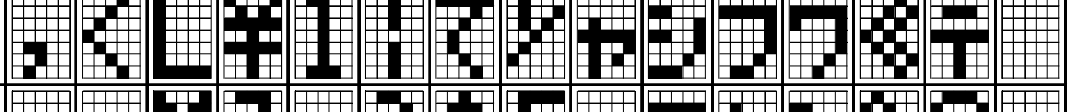
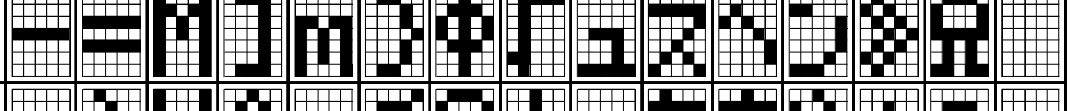
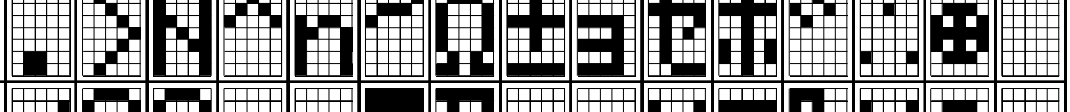
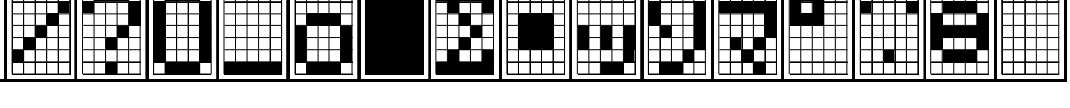


[Driver output current versus output drop voltage]
V_{FL} = –20V, SEGn
[Output current (mA)]



ML9207-01 ROM CODE

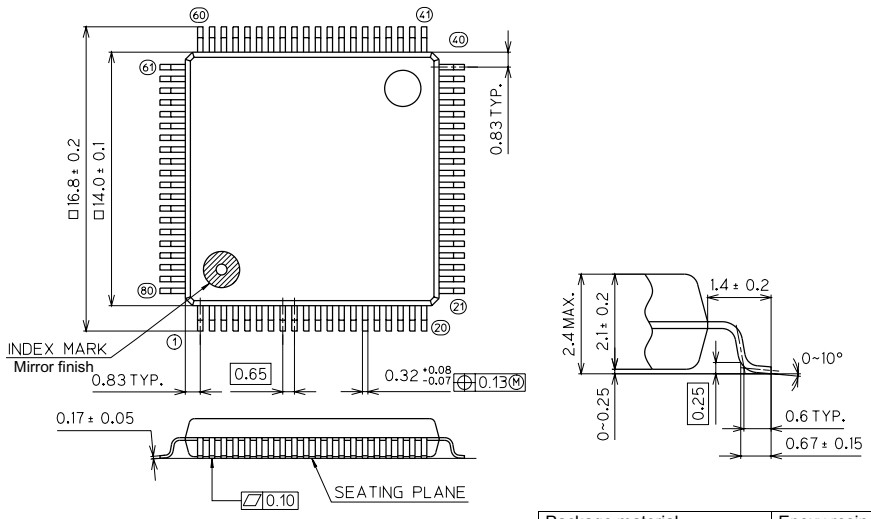
00000000B (00H) to 00000111B (0FH) are the CGRAM addresses.

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000	RAM8															
1001	RAM9															
1010	RAMA															
1011	RAMB															
1100	RAMC															
1101	RAMD															
1110	RAME															
1111	RAMF															

PACKAGE DIMENSIONS

(Unit: mm)

QFP80-P-1414-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.85 TYP.
Rev. No./Last Revised	3/Nov. 28, 1996

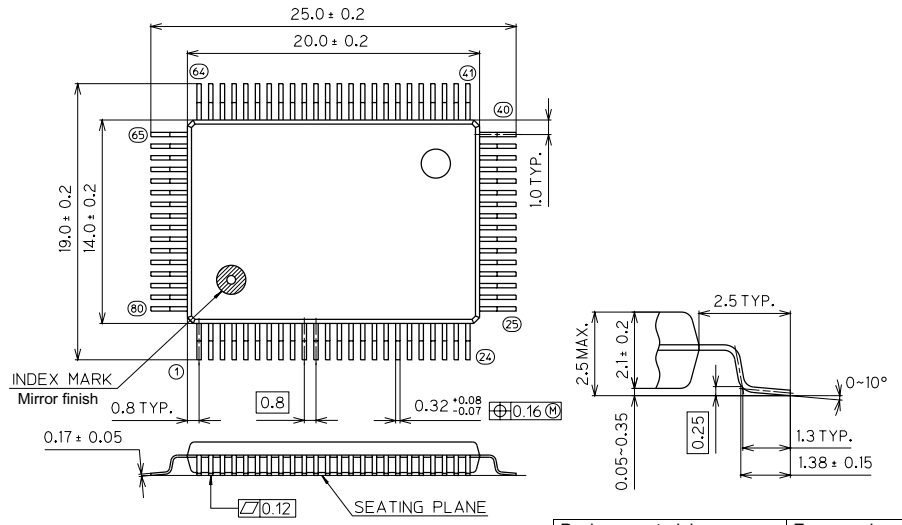
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

QFP80-P-1420-0.80-BK



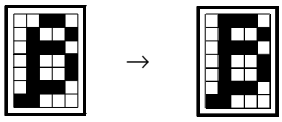
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.27 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9207-01	July 2000	–	–	Final edition 1
FEDL9207-02	May 17, 2005	1	1	TITLE 15×7DotCharacter×16-DigitDisplay Controller/Driver with Character RAM ↓ 15×7DotCharacter×24-DigitDisplay Controller/Driver with Character RAM
		31	31	ROM CODE LSB 0001 MSB 0111 
		-	34	Added Revision History

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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