

MC14174B

Hex Type D Flip-Flop

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

Features

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Functional Equivalent to TTL 74174
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Parameter | Symbol | Value | Unit |
|---|-------------------|---------------------------|-------------|
| DC Supply Voltage Range | V_{DD} | -0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | V_{in}, V_{out} | -0.5 to V_{DD} + 0.5 | V |
| Input or Output Current (DC or Transient) per Pin | I_{in}, I_{out} | ± 10 | mA |
| Power Dissipation, per Package (Note 1) | P_D | 500 | mW |
| Ambient Temperature Range | T_A | -55 to +125 | $^{\circ}C$ |
| Storage Temperature Range | | -65 to +150 | $^{\circ}C$ |
| Lead Temperature (8-Second Soldering) | | 260 | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic "P and D/DW"
Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

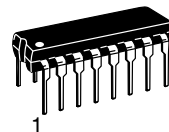
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



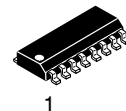
ON Semiconductor®

<http://onsemi.com>

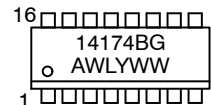
MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------|------------------|
| MC14174BCPG | PDIP-16 (Pb-Free) | 500 Units/Rail |
| MC14174BDG | SOIC-16 (Pb-Free) | 48 Units/Rail |
| MC14174BDR2G | SOIC-16 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14174B

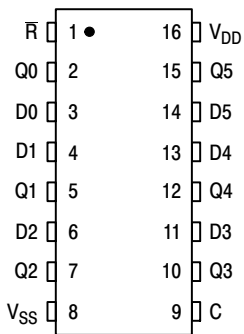
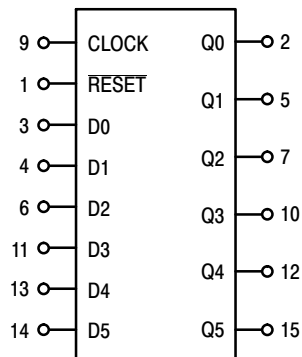


Figure 1. Pin Assignment



V_{DD} = PIN 16
V_{SS} = PIN 8

Figure 2. Block Diagram

TRUTH TABLE (Positive Logic)

| Inputs | | | Output |
|--------|------|-------|--------|
| Clock | Data | Reset | Q |
| ⌊ | 0 | 1 | 0 |
| ⌊ | 1 | 1 | 1 |
| ⌋ | X | 1 | Q |
| X | X | 0 | 0 |

No Change

X = Don't Care

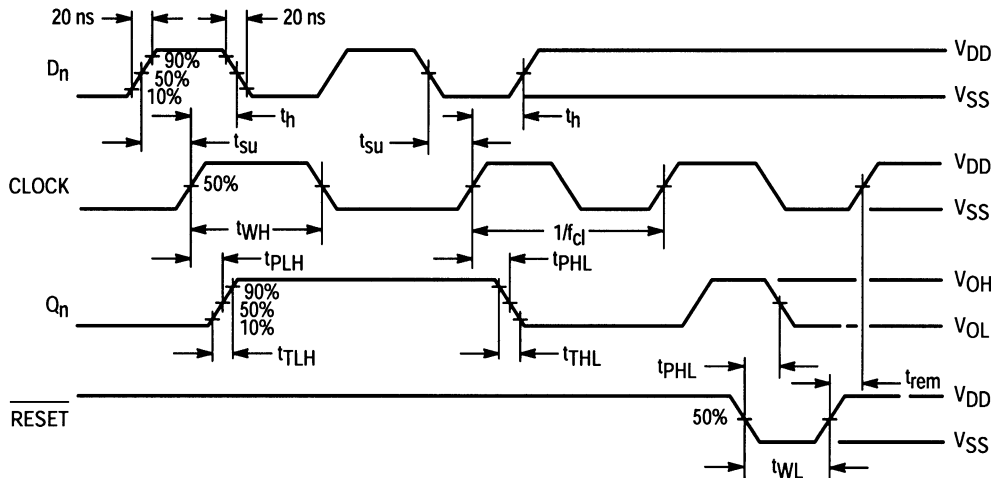


Figure 3. Timing Diagram

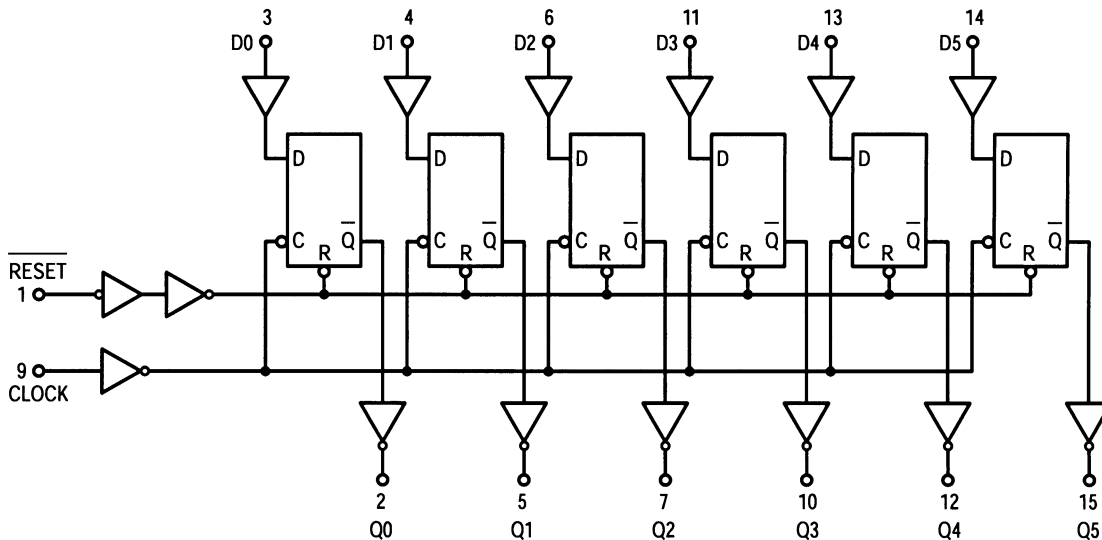


Figure 4. Functional Block Diagram

MC14174B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|---|---------------------------|-----------------|--|-----------|-------|-----------------|-----------|-------|-----------|-----------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | |
| Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD} | "0" Level V_{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | "1" Level V_{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | Vdc |
| | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | |
| | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | |
| Input Voltage $(V_O = 4.5$ or 0.5 Vdc) $(V_O = 9.0$ or 1.0 Vdc) $(V_O = 13.5$ or 1.5 Vdc) $(V_O = 0.5$ or 4.5 Vdc) $(V_O = 1.0$ or 9.0 Vdc) $(V_O = 1.5$ or 13.5 Vdc) | "0" Level V_{IL} | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | Vdc |
| | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | |
| | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | |
| | "1" Level V_{IH} | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | - | Vdc |
| | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | - | |
| | | 15 | 11 | - | 11 | 8.25 | - | 11 | - | |
| Output Drive Current $(V_{OH} = 2.5$ Vdc) $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc) $(V_{OL} = 0.4$ Vdc) $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc) | Source I_{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | |
| | Sink I_{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | mAdc |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | |
| 15 | | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | | |
| Input Current | I_{in} | 15 | - | ± 0.1 | - | ± 0.00001 | ± 0.1 | - | ± 1.0 | μ Adc |
| Input Capacitance, ($V_{in} = 0$) | C_{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | μ Adc |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | |
| Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching) | I_T | 5.0 | $I_T = (1.1 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (2.3 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.7 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | μ Adc |
| | | 10 | | | | | | | | |
| | | 15 | | | | | | | | |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$ where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.003$.

MC14174B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | All Types | | | Unit |
|--|--------------------|-----------------|------------------|-------------------|-------------------|---------------|
| | | | Min | Typ (Note 6) | Max | |
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{TLH}, t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time — Clock to Q $t_{PLH}, t_{PHL} = (0.9 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 64 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 52 \text{ ns}$ | t_{PLH}, t_{PHL} | 5.0 10 15 | – – – | 210 85 65 | 400 160 120 | ns |
| Propagation Delay Time — Reset to Q $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 79 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$ | t_{PHL} | 5.0 10 15 | – – – | 250 100 75 | 500 200 150 | ns |
| Clock Pulse Width | t_{WH} | 5.0 10 15 | 150 90 70 | 75 45 35 | – – – | ns |
| Reset Pulse Width | t_{WL} | 5.0 10 15 | 200 100 80 | 100 50 40 | – – – | ns |
| Clock Pulse Frequency | f_{cl} | 5.0 10 15 | – – – | 7.0 12 15.5 | 2.0 5.0 6.5 | mHz |
| Clock Pulse Rise and Fall Time | t_{TLH}, t_{THL} | 5.0 10 15 | – – – | – – – | 15 5.0 4.0 | μs |
| Data Setup Time | t_{su} | 5.0 10 15 | 40 20 15 | 20 10 0 | – – – | ns |
| Data Hold Time | t_h | 5.0 10 15 | 80 40 30 | 40 20 15 | – – – | ns |
| Reset Removal Time | t_{rem} | 5.0 10 15 | 250 100 80 | 125 50 40 | – – – | ns |

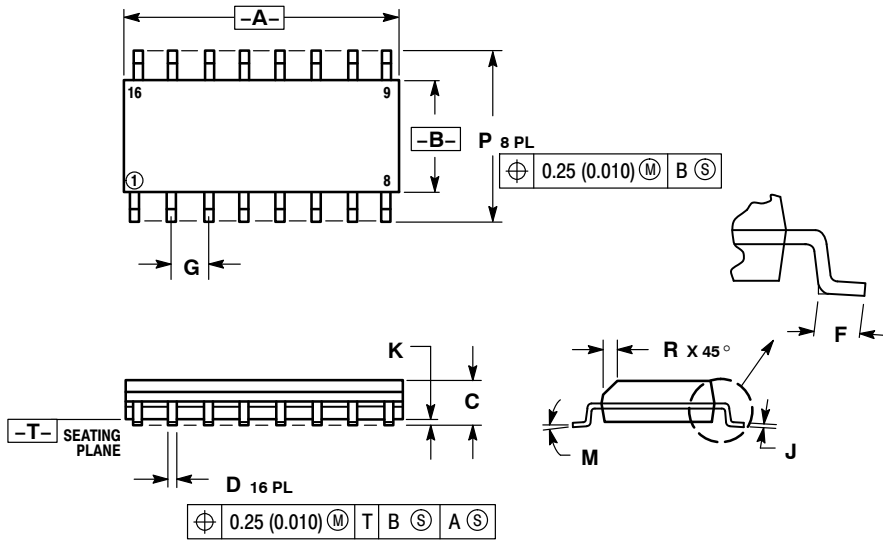
5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14174B

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

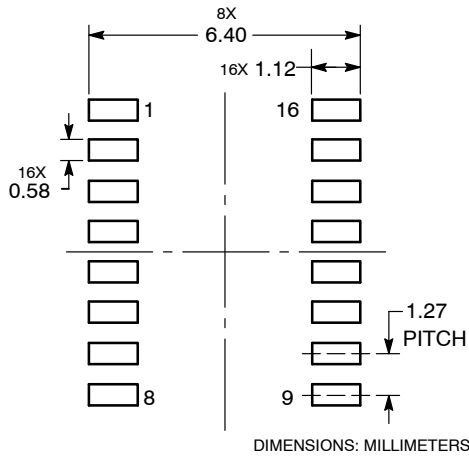


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

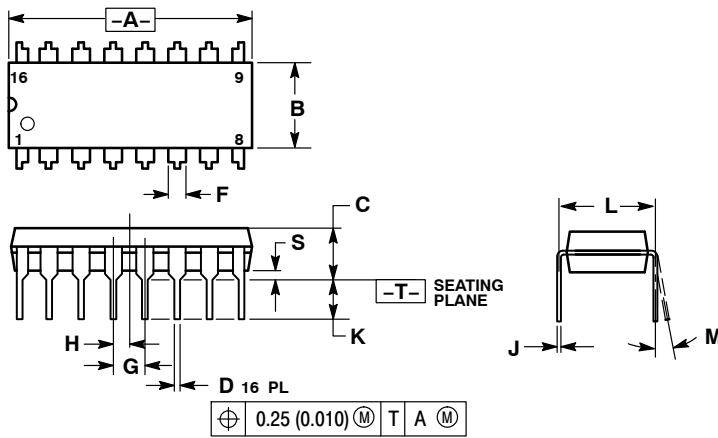
SOLDERING FOOTPRINT



MC14174B

PACKAGE DIMENSIONS

PDIP-16
CASE 648-08
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative