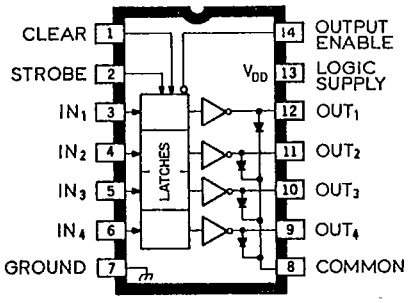
5800 AND 5801

MIL-STD-883 COMPLIANT

T-52-17

BiMOS II LATCHED DRIVERS

UCS5800H



Dwg. No. A-10,499D

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . **50 V**
Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Collector Current,
I_C . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Ambient Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Note: Output current rating may be limited by duty cycle, ambient temperature, air flow, and number of outputs conducting. Under any set of conditions, do not exceed a maximum junction temperature of +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Simplifying interface between LSI and peripheral power loads, the hermetically sealed UCS5800H (4-bit) and UCS5801H (8-bit) latched drivers combine the advantages of CMOS logic and control and high-voltage, high-current bipolar output buffers. Typical applications include microprocessor interface to relays, solenoids, dc and stepper motors, printers, LED or incandescent displays requiring hermetic packaging and an operating temperature range of -55°C to +125°C.

BiMOS II latched drivers have data input rates faster than those of the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The Darlington open-collector outputs will drive power loads rated to 50 V and 350 mA (500 mA, maximum). Integral diodes for inductive load transient suppression are included. Because of limitations on package power dissipation, the simultaneous operation of all drivers at high current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load-current capability.

The 4-bit, UCS5800H is furnished in a standard 14-pin side-brazed hermetic package. The 8-bit, UCS5801H is supplied in a 22-pin side-brazed hermetic package with row spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs. Both packages conform to the dimensional requirements of MIL-M-38510. High-temperature reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

FEATURES

- 4.4 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Control and Latches
- High-Voltage, High-Current Outputs
- Transient-Protected Outputs
- Operating Temperature -55°C to +125°C
- High-Reliability Screening to MIL-STD-883, Class B

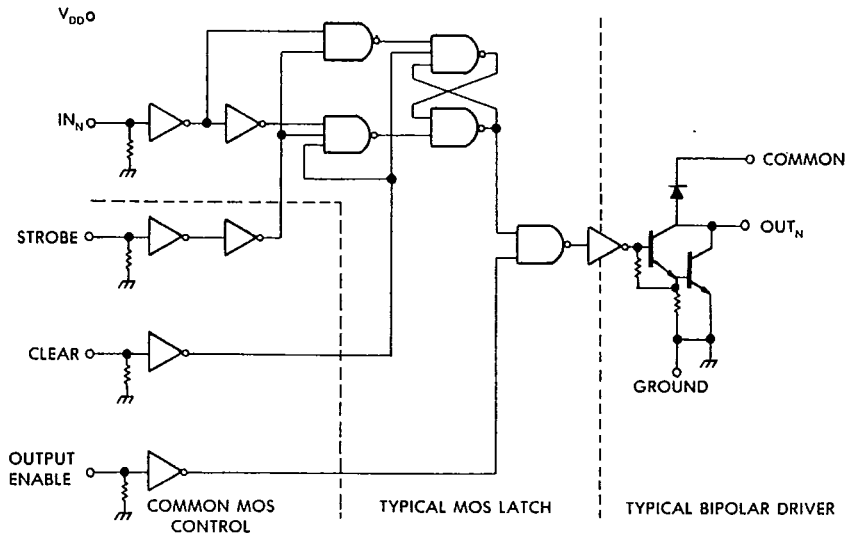
Always order by complete part number:

Part Number	Description
UCS5800H883	4-Bit Latched Driver
UCS5801H883	8-Bit Latched Driver

5800 AND 5801 BiMOS II LATCHED DRIVERS

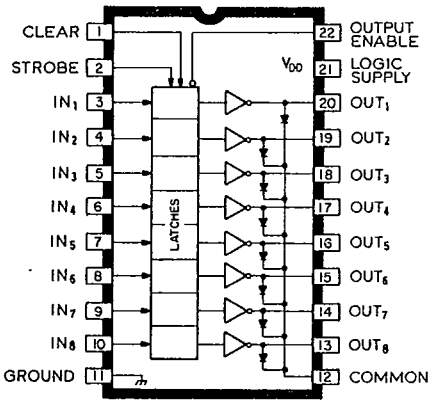
T-52-17

FUNCTIONAL BLOCK DIAGRAM



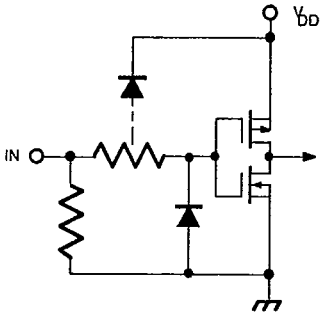
Dwg. No. A-10,495A

UCS5801H



Dwg. No. A-10,498D

TYPICAL INPUT CIRCUIT



Dwg. EP-010-4

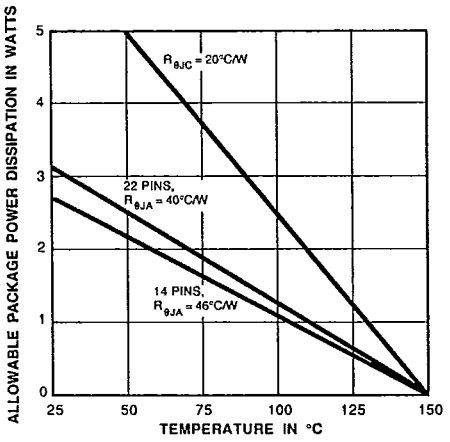
5800 AND 5801
BiMOS II LATCHED DRIVERS

T-52-17

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.1	V
		I_C = 200 mA	—	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Dwg. GM-008

5800 AND 5801 BiMOS II LATCHED DRIVERS

T-52-17

ELECTRICAL CHARACTERISTICS at T_A = -55°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.3	V
		I_C = 200 mA	—	1.5	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	11	—	V
		V_{DD} = 10 V	9.0	—	V
		V_{DD} = 5.0 V (See Note)	3.6	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	35	—	kΩ
		V_{DD} = 10 V	35	—	kΩ
		V_{DD} = 5.0 V	35	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.5	mA
		V_{DD} = 10 V, Outputs Open	—	2.1	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.1	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

5800 AND 5801
BiMOS II LATCHED DRIVERS

T-52-17

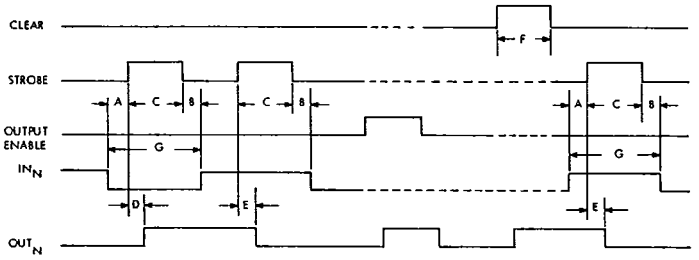
ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.3	V
		I_C = 200 mA	—	1.5	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

5800 AND 5801 BiMOS II LATCHED DRIVERS

T-52-17



Dwg. No. A-10,895A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**
C. Minimum Strobe Pulse Width . . . . . **125 ns**
D. Typical Time Between Strobe Activation and Output On to Off Transition . . . . . **500 ns**
E. Typical Time Between Strobe Activation and Output Off to On Transition . . . . . **500 ns**
F. Minimum Clear Pulse Width . . . . . **300 ns**
G. Minimum Data Pulse Width. . . . . **225 ns**

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_{IN} t-1	OUT_{IN} t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

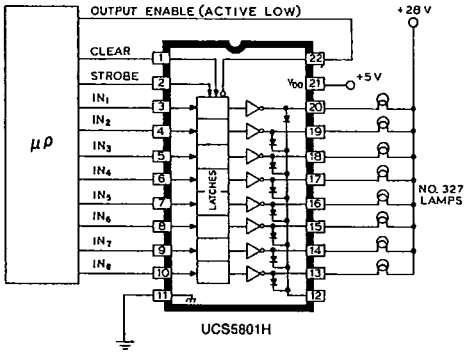
X = Irrelevant
t-1 = Previous Output State
t = Present Output State

5800 AND 5801
BiMOS II LATCHED DRIVERS

T-52-17

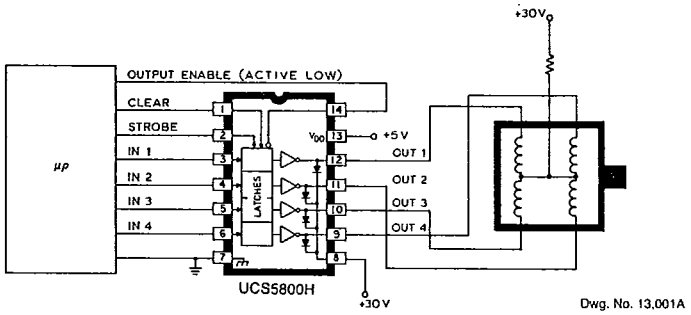
TYPICAL APPLICATIONS

INCANDESCENT LAMP DRIVER



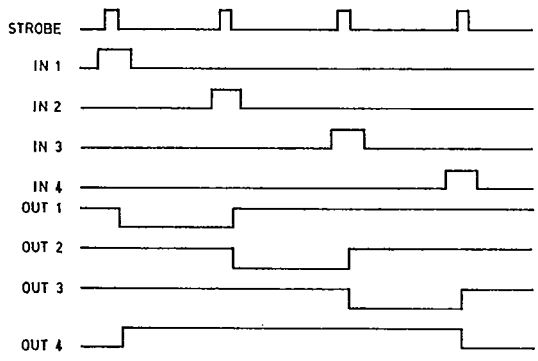
Dwg. No. 13,000A

UNIPOLAR STEPPER-MOTOR DRIVE



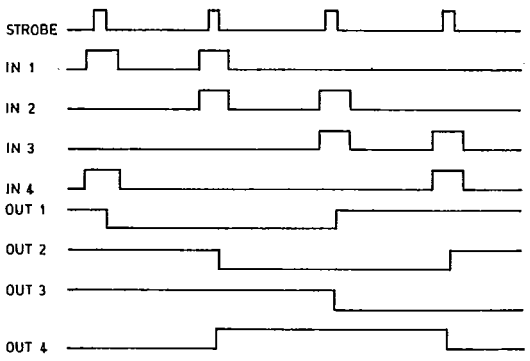
Dwg. No. 13,001A

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447