

# NSTB1005DXV5T1, NSTB1005DXV5T5

Preferred Devices

## Dual Common Base-Collector Bias Resistor Transistors

### NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. The NSTB1005DXV5T1 contains two complementary BRT devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free

[www.DataSheet4U.com](http://www.DataSheet4U.com)

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for Q<sub>1</sub> and Q<sub>2</sub>, - minus sign for Q<sub>1</sub> (PNP) omitted)

| Rating                    | Symbol    | Value | Unit |
|---------------------------|-----------|-------|------|
| Collector-Base Voltage    | $V_{CBO}$ | 50    | Vdc  |
| Collector-Emitter Voltage | $V_{CEO}$ | 50    | Vdc  |
| Collector Current         | $I_C$     | 100   | mAdc |

#### THERMAL CHARACTERISTICS

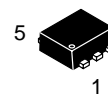
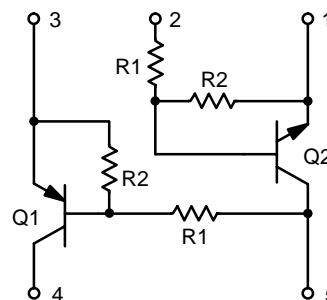
| Characteristic<br>(One Junction Heated)   | Symbol          | Max                          | Unit        |
|---|-----------------|------------------------------|-------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$           | 357 (Note 1)<br>2.9 (Note 1) | mW<br>mW/°C |
| Thermal Resistance –<br>Junction-to-Ambient   | $R_{\theta JA}$ | 350 (Note 1)                 | °C/W        |
| Characteristic<br>(Both Junctions Heated)   | Symbol          | Max                          | Unit        |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$           | 500 (Note 1)<br>4.0 (Note 1) | mW<br>mW/°C |
| Thermal Resistance –<br>Junction-to-Ambient   | $R_{\theta JA}$ | 250 (Note 1)                 | °C/W        |
| Junction and Storage Temperature  | $T_J, T_{stg}$  | -55 to +150                  | °C          |

1. FR-4 @ Minimum Pad



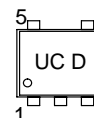
ON Semiconductor®

<http://onsemi.com>



SOT-553  
CASE 463B

#### MARKING DIAGRAM



UC = Specific Device Code  
D = Date Code

#### ORDERING INFORMATION

| Device         | Package | Shipping†                      |
|----------------|---------|--------------------------------|
| NSTB1005DXV5T1 | SOT-553 | 4 mm pitch<br>4000/Tape & Reel |
| NSTB1005DXV5T5 | SOT-553 | 2 mm pitch<br>8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**Preferred** devices are recommended choices for future use and best overall value.

# NSTB1005DXV5T1, NSTB1005DXV5T5

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

| Characteristic  | Symbol               | Min | Typ | Max | Unit |
|---|----------------------|-----|-----|-----|------|
| <b>Q1 TRANSISTOR: PNP – OFF CHARACTERISTICS</b>                                   |                      |     |     |     |      |
| Collector–Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)        | I <sub>CBO</sub>     | –   | –   | 100 | nAdc |
| Collector–Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)     | I <sub>CEO</sub>     | –   | –   | 500 | nAdc |
| Emitter–Base Cutoff Current   | I <sub>EBO</sub>     | –   | –   | 0.1 | mAdc |
| Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)     | V <sub>(BR)CBO</sub> | 50  | –   | –   | Vdc  |
| Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0) | V <sub>(BR)CEO</sub> | 50  | –   | –   | Vdc  |

### ON CHARACTERISTICS

|   |                                |      |     |      |     |
|---|--------------------------------|------|-----|------|-----|
| DC Current Gain   | h <sub>FE</sub>                | 80   | 140 | –    |     |
| Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>E</sub> = 0.3 mA)          | V <sub>CE(sat)</sub>           | –    | –   | 0.25 | Vdc |
| Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 3.5 V, R <sub>L</sub> = 1.0 kΩ)  | V <sub>OL</sub>                | –    | –   | 0.2  | Vdc |
| Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ) | V <sub>OH</sub>                | 4.9  | –   | –    | Vdc |
| Input Resistor  | R1                             | 32.9 | 47  | 61.1 | kΩ  |
| Resistor Ratio  | R <sub>1</sub> /R <sub>2</sub> | 0.8  | 1.0 | 1.2  |     |

### Q2 TRANSISTOR: NPN – OFF CHARACTERISTICS

|   |                  |   |   |     |      |
|---|------------------|---|---|-----|------|
| Collector–Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)    | I <sub>CBO</sub> | – | – | 100 | nAdc |
| Collector–Emitter Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>B</sub> = 0) | I <sub>CEO</sub> | – | – | 500 | nAdc |
| Emitter–Base Cutoff Current (V <sub>EB</sub> = 6.0, I <sub>C</sub> = 5.0 mA)  | I <sub>EBO</sub> | – | – | 0.1 | mAdc |

### ON CHARACTERISTICS

|   |                      |     |     |      |     |
|---|----------------------|-----|-----|------|-----|
| Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)                   | V <sub>(BR)CBO</sub> | 50  | –   | –    | Vdc |
| Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)               | V <sub>(BR)CEO</sub> | 50  | –   | –    | Vdc |
| DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)                               | h <sub>FE</sub>      | 80  | 140 | –    |     |
| Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0.3 mA)          | V <sub>CE(SAT)</sub> | –   | –   | 0.25 | Vdc |
| Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ)  | V <sub>OL</sub>      | –   | –   | 0.2  | Vdc |
| Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ) | V <sub>OH</sub>      | 4.9 | –   | –    | Vdc |
| Input Resistor  | R1                   | 33  | 47  | 61   | kΩ  |
| Resistor Ratio  | R1/R2                | 0.8 | 1.0 | 1.2  |     |

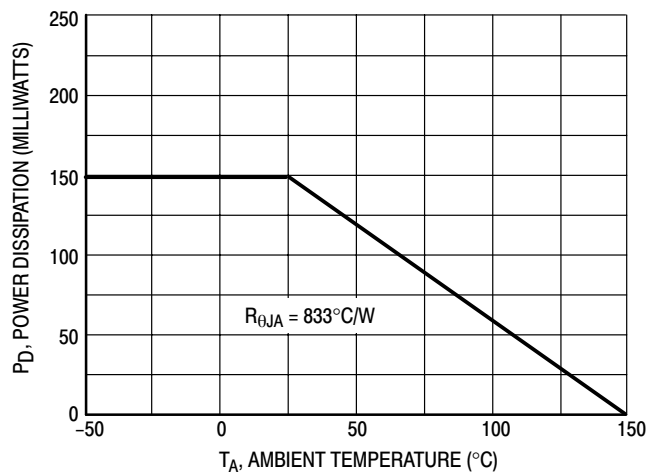


Figure 1. Derating Curve

# NSTB1005DXV5T1, NSTB1005DXV5T5

## TYPICAL ELECTRICAL CHARACTERISTICS – PNP TRANSISTOR

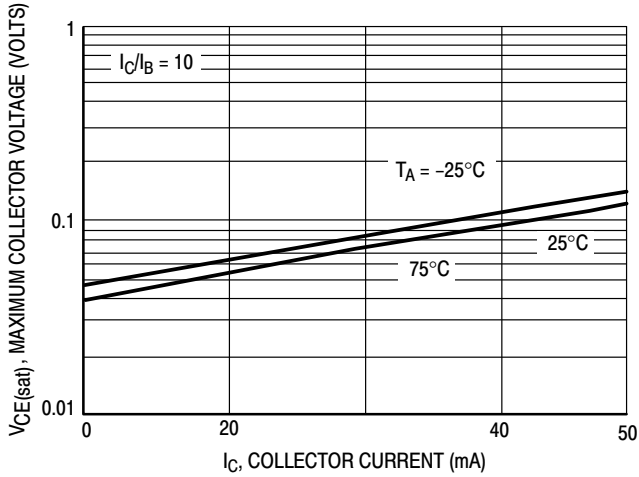


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

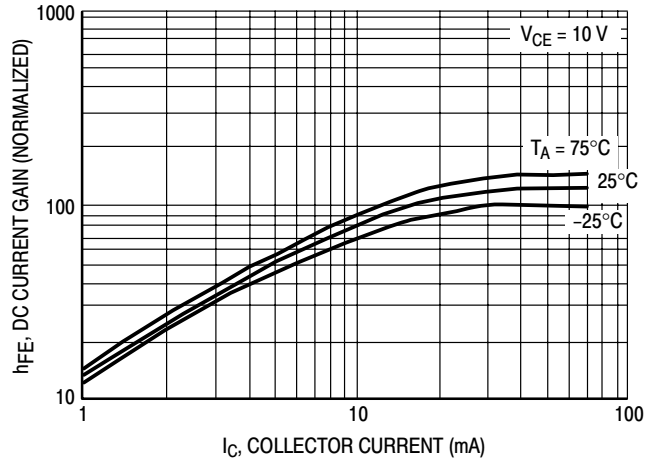


Figure 3. DC Current Gain

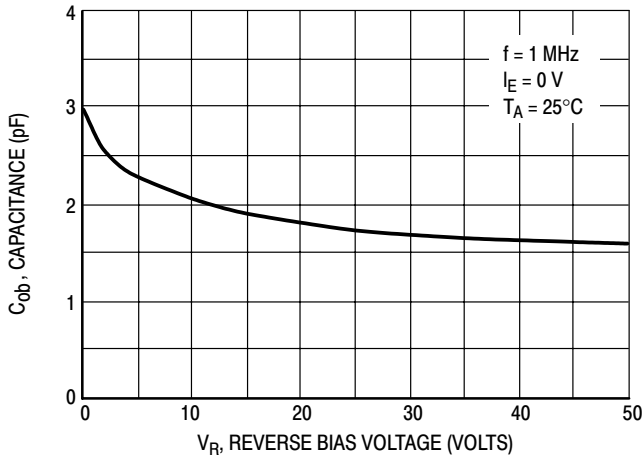


Figure 4. Output Capacitance

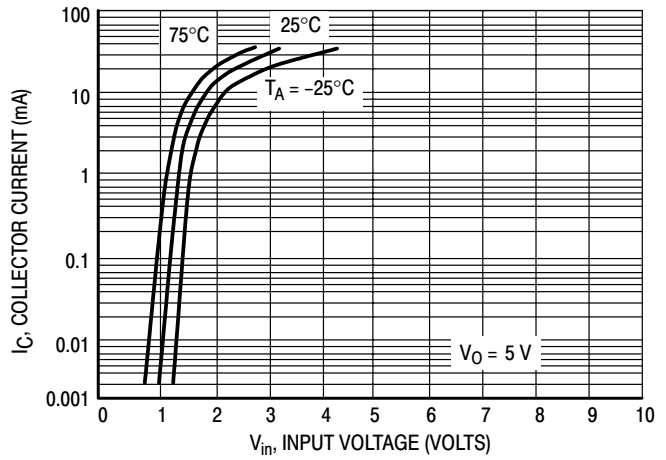


Figure 5. Output Current versus Input Voltage

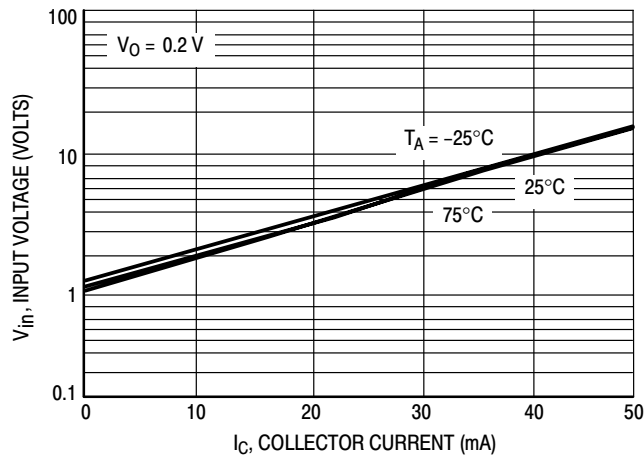


Figure 6. Input Voltage versus Output Current

# NSTB1005DXV5T1, NSTB1005DXV5T5

## TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

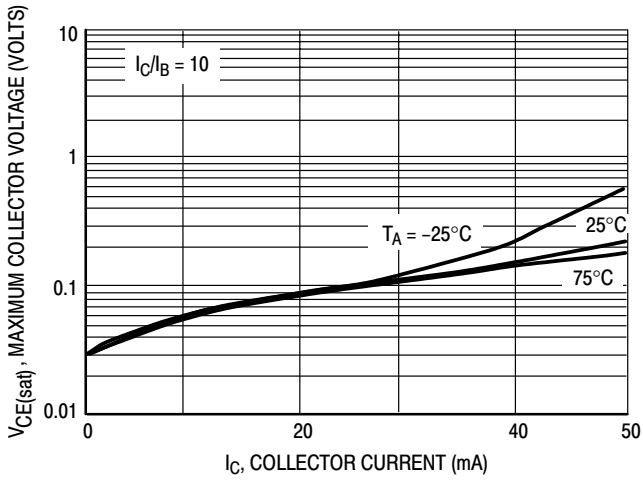


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

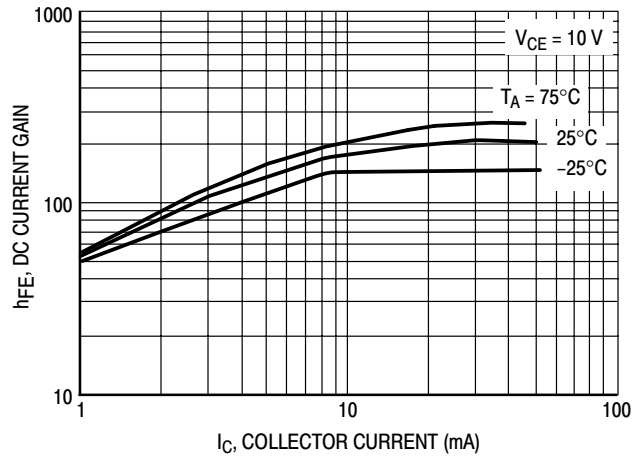


Figure 8. DC Current Gain

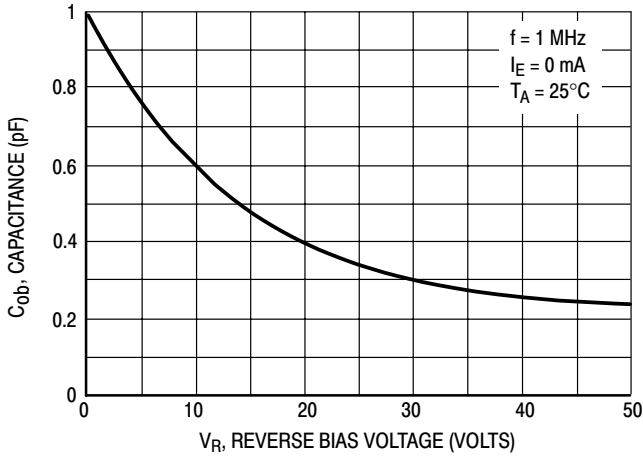


Figure 9. Output Capacitance

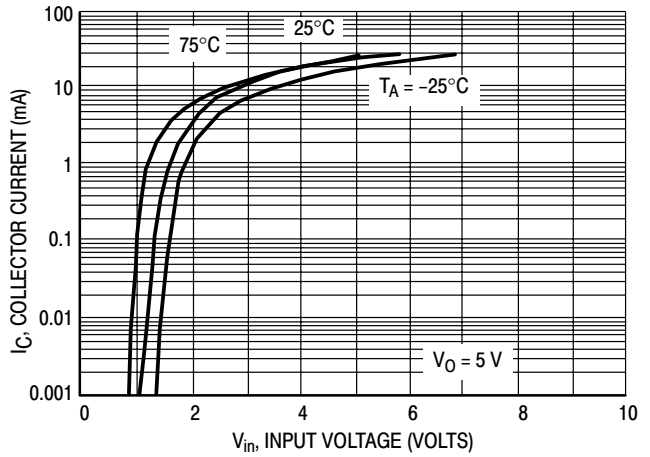


Figure 10. Output Current versus Input Voltage

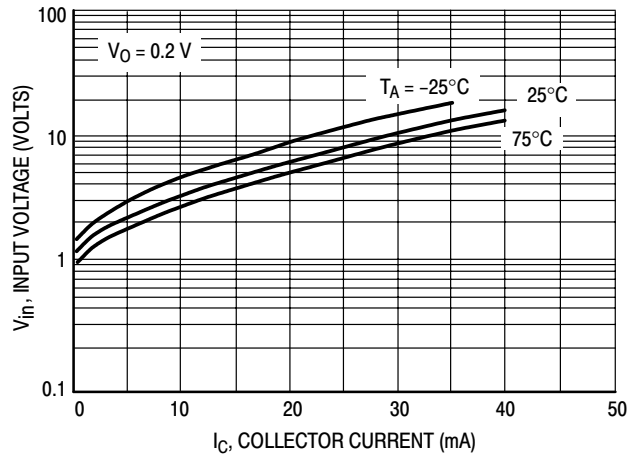
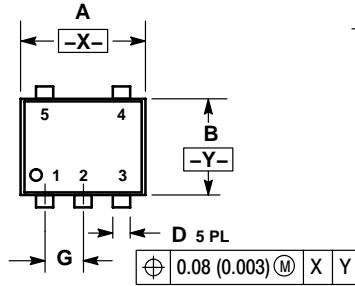


Figure 11. Input Voltage versus Output Current

# NSTB1005DXV5T1, NSTB1005DXV5T5

## PACKAGE DIMENSIONS

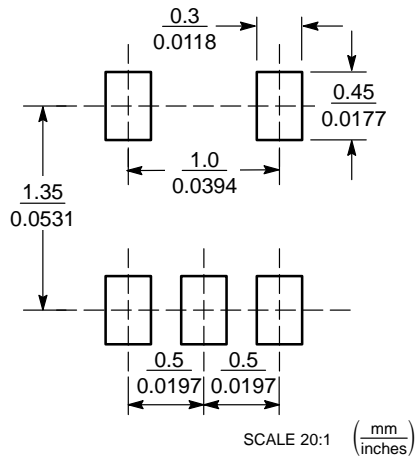
**SOT-553**  
**XV5 SUFFIX**  
 5-LEAD PACKAGE  
 CASE 463B-01  
 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.50        | 1.70 | 0.059     | 0.067 |
| B   | 1.10        | 1.30 | 0.043     | 0.051 |
| C   | 0.50        | 0.60 | 0.020     | 0.024 |
| D   | 0.17        | 0.27 | 0.007     | 0.011 |
| G   | 0.50 BSC    |      | 0.020 BSC |       |
| J   | 0.08        | 0.18 | 0.003     | 0.007 |
| K   | 0.10        | 0.30 | 0.004     | 0.012 |
| S   | 1.50        | 1.70 | 0.059     | 0.067 |

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NSTB1005DXV5T1, NSTB1005DXV5T5

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