

Features

- 13-Bit Resolution
- 20/40 MSPS Maximum Sampling Rate
- Ultra-Low Power Dissipation: 19/33 mW
- 72 dB SNR @ 8 MHz FIN
- Internal Reference Circuitry
- 1.8 V Core Supply Voltage
- 1.7 - 3.6 V I/O Supply Voltage
- Parallel CMOS Output
- 6 x 6 mm 40-Pin QFN (LP6HE) Package

Typical Applications

- Handheld Communication, PMR, SDR
- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- Baseband / IF Communication
- Video Digitizing
- CCD Digitizing

Functional Diagram

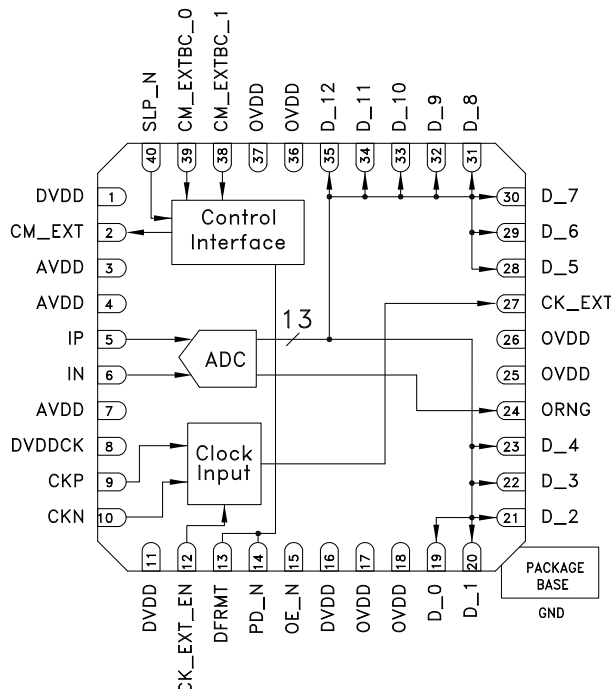


Figure 1. Functional Block Diagram

General Description

The HMCAD1051-40 is a high performance ultra low power analog-to-digital converter (ADC). The ADC employs internal reference circuitry, a CMOS control interface, CMOS output data and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Two idle modes with fast startup times exist. The entire chip can either be put in Standby Mode or Power Down mode. The two modes are optimized to allow the user to select the mode resulting in the lowest possible energy consumption during idle mode and startup.

The HMCAD1051-40 has a highly linear THA optimized for frequencies up to Nyquist. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave and CMOS clock inputs.

Pin compatible with HMCAD1041-40, HMCAD1041-80 and HMCAD1051-80.

Electrical Specifications

DC Electrical Specifications

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, 20/40 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 13 bit output, unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
DC accuracy					
No missing codes		Guaranteed			
Offset error	Midscale offset		1		LSB
Gain error	Full scale range deviation from typical			± 6	%FS
DNL	Differential nonlinearity (12-bit level)		± 0.2		LSB
INL	Integral nonlinearity (12-bit level)		± 0.6		LSB
V _{CM}	Common mode voltage output		V _{AVDD} /2		V
Analog Input					
Input common mode	Analog input common mode voltage	V _{CM} -0.1		V _{CM} +0.2	V
Full scale range, Normal	Differential input voltage range,		2		V _{pp}
Full scale range, Option	Differential input voltage range, 1V (see section Reference Voltages)		1		V _{pp}
Input capacitance	Differential input capacitance		2		pF
Bandwidth	Input Bandwidth	500			MHz
Power Supply					
Core Supply Voltage	Supply voltage to all 1.8V domain pins. See Pin Configuration and Description	1.7	1.8	2	V
I/O Supply Voltage	Output driver supply voltage (OVDD). Must be higher than or equal to Core Supply Voltage (V _{OVDD} ≥ V _{DVDD})	1.7	2.5	3.6	V

AC Electrical Specifications - 20 MSPS

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, FS=20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit	
Performance						
SNR	Signal to Noise Ratio					
	$F_{IN} = 2 \text{ MHz}$		72.5		dBFS	
	$F_{IN} = 8 \text{ MHz}$	71.5	72.2		dBFS	
	$F_{IN} = \sim \text{FS}/2$		72.1		dBFS	
SNDR	Signal to Noise and Distortion Ratio					
	$F_{IN} = 2 \text{ MHz}$		72.4		dBFS	
	$F_{IN} = 8 \text{ MHz}$	71	72		dBFS	
	$F_{IN} = \sim \text{FS}/2$		71.7		dBFS	
SFDR	Spurious Free Dynamic Range					
	$F_{IN} = 2 \text{ MHz}$		87		dBc	
	$F_{IN} = 8 \text{ MHz}$	75	85		dBc	
	$F_{IN} = \sim \text{FS}/2$		80		dBc	
HD2	Second order Harmonic Distortion					
	$F_{IN} = 2 \text{ MHz}$		-90		dBc	
	$F_{IN} = 8 \text{ MHz}$	-85	-95		dBc	
	$F_{IN} = \sim \text{FS}/2$		-95		dBc	
HD3	Third order Harmonic Distortion					
	$F_{IN} = 2 \text{ MHz}$		-87		dBc	
	$F_{IN} = 8 \text{ MHz}$	-75	-85		dBc	
	$F_{IN} = \sim \text{FS}/2$		-80		dBc	
ENOB	Effective number of Bits					
	$F_{IN} = 2 \text{ MHz}$		11.7		bits	
	$F_{IN} = 8 \text{ MHz}$	11.5	11.7		bits	
	$F_{IN} = \sim \text{FS}/2$		11.6		bits	
Power Supply						
	Analog supply current		7.8		mA	
	Digital supply current	Digital core supply				mA
	Output driver supply	2.5V output driver supply, sine wave input, $F_{IN} = 1 \text{ MHz}$, CK_EXT enabled		1.7		mA
	Output driver supply	2.5V output driver supply, sine wave input, $F_{IN} = 1 \text{ MHz}$, CK_EXT disabled		1.3		mA
	Analog power Dissipation			14		mW
	Digital power Dissipation	OVDD = 2.5V, 5pF load on output bits, $F_{IN} = 1 \text{ MHz}$, CK_EXT disabled		5.1		mW
	Total power Dissipation	OVDD = 2.5V, 5pF load on output bits, $F_{IN} = 1 \text{ MHz}$, CK_EXT disabled		19.1		mW
	Power Down Dissipation			9.9		μW
	Sleep Mode	Power Dissipation, Sleep mode				mW
Clock Inputs						
Max. Conversion Rate			20		MSPS	
Min. Conversion Rate				3	MSPS	



**SINGLE 13/12-BIT 20/40 MSPS
A/D CONVERTER**

AC Electrical Specifications - 40 MSPS

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, FS= 40 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit	
Performance						
SNR	Signal to Noise Ratio					
	$F_{IN} = 2$ MHz		72.5		dBFS	
	$F_{IN} = 8$ MHz	71.9	72.7		dBFS	
	$F_{IN} = \sim FS/2$		72		dBFS	
SNDR	Signal to Noise and Distortion Ratio					
	$F_{IN} = 2$ MHz		71.7		dBFS	
	$F_{IN} = 8$ MHz	71	72.1		dBFS	
	$F_{IN} = \sim FS/2$		71.5		dBFS	
SFDR	Spurious Free Dynamic Range					
	$F_{IN} = 2$ MHz		81		dBc	
	$F_{IN} = 8$ MHz	75	81		dBc	
	$F_{IN} = \sim FS/2$		80		dBc	
HD2	Second order Harmonic Distortion					
	$F_{IN} = 2$ MHz		-90		dBc	
	$F_{IN} = 8$ MHz	-85	-95		dBc	
	$F_{IN} = \sim FS/2$		-95		dBc	
HD3	Third order Harmonic Distortion					
	$F_{IN} = 2$ MHz		-81		dBc	
	$F_{IN} = 8$ MHz	-75	-81		dBc	
	$F_{IN} = \sim FS/2$		-80		dBc	
ENOB	Effective number of Bits					
	$F_{IN} = 2$ MHz		11.6		bits	
	$F_{IN} = 8$ MHz	11.5	11.7		bits	
	$F_{IN} = \sim FS/2$		11.6		bits	
Power Supply						
	Analog supply current		13.4		mA	
	Digital supply current	Digital core supply		1.7		mA
	Output driver supply	2.5V output driver supply, sine wave input, $F_{IN} = 1$ MHz, CK_EXT enabled		3.3		mA
	Output driver supply	2.5V output driver supply, sine wave input, $F_{IN} = 1$ MHz, CK_EXT disabled		2.4		mA
	Analog power Dissipation			24.1		mW
	Digital power Dissipation	OVDD = 2.5V, 5pF load on output bits, $F_{IN} = 1$ MHz, CK_EXT disabled		9.1		mW
	Total power Dissipation	OVDD = 2.5V, 5pF load on output bits, $F_{IN} = 1$ MHz, CK_EXT disabled		33.2		mW
	Power Down Dissipation			9.7		μ W
	Sleep Mode	Power Dissipation, Sleep mode		14.2		mW
Clock Inputs						
Max. Conversion Rate		40			MSPS	
Min. Conversion Rate				3	MSPS	

Digital and Timing Specifications

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, Conversion Rate: Max specified, 50% clock duty cycle, -1 dBFS input signal, 5 pF capacitive load on data outputs, unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
Clock Inputs					
Duty Cycle		20		80	% high
Compliance		CMOS, LVDS, LVPECL, Sine Wave			
Input range	Differential input swing	0.4			V _{pp}
Input range	Differential input swing, sine wave clock input	1.6			V _{pp}
Input common mode voltage	Keep voltages within ground and voltage of OVDD	0.3		V _{OVDD} -0.3	V
Input capacitance	Differential		2		pF
Timing					
T _{PD}	Start up time from Power Down Mode to Active Mode			900	clock cycles
T _{SLP}	Start up time from Sleep Mode to Active Mode			20	clock cycles
T _{OVR}	Out of range recovery time		1		clock cycles
T _{AP}	Aperture Delay		0.8		ns
ε _{rms}	Aperture jitter		< 0.5		ps
T _{LAT}	Pipeline Delay		12		clock cycles
T _D	Output delay (see timing diagram). 5pF load on output bits	3		10	ns
T _{DC}	Output delay relative to CK_EXT (see timing diagram)	1		6	ns
Logic Inputs					
V _{HI}	High Level Input Voltage. V _{OVDD} ≥ 3.0V	2			V
V _{HI}	High Level Input Voltage. V _{OVDD} = 1.7V – 3.0V	0.8 · V _{OVDD}			V
V _{LI}	Low Level Input Voltage. V _{OVDD} ≥ 3.0V	0		0.8	V
V _{LI}	Low Level Input Voltage. V _{OVDD} = 1.7V – 3.0V	0		0.2 · V _{OVDD}	V
I _{HI}	High Level Input leakage Current			±10	μA
I _{LI}	Low Level Input leakage Current			±10	μA
C _I	Input Capacitance		3		pF
Logic Outputs					
V _{HO}	High Level Output Voltage	V _{OVDD} -0.1			V
V _{LO}	Low Level Output Voltage			0.1	V
C _L	Max capacitive load. Post-driver supply voltage equal to pre-driver supply voltage V _{OVDD} = V _{OCVDD}			5	pF
C _L	Max capacitive load. Post-driver supply voltage above 2.25V ⁽¹⁾		10		pF

(1) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum

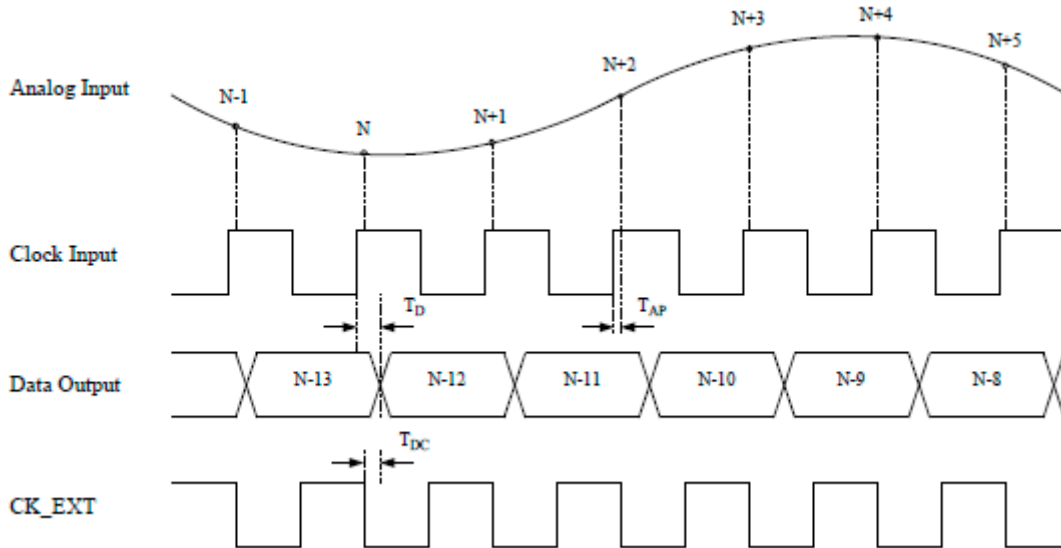
Timing Diagram


Figure 2: Timing Diagram

Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied for short periods of time. Exposure to absolute maximum rating conditions for an extended period of time may reduce device lifetime.

Table 1:

Pin	Pin	Rating
AVDD	VSS	-0.3V to +2.3V
DVDD	VSS	-0.3V to +2.3V
AVSS, DVSSCK, DVSS, OVSS	VSS	-0.3V to +0.3V
OVDD	VSS	-0.3V to +3.9V
IP, IN, analog inputs and outputs	VSS	-0.3V to +2.3V
Digital outputs	VSS	-0.3V to +3.9V
CKP, CKN	VSS	-0.3V to +3.9V
Digital Inputs	VSS	-0.3V to +3.9V
Operating temperature		-40 to +85 °C
Storage temperature		-60 to +150 °C
Soldering Profile Qualification		J-STD-020



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

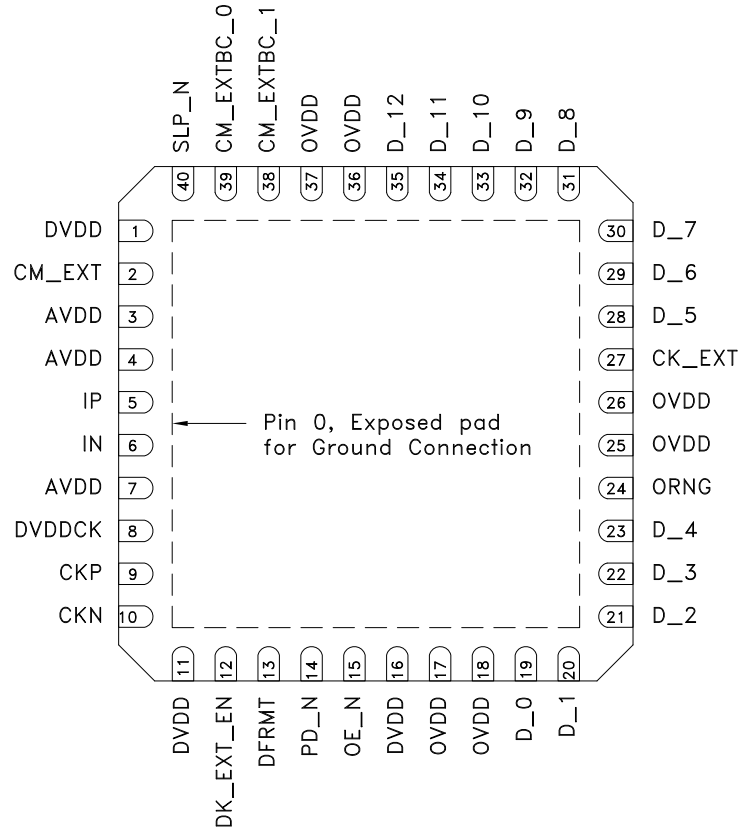
Pin Configuration and Description


Figure 3: Package Drawing, QFN 40-pin

Table 2: Pin Function

Pin #	Name	Description
0	VSS	Ground connection for all power domains. Exposed pad
1, 11, 16	DVDD	Digital and I/O-ring pre driver supply voltage, 1.8V
2	CM_EXT	Common Mode voltage output
3, 4, 7,	AVDD	Analog supply voltage, 1.8V
5, 6	IP, IN	Analog input (non-inverting, inverting)
8	DVDDCK	Clock circuitry supply voltage, 1.8V
9	CKP	Clock input, non-inverting (Format: LVDS, LVPECL, CMOS/TTL, Sine Wave)
10	CKN	Clock input, inverting. For CMOS input on CKP, connect CKN to ground.
12	CK_EXT_EN	CK_EXT signal enabled when low (zero). Tristate when high.
13	DFRMT	Data format selection. 0: Offset Binary, 1: Two's Complement
14	PD_N	Full chip Power Down mode when Low. All digital outputs reset to zero. After chip power up always apply Power Down mode before using Active Mode to reset chip.
15	OE_N	Output Enable. Tristate when high
17, 18, 25, 26, 36, 37	OVDD	I/O ring post-driver supply voltage. Voltage range 1.7 to 3.6V
19	D_0	Output Data (LSB, 13 bit output or 1Vpp full scale range)
20	D_1	Output Data (LSB, 12 bit output 2Vpp full scale range)

Table 2: Pin Function

Pin #	Name	Description
21	D_2	Output Data
22	D_3	Output Data
23	D_4	Output Data
24	ORNG	Out of Range flag. High when input signal is out of range
27	CK_EXT	Output clock signal for data synchronization. CMOS levels
28	D_5	Output Data
29	D_6	Output Data
30	D_7	Output Data
31	D_8	Output Data
32	D_9	Output Data
33	D_10	Output Data
34	D_11	Output Data (MSB for 1Vpp full scale range, see Reference Voltages section)
35	D_12	Output Data (MSB for 2Vpp full scale range)
38, 39	CM_EXTBC_1, CM_EXTBC_0	Bias control bits for the buffer driving pin CM_EXT 00: OFF 01: 50uA 10: 500uA 11: 1mA
40	SLP_N	Sleep Mode when low

Recommended Usage

Analog Input

The analog inputs to the HMCAD1051-40 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The CM_EXT pin provides a voltage suitable as common mode voltage reference. The internal buffer for the CM_EXT voltage can be switched off, and driving capabilities can be changed by using the CM_EXTBC control input.

Figure 4 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22 Ohm) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

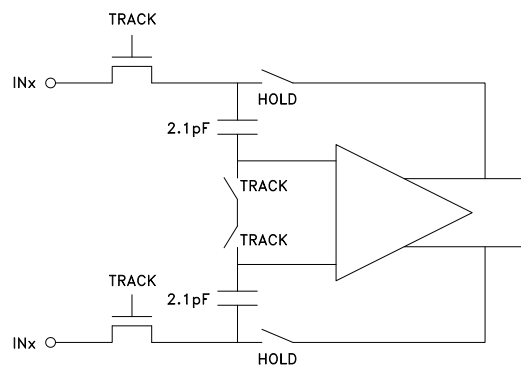


Figure 4: Input configuration

DC-Coupling

Figure 5 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as reference to set the common mode voltage.

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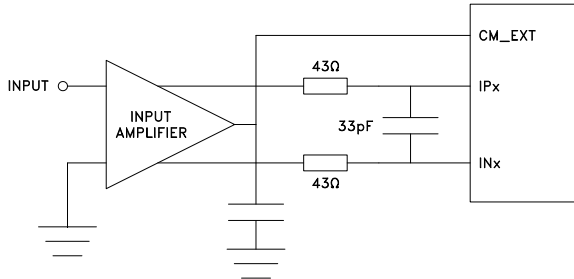


Figure 5: DC coupled input with buffer

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the HMCAD1051-40 input specifications.

Detailed configuration and usage instructions must be found in the documentation of the selected driver, and the values given in figure 5 must be varied according to the recommendations for the driver.

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 6 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to minimize phase mismatch between the differential ADC inputs for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in figure 8 can be used.

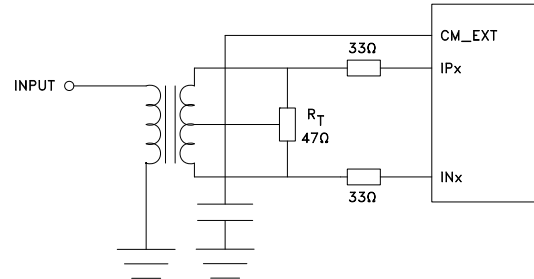


Figure 6: Transformer coupled input

Figure 7 shows AC-coupling using capacitors. Resistors from the CM_EXT output, R_{CM}, should be used to bias the differential input signals to the correct voltage. The series capacitor, C₁, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

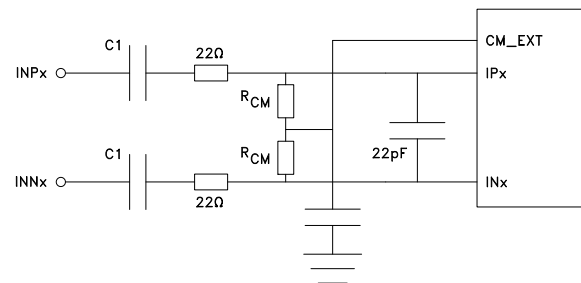


Figure 7: AC coupled input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of figure 8 can be used. The configuration in figure 8 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

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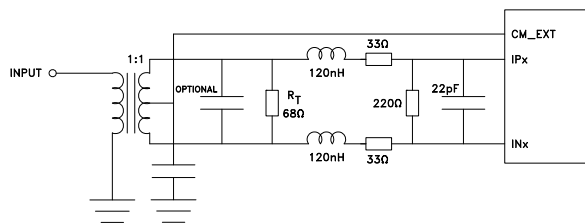


Figure 8: Alternative input network

Clock Input and Jitter considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the HMCAD1051-40 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% are acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally. Hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CKN pin should be connected to ground, and the CMOS clock signal should be connected to CKP. For differential sine wave clock, the input amplitude must be at least ± 800 mVpp.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1,

$$SNR_{jitter} = 20 \cdot \log(2 \cdot \pi \cdot f_{IN} \cdot \epsilon_t) \quad (1)$$

where f_{IN} is the signal frequency, and ϵ_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter

performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be re-timed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Digital Outputs

Digital output data are presented on parallel CMOS form. The voltage on the OVDD pin set the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OVDD above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CK_EXT always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE_N signal high.

The HMCAD1051-40 employs digital offset correction. This means that the output code will be 4096 with shorted inputs. However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of codes at the edges of the full scale range. With no offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for over range and all zeros for under range.

Note that the out of range flags (ORNG) will behave differently for 12 bit and 13 bit output. For 13 bit output ORNG will be set when digital output data are all ones or all zeros. For 12-bit output the ORNG flags will be set when all twelve bits are zeros or ones and when the thirteenth bit is equal to the rest of the bits.

Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connect to OVSS). Setting DFRMT high (connect to OVDD) results in 2's complement output format. Details are shown in table 3.

Table 3: Data Format Description for 2Vpp Full Scale Range

Differential Input Voltage (IP - IN)	Output data: D_12 : D_0 (DFRMT = 0, Offset Binary)	Output Data: D_12 : D_0 (DFRMT = 1, 2's Complement)
1.0 V	1 1111 1111 1111	0 1111 1111 1111
+0.24mV	1 0000 0000 0000	0 0000 0000 0000
-0.24mV	0 1111 1111 1111	1 1111 1111 1111
-1.0V	0 0000 0000 0000	1 0000 0000 0000

The data outputs can be used in three different configurations.

• **Normal mode:**

All 13 bits are used. MSB is D_12 and LSB is D_0. This mode gives optimum performance

• **12-bit mode:**

The LSB is left unconnected such that only 12 bits are used. MSB is D_12 and LSB is D_1. This mode gives slightly reduced performance due to increased quantization noise.

• **Reduced full scale range mode:**

The full scale range is reduced from 2 Vpp to 1 Vpp which is equivalent to 6 dB gain in the ADC frontend. Note that data are only available in 2's complement format in this mode. MSB is D_11 and LSB is D_0. Note that the codes will wrap around when exceeding the full scale range, and that out of range bits should be used to clamp output data. See section Reference Voltages for details. This mode gives slightly reduced performance

Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

If a lower full scale range is required the 13-bit output word provides sufficient resolution to perform digital scaling with an equivalent impact on noise compared to adjusting the reference voltages.

A simple way to obtain 1.0 Vpp input range with a 12-bit output word is shown in table 4. Note that only 2's complement output data are available in this mode and that out of range conditions must be determined based on a two bit output. The output code will wrap around when the code goes outside the full scale range. The out of range bits should be used to clamp the output data for over range conditions.

Table 4: Data Format Description for 1Vpp Full Scale Range

Differential Input Voltage (IP - IN)	Output Data D_11:D_0 (DFRMT = 0) (2's Complement)	Out of Range (Use Logical AND Function for &)	Output Data D_11:D_0 (DFRMT = 1) (2's Complement)	Out of Range (Use Logical AND Function for &)
> 0.5V	0111 1111 1111	D_12 = 1 & D_11 = 1	0111 1111 1111	D_12 = 0 & D_11 = 1
0.5V	0111 1111 1111		0111 1111 1111	
+0.24mV	0000 0000 0000		0000 0000 0000	
-0.24mV	1111 1111 1111		1111 1111 1111	
-0.5V	1000 0000 0000		1000 0000 0000	
< -0.5V	1000 0000 0000	D_12 = 0 & D_11 = 0	1000 0000 0000	D_12 = 1 & D_11 = 0

**SINGLE 13/12-BIT 20/40 MSPS
A/D CONVERTER****Operational Modes**

The operational modes are controlled with the PD_N and SLP_N pins. If PD_N is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for Sleep Mode as all references need to settle to their final values before normal operation can resume.

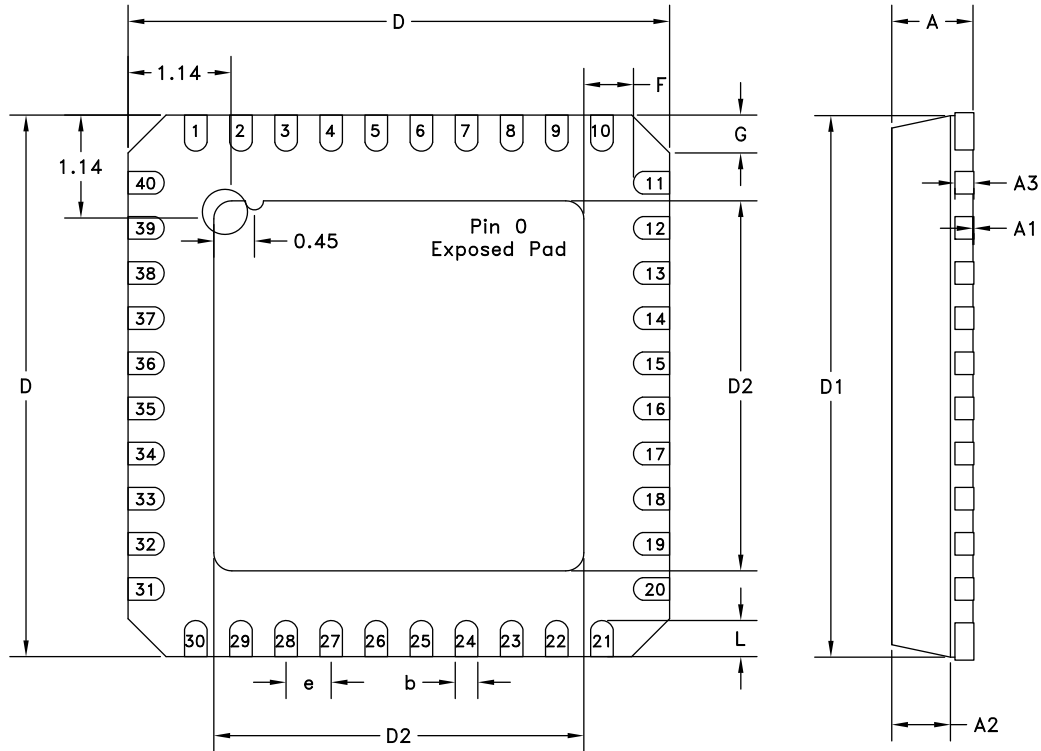
The SLP_N signal can be used to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

The input clock should be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

Startup Initialization

The HMCAD1051-40 must be reset prior to normal operation. This is required every time the power supply voltage has been switched off. A reset is performed by applying Power Down mode. Wait until a stable supply voltage has been reached, and pull the PD_N pin for the duration of at least one clock cycle. The input clock must be running continuously during this Power Down period and until active operation is reached. Alternatively the PD pin can be kept low during power-up, and then be set high when the power supply voltage is stable.

Outline Drawing



BOTTOM VIEW

Table 5: 6x6 mm QFN (40 Pin LP6H) Dimensions

Symbol	Millimeter			Inch		
	Min	Typ	Max	Min	Typ	Max
A			0.9			0.035
A1	0	0.01	0.05	0	0.000	0.002
A2		0.65	0.7		0.026	0.028
A3	0.2 REF			0.008 REF		
b	0.2	0.25	0.32	0.008	0.01	0.013
D	6.00 bsc			0.236 bsc		
D1	5.75 bsc			0.226 bsc		
D2	3.95	4.1	4.25	0.156	0.162	0.167
L	0.3	0.4	0.5	0.012	0.016	0.02
e	0.50 bsc			0.020 bsc		
Θ1	0°		12°	0°		12°
F	0.2			0.008		
G	0.24	0.42	0.6	0.010	0.017	0.024



**SINGLE 13/12-BIT 20/40 MSPS
A/D CONVERTER**

Package Information

Part Number	Package Body Material	Lead Finish	MSL [1]	Package Marking [2]
HMCAD1051-40	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	Level 2A	ASD0501 XXXX XXXX

[1] MSL, Peak Temp: The moisture sensitivity level rating classified according to the JEDEC industry standard and to peak solder temperature.

[2] Proprietary marking XXXX, 4-Digit lot number XXXX