■ FEATURES

€ **CPU**

- Instruction system best suited to controller
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
  - Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
  - Employing system stack pointer
  - Various enhanced pointer indirect instructions
  - Barrel shift instructions
- Increased processing speed
  - 4-byte instruction queue

€ **Serial interface**

- LIN-UART : 4 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- I^2C interface : 2 channels (only for devices with a C suffix in the part number)
  - Up to 400 kbps transfer rate

€ **Interrupt controller**

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported
- Automatic data transfer function independent of CPU
  - Expanded intelligent I/O service function (EI^2OS) : up to 16 channels

€ **I/O ports**

- General-purpose input/output port (CMOS output)
  - 80 ports (for devices without an S suffix in the part number - i.e. devices that support the sub clock)
  - 82 ports (for devices with an S suffix in the part number - i.e. devices that do not support the sub clock)

€ **8/10-bit A/D converter**

- 16 channels (only for devices without a C suffix in the part number)
- 24 channels (only for devices with a C suffix in the part number)
- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

€ **Address match detection (program patch) function**

- Detects address matches against 6 address pointers

€ **Timer**

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit × 16 channels, or 16-bit × 8 channels
- 16-bit reload timer : 4 channels
- 16-bit input/output timer
  - 16-bit free-run timer : 2 channels
  (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture: (ICU): 8 channels
  - 16-bit output compare: (OCU): 8 channels

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€ **Full-CAN controller**
- Up to 2 channels
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 16 built-in message buffers
- CAN wake-up function

€ **Low power consumption (standby) mode**
- Sleep mode (a mode that halts CPU operating clock)
- Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

€ **Clock modulation circuit**

€ **Technology**
- CMOS technology

■ PRODUCT LINEUP

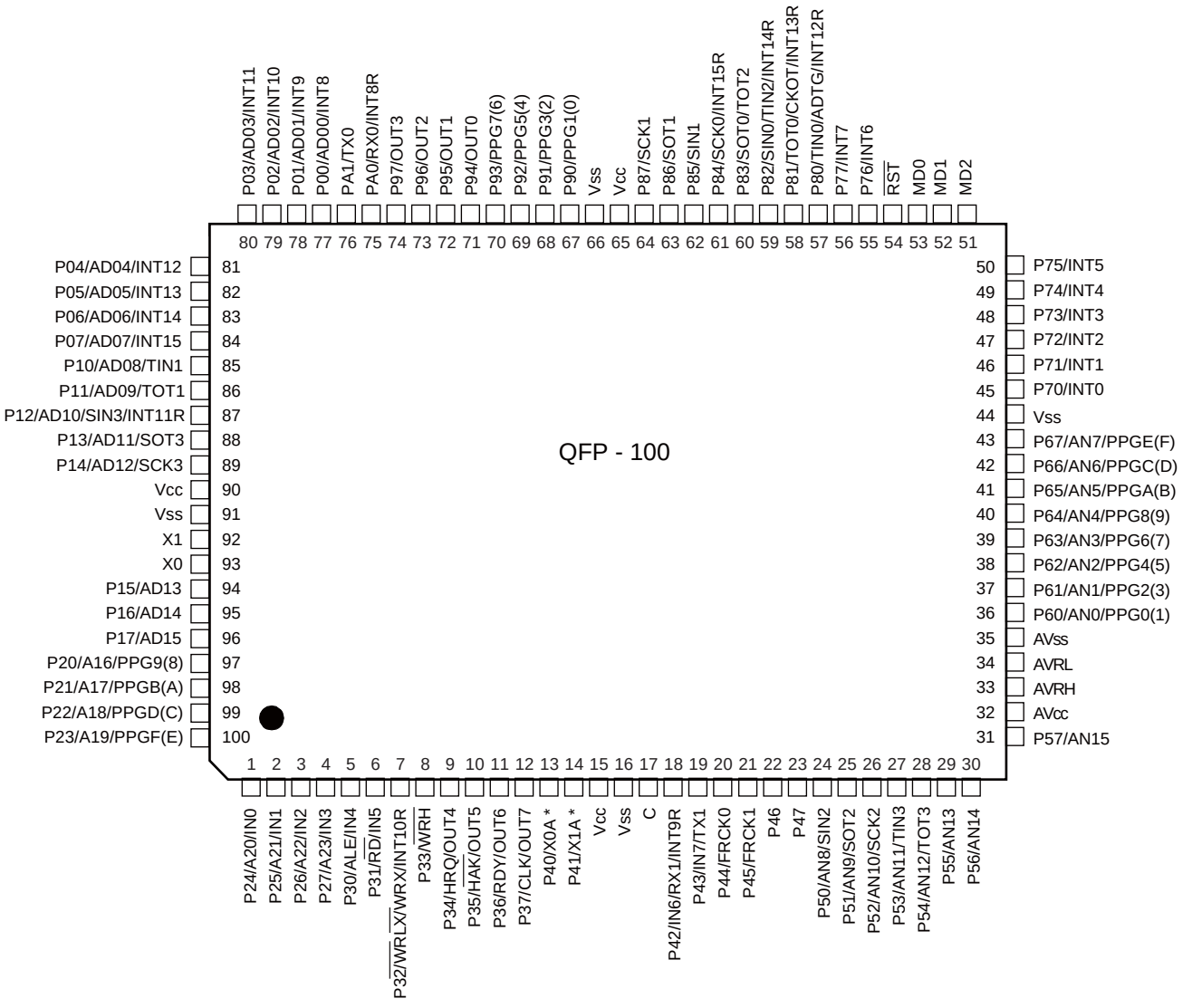
Part Number / Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes		
Technology	0.35 µm CMOS with regulator for built-in power supply	0.35 µm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range		Š 40 °C to +105 °C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I²C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number :	

(Continued)

■ PIN ASSIGNMENTS

- MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)

(TOP VIEW)



(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

(Continued)

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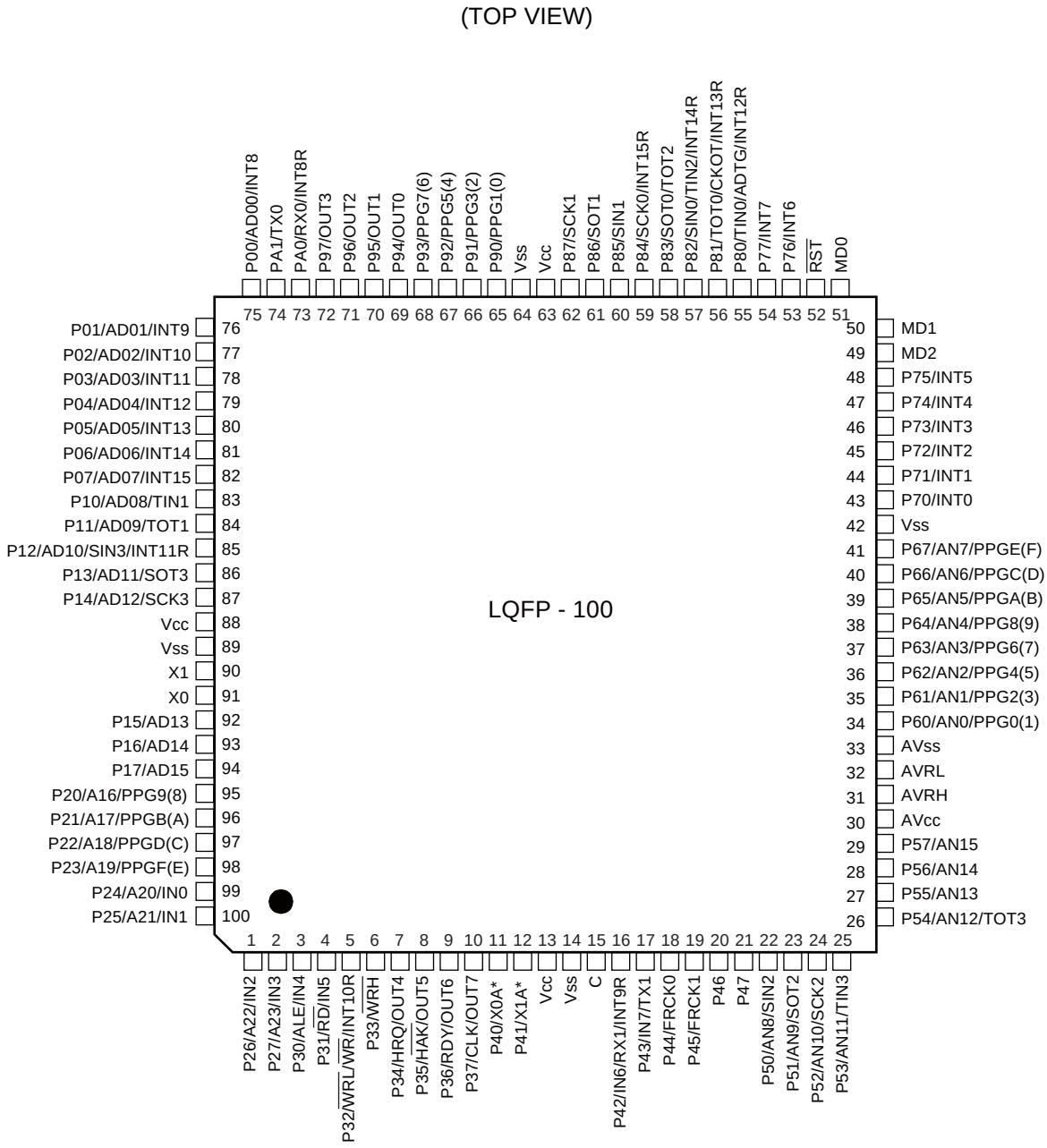
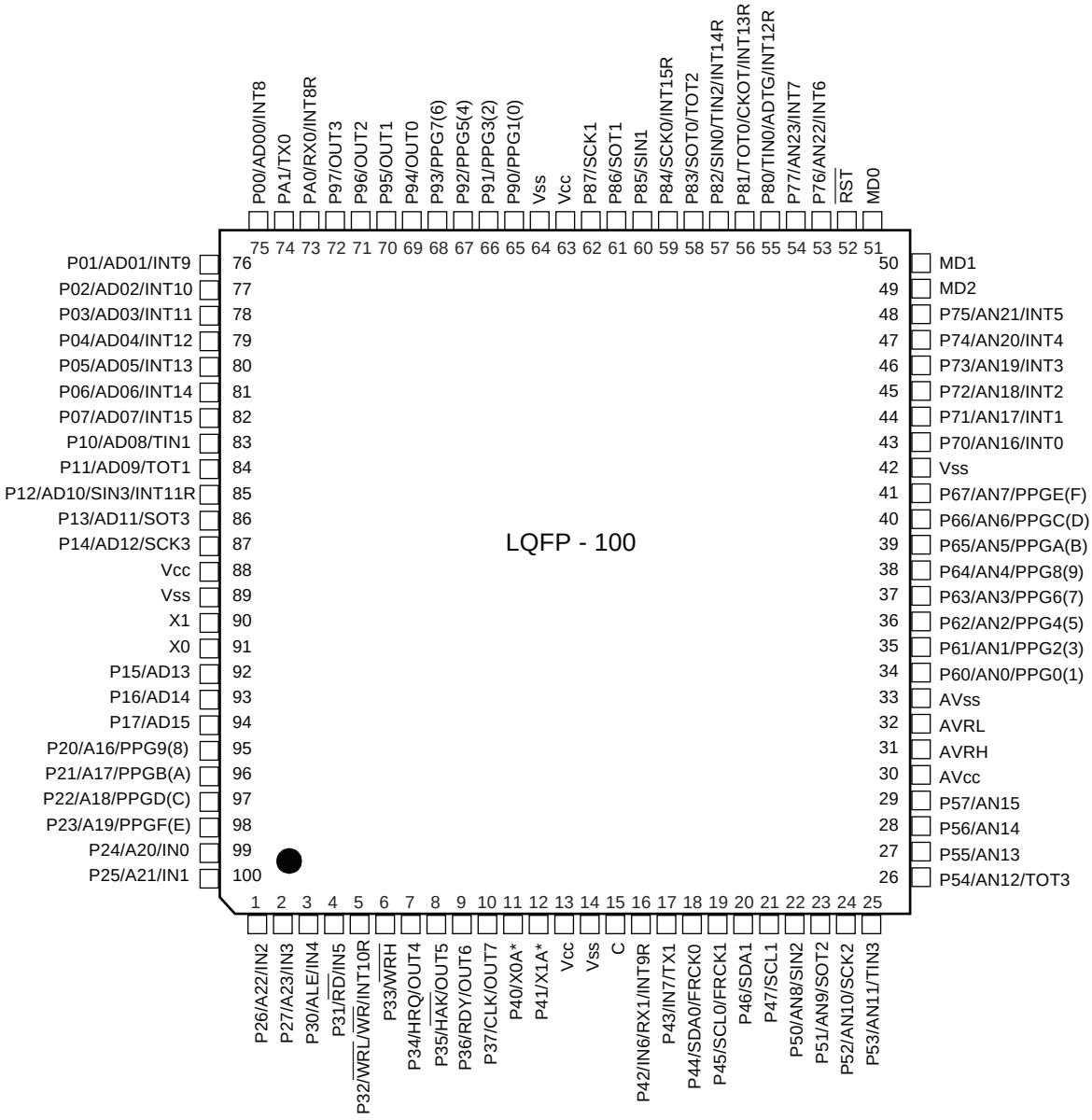


(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

(Continued)

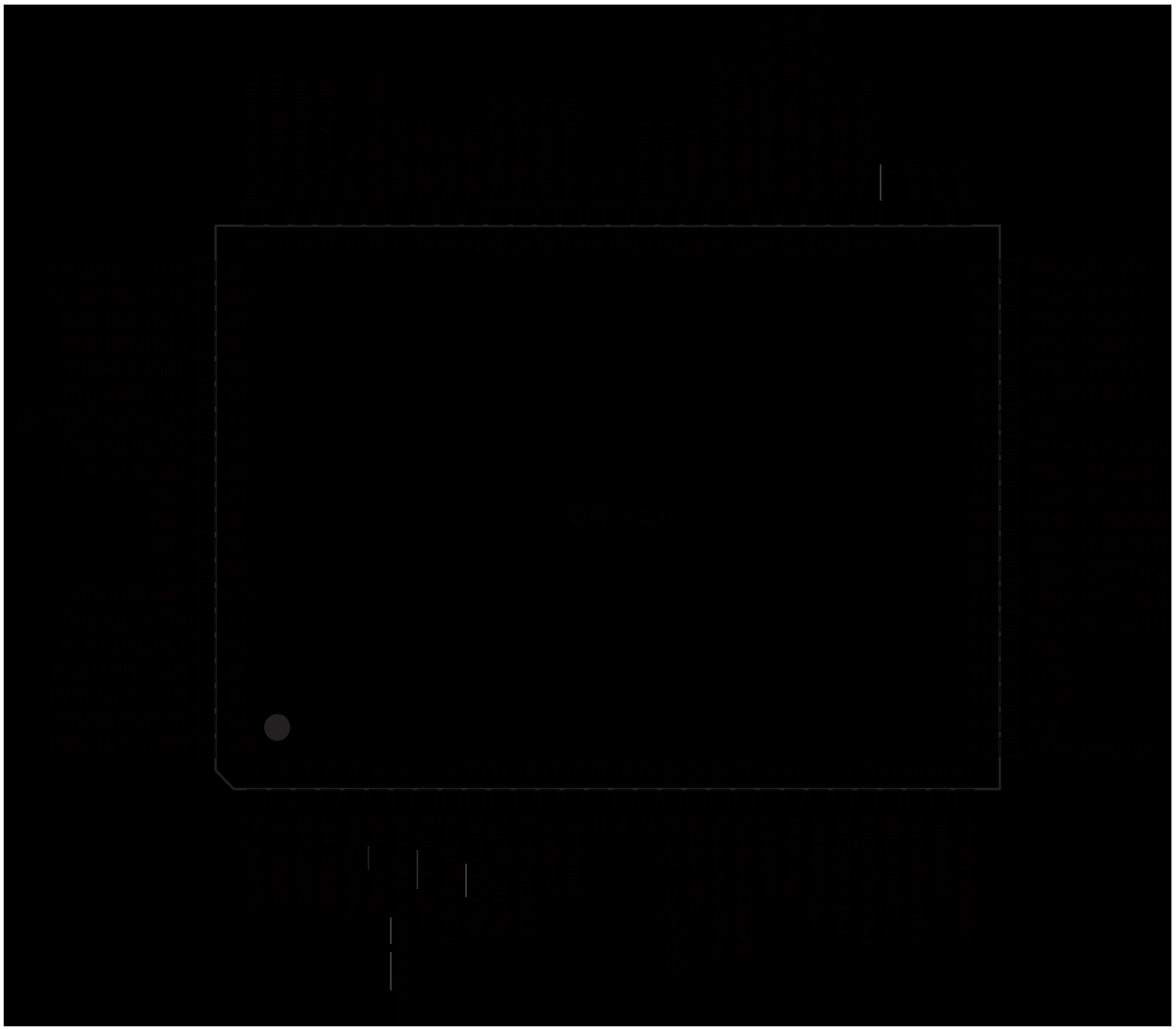
(TOP VIEW)



(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

- MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

(Continued)

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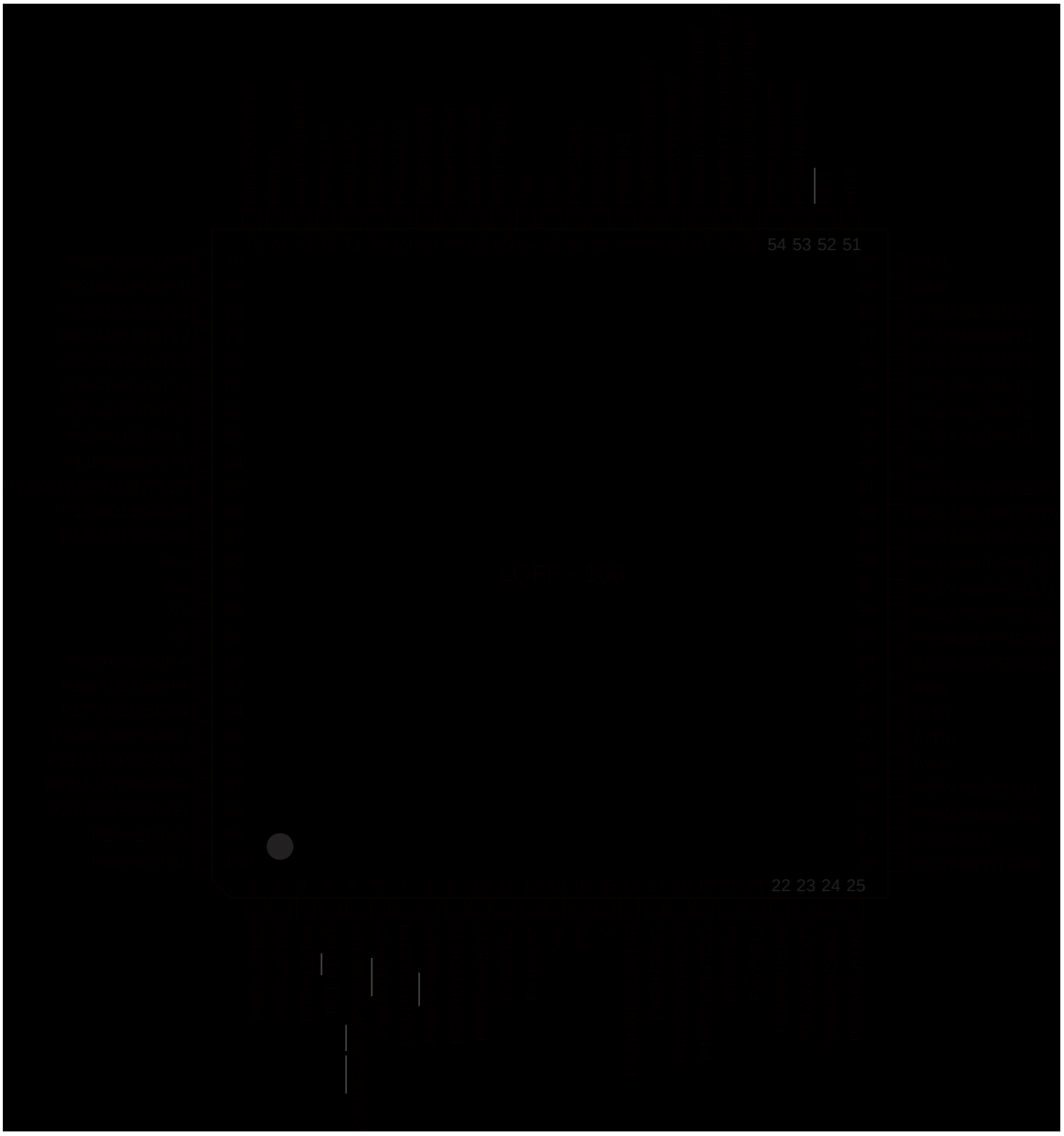


This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V_{CC}		Power (3.5 V to 5.5 V) input pin
16	14	V_{SS}		GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF.
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

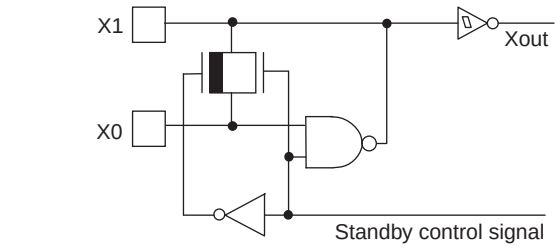
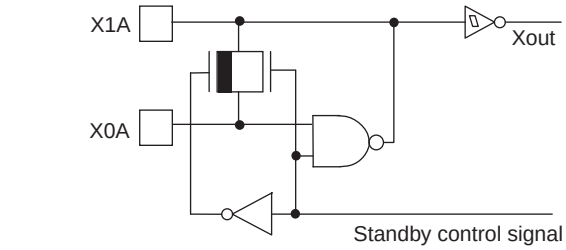
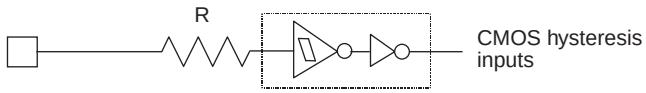
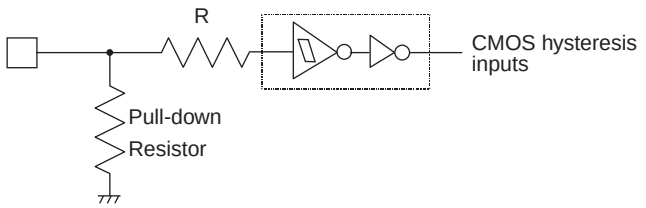
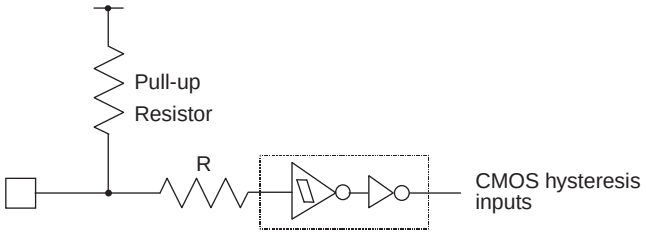
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I²C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I²C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I²C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I²C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV_{CC}	K	Analog power input pin for the A/D Converter

(Continued)

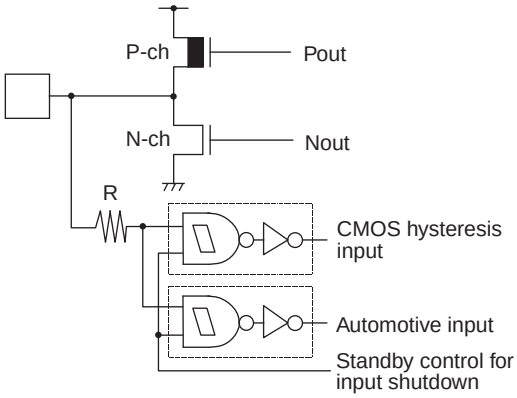
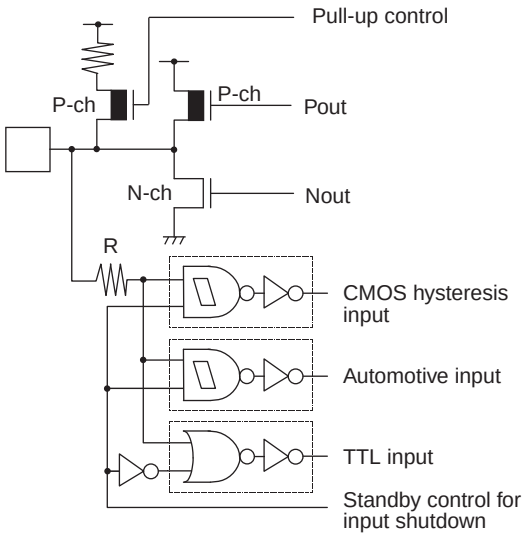
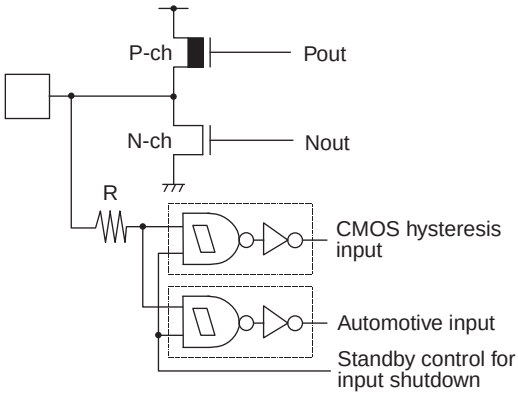
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V_{CC}		Power (3.5 V to 5.5 V) input pin
91	89	V_{SS}		GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

(Continued)

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 M
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 M
C		• MASK ROM and evaluation products: CMOS hysteresis input pin • Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: • CMOS hysteresis input pin • Pull-down resistor value: approx. 50 k Flash memory products: • CMOS input pin • No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 k

(Continued)

Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = Š4 mA) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = Š4 mA) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • Programmable pull-up resistor: 50 k approx.
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = Š3 mA) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)

(Continued)

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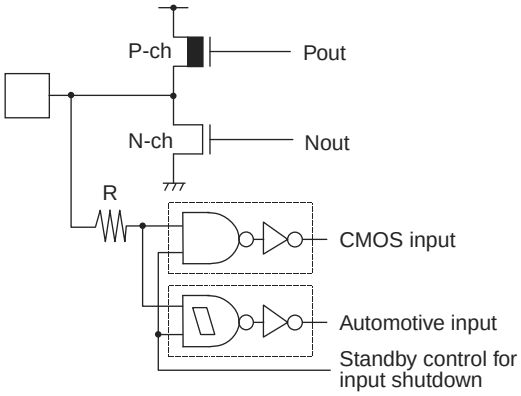
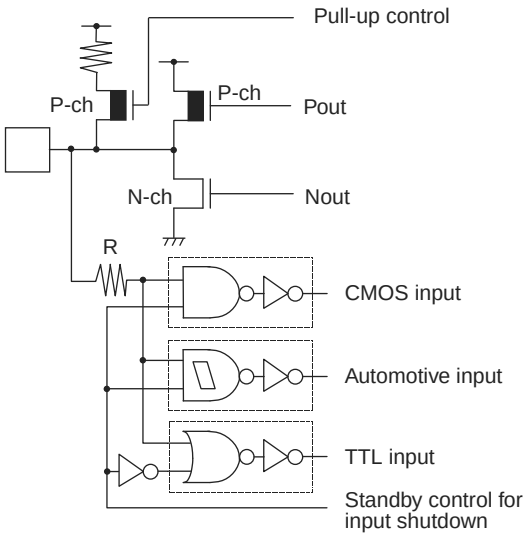
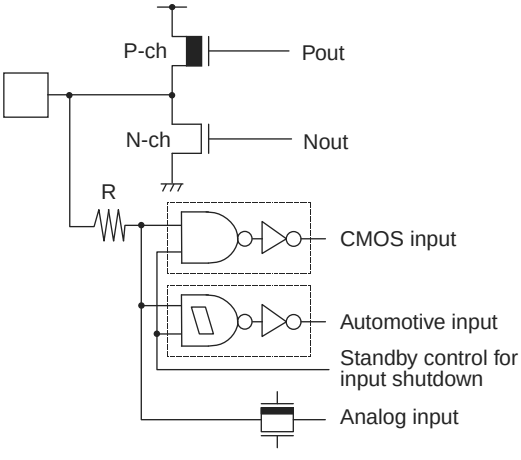
Type	Circuit	Remarks
M		• CMOS level output (I_{OL} = 4 mA, I_{OH} = Š4 mA) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = Š4 mA) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 k approx
O		• CMOS level output (I_{OL} = 4 mA, I_{OH} = Š4 mA) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input

■ HANDLING DEVICES

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

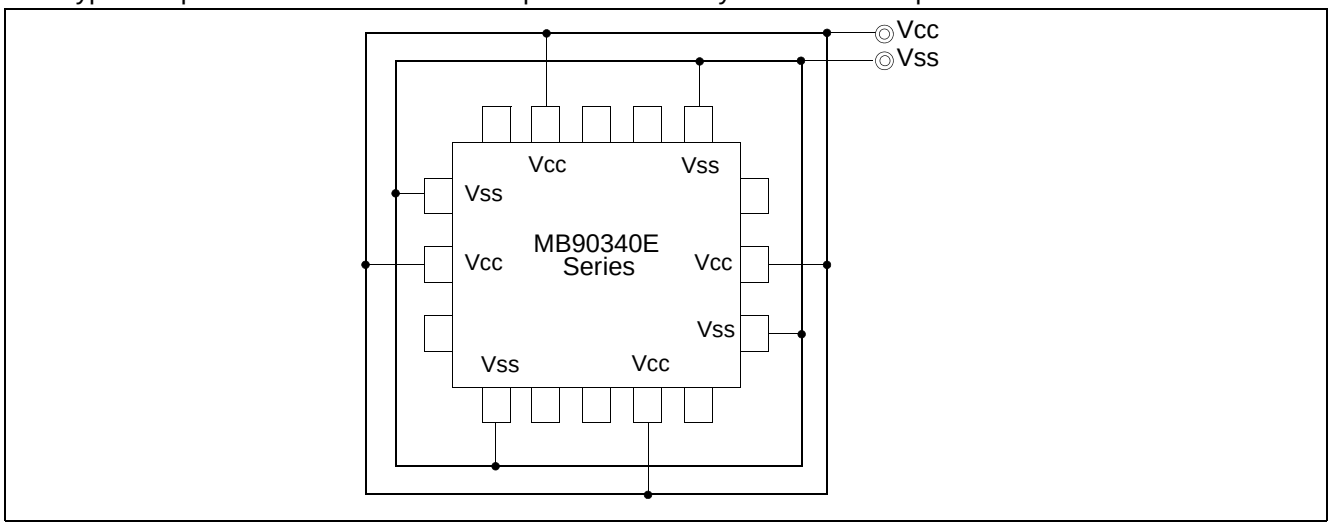
For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Handling unused pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
  Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

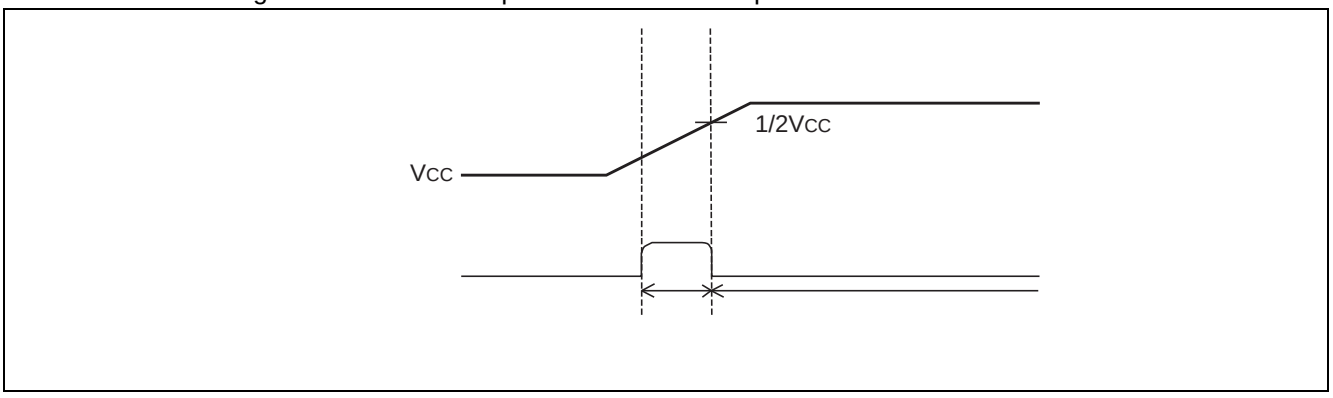
Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14. Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



15. Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

16. Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.
If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Refer to following table for the address of the security bit.

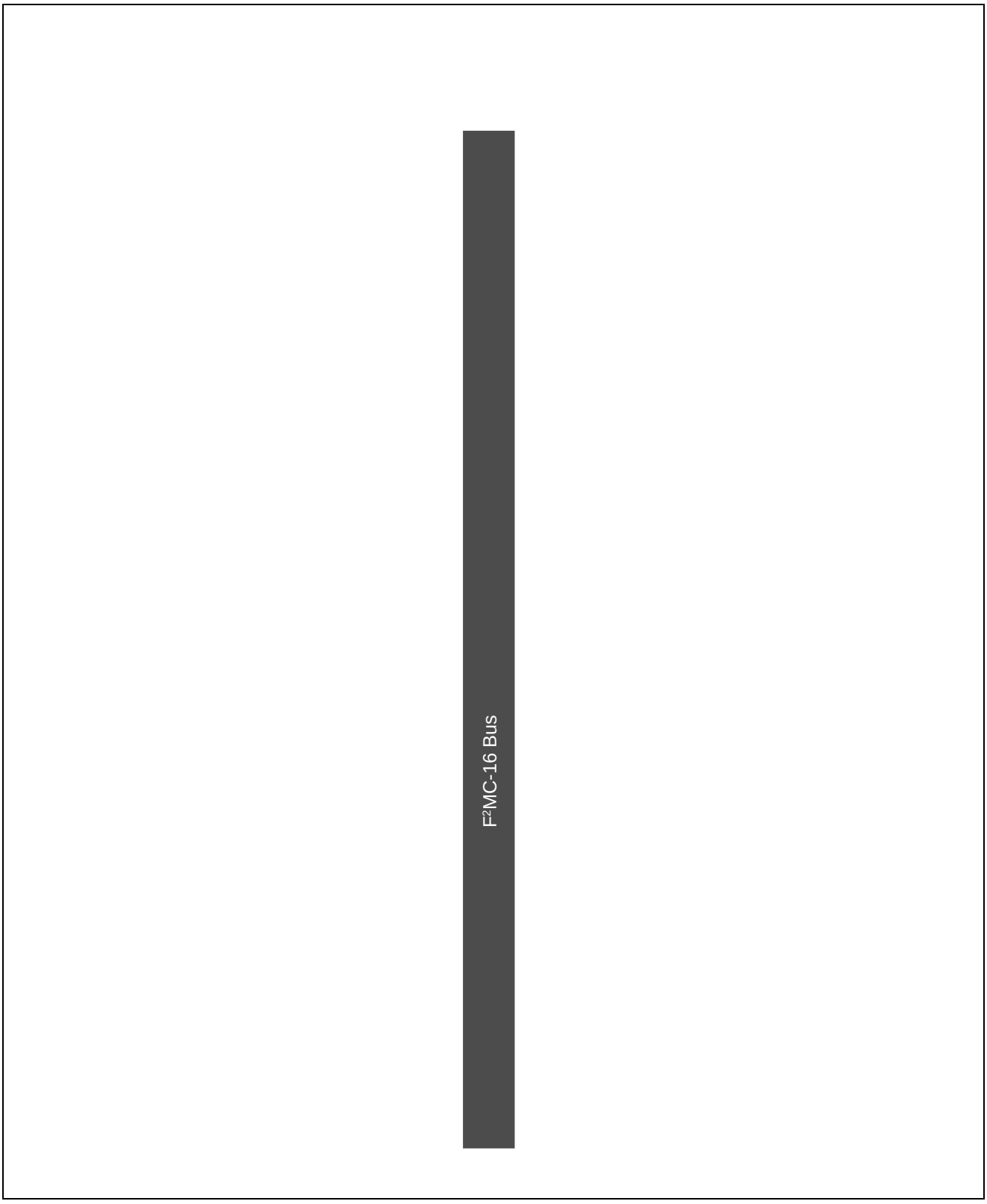
	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	$FE0001_H$
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	$FC0001_H$
MB90F345E	Embedded 4 Mbits Flash Memory	$F80001_H$

17. Serial Communication

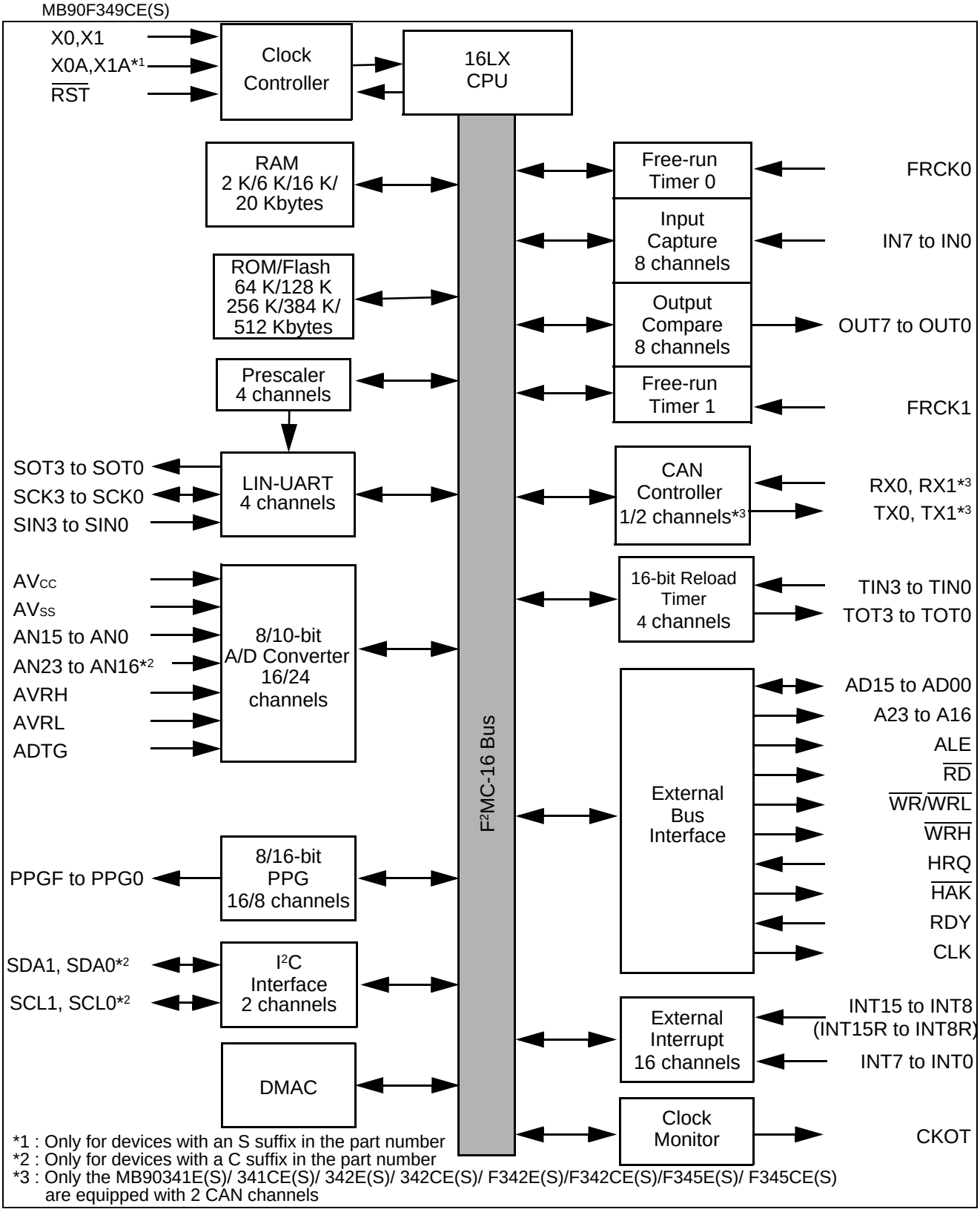
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

■ BLOCK DIAGRAMS

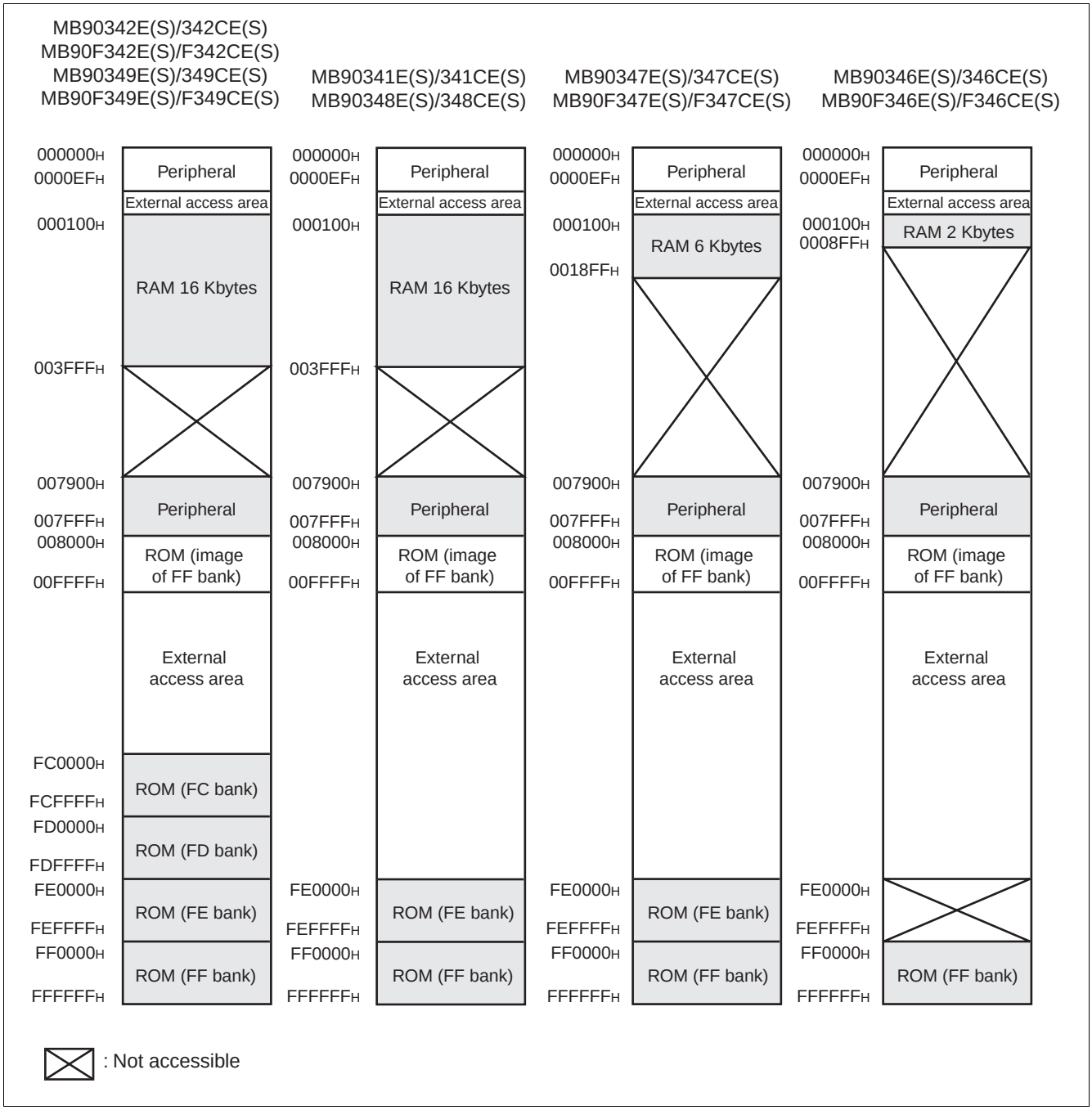
- MB90V340E-101/102



- MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



*1 : Only for devices with an S suffix in the part number
*2 : Only for devices with a C suffix in the part number
*3 : Only the MB90341E(S)/ 341CE(S)/ 342E(S)/ 342CE(S)/ F342E(S)/F342CE(S)/F345E(S)/ F345CE(S) are equipped with 2 CAN channels



Note: An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address 00C000H is accessed, the data at FFC000H in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
000000H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH	Port A Data Register	PDRA	R/W	Port A	XXXXXXXXB
00000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111B
00000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111B
00000DH	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	11111111B
00000EH	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXXB
00000FH	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXXB
000010H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000B
000012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000B
000013H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000B
00001AH	Port A Direction Register	DDRA	R/W	Port A	00000100B
00001BH	Reserved				
00001CH	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000B
00001DH	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000B
00001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000B
00001FH	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	00000000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000020H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000B
000021H	Serial Control Register 0	SCR0	W,R/W		00000000B
000022H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000B
000023H	Serial Status Register 0	SSR0	R,R/W		00001000B
000024H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XXB
000025H	Extended Status/Control Register 0	ESCR0	R/W		00000100B
000026H	Baud Rate Generator Register 00	BGR00	R/W		00000000B
000027H	Baud Rate Generator Register 01	BGR01	R/W		00000000B
000028H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000B
000029H	Serial Control Register 1	SCR1	W,R/W		00000000B
00002AH	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000B
00002BH	Serial Status Register 1	SSR1	R,R/W		00001000B
00002CH	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XXB
00002DH	Extended Status/Control Register 1	ESCR1	R/W		00000100B
00002EH	Baud Rate Generator Register 10	BGR10	R/W		00000000B
00002FH	Baud Rate Generator Register 11	BGR11	R/W		00000000B
000030H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1B
000031H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001B
000032H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0B
000033H	Reserved				
000034H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1B
000035H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001B
000036H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0B
000037H	Reserved				
000038H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1B
000039H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001B
00003AH	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0B
00003BH	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000B
00003CH	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1B
00003DH	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001B
00003EH	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0B
00003FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000040H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1B
000041H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001B
000042H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0B
000043H	Reserved				
000044H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1B
000045H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001B
000046H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0B
000047H	Reserved				
000048H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1B
000049H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001B
00004AH	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0B
00004BH	Reserved				
00004CH	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1B
00004DH	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001B
00004EH	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0B
00004FH	Reserved				
000050H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000B
000051H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XXB
000052H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000B
000053H	Input Capture Edge 2/3	ICE23	R		XXXXXXXXB
000054H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000B
000055H	Input Capture Edge 4/5	ICE45	R		XXXXXXXXB
000056H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000B
000057H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XXB
000058H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00B
000059H	Output Compare Control Status 1	OCS1	R/W		0XX00000B
00005AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00B
00005BH	Output Compare Control Status 3	OCS3	R/W		0XX00000B
00005CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00B
00005DH	Output Compare Control Status 5	OCS5	R/W		0XX00000B
00005EH	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00B
00005FH	Output Compare Control Status 7	OCS7	R/W		0XX00000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000060H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000B
000061H	Timer Control Status 0	TMCSR0	R/W		XXXX0000B
000062H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000B
000063H	Timer Control Status 1	TMCSR1	R/W		XXXX0000B
000064H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000B
000065H	Timer Control Status 2	TMCSR2	R/W		XXXX0000B
000066H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000B
000067H	Timer Control Status 3	TMCSR3	R/W		XXXX0000B
000068H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0B
000069H	A/D Control Status 1	ADCS1	R/W		0000000XB
00006AH	A/D Data 0	ADCR0	R		00000000B
00006BH	A/D Data 1	ADCR1	R		XXXXXX00B
00006CH	ADC Setting 0	ADSR0	R/W		00000000B
00006DH	ADC Setting 1	ADSR1	R/W		00000000B
00006EH	Reserved				
00006FH	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXX1B
000070H to 00008FH	Reserved for CAN Controller 0/1. Refer to "■ CAN CONTROLLERS"				
000090H to 00009AH	Reserved				
00009BH	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000B
00009CH	DMA Status L Register	DSRL	R/W		00000000B
00009DH	DMA Status H Register	DSRH	R/W		00000000B
00009EH	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000B
00009FH	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXX0B
0000A0H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000B
0000A1H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100B
0000A2H, 0000A3H	Reserved				
0000A4H	DMA Stop Status Register	DSSR	R/W	DMA	00000000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00B
0000A6H	External Address Output Control Register	HACR	W		00000000B
0000A7H	Bus Control Signal Selection Register	ECSR	W		0000000XB
0000A8H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111B
0000A9H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100B
0000AAH	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000B
0000ABH	Reserved				
0000ACH	DMA Enable L Register	DERL	R/W	DMA	00000000B
0000ADH	DMA Enable H Register	DERH	R/W		00000000B
0000AEH	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000B
0000AFH	Reserved				
0000B0H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111B
0000B1H	Interrupt Control Register 01	ICR01	W,R/W		00000111B
0000B2H	Interrupt Control Register 02	ICR02	W,R/W		00000111B
0000B3H	Interrupt Control Register 03	ICR03	W,R/W		00000111B
0000B4H	Interrupt Control Register 04	ICR04	W,R/W		00000111B
0000B5H	Interrupt Control Register 05	ICR05	W,R/W		00000111B
0000B6H	Interrupt Control Register 06	ICR06	W,R/W		00000111B
0000B7H	Interrupt Control Register 07	ICR07	W,R/W		00000111B
0000B8H	Interrupt Control Register 08	ICR08	W,R/W		00000111B
0000B9H	Interrupt Control Register 09	ICR09	W,R/W		00000111B
0000BAH	Interrupt Control Register 10	ICR10	W,R/W		00000111B
0000BBH	Interrupt Control Register 11	ICR11	W,R/W		00000111B
0000BCH	Interrupt Control Register 12	ICR12	W,R/W		00000111B
0000BDH	Interrupt Control Register 13	ICR13	W,R/W		00000111B
0000BEH	Interrupt Control Register 14	ICR14	W,R/W		00000111B
0000BFH	Interrupt Control Register 15	ICR15	W,R/W		00000111B
0000C0H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXXB
0000C1H	D/A Converter Data 1	DAT1	R/W		XXXXXXXXB
0000C2H	D/A Control 0	DACR0	R/W		XXXXXXX0B
0000C3H	D/A Control 1	DACR1	R/W		XXXXXXX0B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000C4H, 0000C5H	Reserved				
0000C6H	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000B
0000C7H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXXB
0000C8H	External Interrupt Level Setting 0	ELVR0	R/W		00000000B
0000C9H	External Interrupt Level Setting 0	ELVR0	R/W		00000000B
0000CAH	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000B
0000CBH	External Interrupt Source 1	EIRR1	R/W		XXXXXXXXB
0000CCH	External Interrupt Level Setting 1	ELVR1	R/W		00000000B
0000CDH	External Interrupt Level Setting 1	ELVR1	R/W		00000000B
0000CEH	External Interrupt Source Select	EISSR	R/W		00000000B
0000CFH	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000B
0000D0H	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXXB
0000D1H	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXXB
0000D2H	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXXB
0000D3H	DMA Control Register	DMACS	R/W		XXXXXXXXB
0000D4H	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXXB
0000D5H	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXXB
0000D6H	Data Counter L Register	DCTL	R/W		XXXXXXXXB
0000D7H	Data Counter H Register	DCTH	R/W		XXXXXXXXB
0000D8H	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000B
0000D9H	Serial Control Register 2	SCR2	W,R/W		00000000B
0000DAH	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000B
0000DBH	Serial Status Register 2	SSR2	R,R/W		00001000B
0000DCH	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XXB
0000DDH	Extended Status Control Register 2	ESCR2	R/W		00000100B
0000DEH	Baud Rate Generator Register 20	BGR20	R/W		00000000B
0000DFH	Baud Rate Generator Register 21	BGR21	R/W		00000000B
0000E0H to 0000EFH	Reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0000F0H to 0000FFH	External				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900H	Reload Register L0	PRLL0	R/W	16-bit PPG 0/1	XXXXXXXXB
007901H	Reload Register H0	PRLH0	R/W		XXXXXXXXB
007902H	Reload Register L1	PRLL1	R/W		XXXXXXXXB
007903H	Reload Register H1	PRLH1	R/W		XXXXXXXXB
007904H	Reload Register L2	PRLL2	R/W	16-bit PPG 2/3	XXXXXXXXB
007905H	Reload Register H2	PRLH2	R/W		XXXXXXXXB
007906H	Reload Register L3	PRLL3	R/W		XXXXXXXXB
007907H	Reload Register H3	PRLH3	R/W		XXXXXXXXB
007908H	Reload Register L4	PRLL4	R/W	16-bit PPG 4/5	XXXXXXXXB
007909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
00790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
00790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
00790CH	Reload Register L6	PRLL6	R/W	16-bit PPG 6/7	XXXXXXXXB
00790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
00790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
00790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
007910H	Reload Register L8	PRLL8	R/W	16-bit PPG 8/9	XXXXXXXXB
007911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
007912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
007913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
007914H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	XXXXXXXXB
007915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
007916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
007917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
007918H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	XXXXXXXXB
007919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
00791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
00791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
00791CH	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXXB
00791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
00791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
00791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
007920H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
007921H	Input Capture 0	IPCP0	R		XXXXXXXXB
007922H	Input Capture 1	IPCP1	R		XXXXXXXXB
007923H	Input Capture 1	IPCP1	R		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
007925H	Input Capture 2	IPCP2	R		XXXXXXXXB
007926H	Input Capture 3	IPCP3	R		XXXXXXXXB
007927H	Input Capture 3	IPCP3	R		XXXXXXXXB
007928H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
007929H	Input Capture 4	IPCP4	R		XXXXXXXXB
00792AH	Input Capture 5	IPCP5	R		XXXXXXXXB
00792BH	Input Capture 5	IPCP5	R		XXXXXXXXB
00792CH	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
00792DH	Input Capture 6	IPCP6	R		XXXXXXXXB
00792EH	Input Capture 7	IPCP7	R		XXXXXXXXB
00792FH	Input Capture 7	IPCP7	R		XXXXXXXXB
007930H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
007931H	Output Compare 0	OCCP0	R/W		XXXXXXXXB
007932H	Output Compare 1	OCCP1	R/W		XXXXXXXXB
007933H	Output Compare 1	OCCP1	R/W		XXXXXXXXB
007934H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
007935H	Output Compare 2	OCCP2	R/W		XXXXXXXXB
007936H	Output Compare 3	OCCP3	R/W		XXXXXXXXB
007937H	Output Compare 3	OCCP3	R/W		XXXXXXXXB
007938H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXXB
007939H	Output Compare 4	OCCP4	R/W		XXXXXXXXB
00793AH	Output Compare 5	OCCP5	R/W		XXXXXXXXB
00793BH	Output Compare 5	OCCP5	R/W		XXXXXXXXB
00793CH	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXXB
00793DH	Output Compare 6	OCCP6	R/W		XXXXXXXXB
00793EH	Output Compare 7	OCCP7	R/W		XXXXXXXXB
00793FH	Output Compare 7	OCCP7	R/W		XXXXXXXXB
007940H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000B
007941H	Timer Data 0	TCDT0	R/W		00000000B
007942H	Timer Control Status 0	TCCSL0	R/W		00000000B
007943H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXB
007944H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000B
007945H	Timer Data 1	TCDT1	R/W		00000000B
007946H	Timer Control Status 1	TCCSL1	R/W		00000000B
007947H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007948H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXXB
007949H			R/W		XXXXXXXXB
00794AH	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXXB
00794BH			R/W		XXXXXXXXB
00794CH	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXXB
00794DH			R/W		XXXXXXXXB
00794EH	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXXB
00794FH			R/W		XXXXXXXXB
007950H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000B
007951H	Serial Control Register 3	SCR3	W,R/W		00000000B
007952H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000B
007953H	Serial Status Register 3	SSR3	R,R/W		00001000B
007954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
007955H	Extended Status Control Register	ESCR3	R/W		00000100B
007956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
007957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
007958H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000B
007959H	Serial Control Register 4	SCR4	W,R/W		00000000B
00795AH	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000B
00795BH	Serial Status Register 4	SSR4	R,R/W		00001000B
00795CH	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XXB
00795DH	Extended Status Control Register	ESCR4	R/W		00000100B
00795EH	Baud Rate Generator Register 40	BGR40	R/W		00000000B
00795FH	Baud Rate Generator Register 41	BGR41	R/W		00000000B
007960H to 00796BH	Reserved				
00796CH	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000B
00796DH	Reserved				
00796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXX0B
00796FH	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXX00B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
007971H	I²C Bus Control Register 0	IBCR0	W,R/W		00000000B
007972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
007973H		ITBAH0	R/W		00000000B
007974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
007975H		ITMKH0	R/W		00111111B
007976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
007977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
007978H	I²C Data Register 0	IDAR0	R/W		00000000B
007979H, 00797AH	Reserved				
00797BH	I²C Clock Control Register 0	ICCR0	R/W	I²C Interface 0	00011111B
00797CH to 00797FH	Reserved				
007980H	I²C Bus Status Register 1	IBSR1	R	I²C Interface 1	00000000B
007981H	I²C Bus Control Register 1	IBCR1	W,R/W		00000000B
007982H	I²C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000B
007983H		ITBAH1	R/W		00000000B
007984H	I²C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111B
007985H		ITMKH1	R/W		00111111B
007986H	I²C 7-bit Slave Address Register 1	ISBA1	R/W		00000000B
007987H	I²C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111B
007988H	I²C Data Register 1	IDAR1	R/W		00000000B
007989H, 00798AH	Reserved				
00798BH	I²C Clock Control Register 1	ICCR1	R/W	I²C Interface 1	00011111B
00798CH to 0079C1H	Reserved				
0079C2H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000B
0079C3H to 0079DFH	Reserved				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
0079E1H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E2H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E3H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E4H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E5H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E6H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E7H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E8H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E9H to 0079EFH	Reserved				
0079F0H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
0079F1H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F2H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F3H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F4H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F5H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F6H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F7H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F8H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F9H to 0079FFH	Reserved				
007A00H to 007AFFH	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007B00H to 007BFFH	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007C00H to 007CFFH	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007D00H to 007DFFH	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007E00H to 007FFFH	Reserved				

Notes : € Initial value of “X” represents unknown value.

€ Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ CAN CONTROLLERS

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - € Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - € 29-bit ID and 8-byte data
  - € Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - € Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message Buffer Valid Register	BVALR	R/W	00000000_B 00000000_B
000071_H	000081_H				
000072_H	000082_H	Transmit Request Register	TREQR	R/W	00000000_B 00000000_B
000073_H	000083_H				
000074_H	000084_H	Transmit Cancel Register	TCANR	W	00000000_B 00000000_B
000075_H	000085_H				
000076_H	000086_H	Transmission Complete Register	TCR	R/W	00000000_B 00000000_B
000077_H	000087_H				
000078_H	000088_H	Receive Complete Register	RCR	R/W	00000000_B 00000000_B
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote Request Receiving Register	RRTRR	R/W	00000000_B 00000000_B
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive Overrun Register	ROVRR	R/W	00000000_B 00000000_B
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Reception Interrupt Enable Register	RIER	R/W	00000000_B 00000000_B
$00007F_H$	$00008F_H$				

List of Control Registers (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007B00H	007D00H	Control Status Register	CSR	R/W, W R/W, R	0XXXX0X1B 00XXX000B
007B01H	007D01H				
007B02H	007D02H	Last Event Indicator Register	LEIR	R/W	000X0000B XXXXXXXXB
007B03H	007D03H				
007B04H	007D04H	Receive And Transmit Error Counter	RTEC	R	00000000B 00000000B
007B05H	007D05H				
007B06H	007D06H	Bit Timing Register	BTR	R/W	11111111B X1111111B
007B07H	007D07H				
007B08H	007D08H	IDE Register	IDER	R/W	XXXXXXXXB XXXXXXXXB
007B09H	007D09H				
007B0AH	007D0AH	Transmit RTR Register	TRTRR	R/W	00000000B 00000000B
007B0BH	007D0BH				
007B0CH	007D0CH	Remote Frame Receive Waiting Register	RFWTR	R/W	XXXXXXXXB XXXXXXXXB
007B0DH	007D0DH				
007B0EH	007D0EH	Transmit Interrupt Enable Register	TIER	R/W	00000000B 00000000B
007B0FH	007D0FH				
007B10H	007D10H	Acceptance Mask Select Register	AMSR	R/W	XXXXXXXXB XXXXXXXXB
007B11H	007D11H				
007B12H	007D12H				XXXXXXXXB XXXXXXXXB
007B13H	007D13H				
007B14H	007D14H	Acceptance Mask Register 0	AMR0	R/W	XXXXXXXXB XXXXXXXXB
007B15H	007D15H				
007B16H	007D16H				XXXXXXXXB XXXXXXXXB
007B17H	007D17H				
007B18H	007D18H	Acceptance Mask Register 1	AMR1	R/W	XXXXXXXXB XXXXXXXXB
007B19H	007D19H				
007B1AH	007D1AH				XXXXXXXXB XXXXXXXXB
007B1BH	007D1BH				

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00H to 007A1FH	007C00H to 007C1FH	General-Purpose RAM		R/W	XXXXXXXXB to XXXXXXXXB
007A20H	007C20H	ID Register 0	IDR0	R/W	XXXXXXXXB
007A21H	007C21H				XXXXXXXXB
007A22H	007C22H				XXXXXXXXB
007A23H	007C23H				XXXXXXXXB
007A24H	007C24H	ID Register 1	IDR1	R/W	XXXXXXXXB
007A25H	007C25H				XXXXXXXXB
007A26H	007C26H				XXXXXXXXB
007A27H	007C27H				XXXXXXXXB
007A28H	007C28H	ID Register 2	IDR2	R/W	XXXXXXXXB
007A29H	007C29H				XXXXXXXXB
007A2AH	007C2AH				XXXXXXXXB
007A2BH	007C2BH				XXXXXXXXB
007A2CH	007C2CH	ID Register 3	IDR3	R/W	XXXXXXXXB
007A2DH	007C2DH				XXXXXXXXB
007A2EH	007C2EH				XXXXXXXXB
007A2FH	007C2FH				XXXXXXXXB
007A30H	007C30H	ID Register 4	IDR4	R/W	XXXXXXXXB
007A31H	007C31H				XXXXXXXXB
007A32H	007C32H				XXXXXXXXB
007A33H	007C33H				XXXXXXXXB
007A34H	007C34H	ID Register 5	IDR5	R/W	XXXXXXXXB
007A35H	007C35H				XXXXXXXXB
007A36H	007C36H				XXXXXXXXB
007A37H	007C37H				XXXXXXXXB
007A38H	007C38H	ID Register 6	IDR6	R/W	XXXXXXXXB
007A39H	007C39H				XXXXXXXXB
007A3AH	007C3AH				XXXXXXXXB
007A3BH	007C3BH				XXXXXXXXB
007A3CH	007C3CH	ID Register 7	IDR7	R/W	XXXXXXXXB
007A3DH	007C3DH				XXXXXXXXB
007A3EH	007C3EH				XXXXXXXXB
007A3FH	007C3FH				XXXXXXXXB

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A40H	007C40H	ID Register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
007A41H	007C41H				
007A42H	007C42H				XXXXXXXXB XXXXXXXXB
007A43H	007C43H				
007A44H	007C44H	ID Register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
007A45H	007C45H				
007A46H	007C46H				XXXXXXXXB XXXXXXXXB
007A47H	007C47H				
007A48H	007C48H	ID Register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
007A49H	007C49H				
007A4AH	007C4AH				XXXXXXXXB XXXXXXXXB
007A4BH	007C4BH				
007A4CH	007C4CH	ID Register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
007A4DH	007C4DH				
007A4EH	007C4EH				XXXXXXXXB XXXXXXXXB
007A4FH	007C4FH				
007A50H	007C50H	ID Register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
007A51H	007C51H				
007A52H	007C52H				XXXXXXXXB XXXXXXXXB
007A53H	007C53H				
007A54H	007C54H	ID Register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
007A55H	007C55H				
007A56H	007C56H				XXXXXXXXB XXXXXXXXB
007A57H	007C57H				
007A58H	007C58H	ID Register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
007A59H	007C59H				
007A5AH	007C5AH				XXXXXXXXB XXXXXXXXB
007A5BH	007C5BH				
007A5CH	007C5CH	ID Register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
007A5DH	007C5DH				
007A5EH	007C5EH				XXXXXXXXB XXXXXXXXB
007A5FH	007C5FH				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60H	007C60H	DLC Register 0	DLCR0	R/W	XXXXXXXXB
007A61H	007C61H				
007A62H	007C62H	DLC Register 1	DLCR1	R/W	XXXXXXXXB
007A63H	007C63H				
007A64H	007C64H	DLC Register 2	DLCR2	R/W	XXXXXXXXB
007A65H	007C65H				
007A66H	007C66H	DLC Register 3	DLCR3	R/W	XXXXXXXXB
007A67H	007C67H				
007A68H	007C68H	DLC Register 4	DLCR4	R/W	XXXXXXXXB
007A69H	007C69H				
007A6AH	007C6AH	DLC Register 5	DLCR5	R/W	XXXXXXXXB
007A6BH	007C6BH				
007A6CH	007C6CH	DLC Register 6	DLCR6	R/W	XXXXXXXXB
007A6DH	007C6DH				
007A6EH	007C6EH	DLC Register 7	DLCR7	R/W	XXXXXXXXB
007A6FH	007C6FH				
007A70H	007C70H	DLC Register 8	DLCR8	R/W	XXXXXXXXB
007A71H	007C71H				
007A72H	007C72H	DLC Register 9	DLCR9	R/W	XXXXXXXXB
007A73H	007C73H				
007A74H	007C74H	DLC Register 10	DLCR10	R/W	XXXXXXXXB
007A75H	007C75H				
007A76H	007C76H	DLC Register 11	DLCR11	R/W	XXXXXXXXB
007A77H	007C77H				
007A78H	007C78H	DLC Register 12	DLCR12	R/W	XXXXXXXXB
007A79H	007C79H				
007A7AH	007C7AH	DLC Register 13	DLCR13	R/W	XXXXXXXXB
007A7BH	007C7BH				
007A7CH	007C7CH	DLC Register 14	DLCR14	R/W	XXXXXXXXB
007A7DH	007C7DH				
007A7EH	007C7EH	DLC Register 15	DLCR15	R/W	XXXXXXXXB
007A7FH	007C7FH				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80H to 007A87H	007C80H to 007C87H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
007A88H to 007A8FH	007C88H to 007C8FH	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
007A90H to 007A97H	007C90H to 007C97H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
007A98H to 007A9FH	007C98H to 007C9FH	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
007AA0H to 007AA7H	007CA0H to 007CA7H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
007AA8H to 007AAFH	007CA8H to 007CAFH	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
007AB0H to 007AB7H	007CB0H to 007CB7H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
007AB8H to 007ABFH	007CB8H to 007CBFH	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
007AC0H to 007AC7H	007CC0H to 007CC7H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
007AC8H to 007ACFH	007CC8H to 007CCFH	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
007AD0H to 007AD7H	007CD0H to 007CD7H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
007AD8H to 007ADFH	007CD8H to 007CDFH	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
007AE0H to 007AE7H	007CE0H to 007CE7H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
007AE8H to 007AEFH	007CE8H to 007CEFH	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0H to 007AF7H	007CF0H to 007CF7H	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
007AF8H to 007AFFH	007CF8H to 007CFFH	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N		#08	FFFFDC$_H$		
INT9 instruction	N		#09	FFFFD8$_H$		
Exception	N		#10	FFFFD4$_H$		
CAN 0 RX	N		#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N		#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1		#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1		#14	FFFFC4$_H$		
CAN 2 RX / I²C0	N		#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 2 TX/NS	N		#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1		#20	FFFFAC$_H$		
PPG 0/1/4/5	N		#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N		#22	FFFFA4$_H$		
PPG 8/9/C/D	N		#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N		#24	FFFF9C$_H$		
Time Base Timer	N		#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N		#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / Free-run Timer 1	N		#30	FFFF84$_H$		
Input Capture 4/5 / I²C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	Y1	11	#36	FFFF6C$_H$		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64$_H$		

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Interrupt cause	EI²OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N		#41	FFFF58H	ICR15	0000BFH
Delayed Interrupt	N		#42	FFFF54H		

Y1 : Usable
Y2 : Usable, with EI²OS stop function
N : Unusable

Notes : € The peripheral resources sharing the ICR register have the same interrupt level.
€ When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
€ When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} Š 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} Š 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC}*2
	AVRH, AVRL	V_{SS} Š 0.3	V_{SS} + 6.0	V	AV_{CC} AVRH, AV_{CC} AVRL, AVRH AVRL
Input voltage*1	V_I	V_{SS} Š 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} Š 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	Š4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\|I_{CLAMP}\|$		40	mA	*5
“L” level maximum output current	I_{OL}		15	mA	*4, *6
“L” level average output current	I_{OLAV}		4	mA	*4, *7
“L” level maximum overall output current	I_{OL}		100	mA	*4
“L” level average overall output current	I_{OLAV}		50	mA	*4, *8
“H” level maximum output current	I_{OH}		Š 15	mA	*4, *6
“H” level average output current	I_{OHAV}		Š 4	mA	*4, *7
“H” level maximum overall output current	I_{OH}		Š 100	mA	*4
“H” level average overall output current	I_{OHAV}		Š 50	mA	*4, *8
Power consumption	P_D		450	mW	
Operating temperature	T_A	Š40	+105	°C	
Storage temperature	T_{STG}	Š55	+150	°C	

*1: This parameter is based on V_{SS} = AV_{SS} = 0 V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5: € Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

€ Use within recommended operating conditions.

€ Use with DC voltage (current)

€ The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.

€ The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.

€ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

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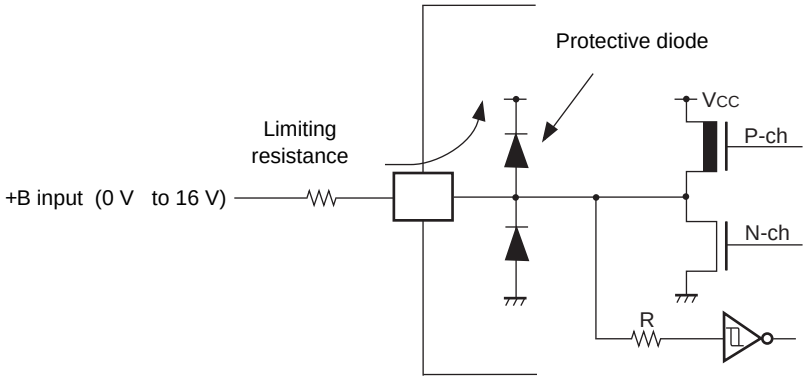
- € Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- € Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- € Care must be taken not to leave the +B input pin open.
- € Sample recommended circuits:

• Input/output equivalent circuits



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

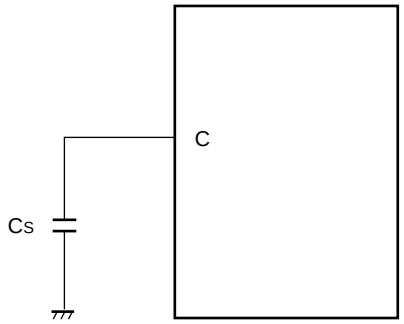
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0		5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1		1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	Š40		+ 105	°C	

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}			0.8 V_{CC}		V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}			0.8 V_{CC}		V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}			2.0		V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}			0.7 V_{CC}		V_{CC} + 0.3	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}			0.7 V_{CC}		V_{CC} + 0.3	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}			0.8 V_{CC}		V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}			V_{CC} Š0.3		V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}			V_{SS} Š0.3		0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}			V_{SS} Š0.3		0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}			V_{SS} Š0.3		0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}			V_{SS} Š0.3		0.3 V_{CC}	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}			V_{SS} Š0.3		0.3 V_{CC}	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}			V_{SS} Š0.3		0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}			V_{SS} Š0.3		V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = Š4.0 mA	V_{CC} Š0.5			V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = Š3.0 mA	V_{CC} Š0.5			V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA			0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA			0.4	V	

(Continued)

(Continued)

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}		V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	Š1		+ 1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$		25	50	100	k	
Pull-down resistance	R_{DOWN}	MD2		25	50	100	k	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.		55	70	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.		70	85	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.		75	90	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In Sleep mode.		25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode		0.3	0.8	mA	
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz		4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub operation T_A = +25°C		70	140	µA	
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub sleep T_A = +25°C		20	50	µA	
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In watch mode T_A = +25°C		10	35	µA	
	I_{CCH}		V_{CC} = 5.0 V, In Stop mode, T_A = +25°C		7	25	µA	
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}			5	15	pF	

* : The power supply current is measured with an external clock.

4. AC Characteristics

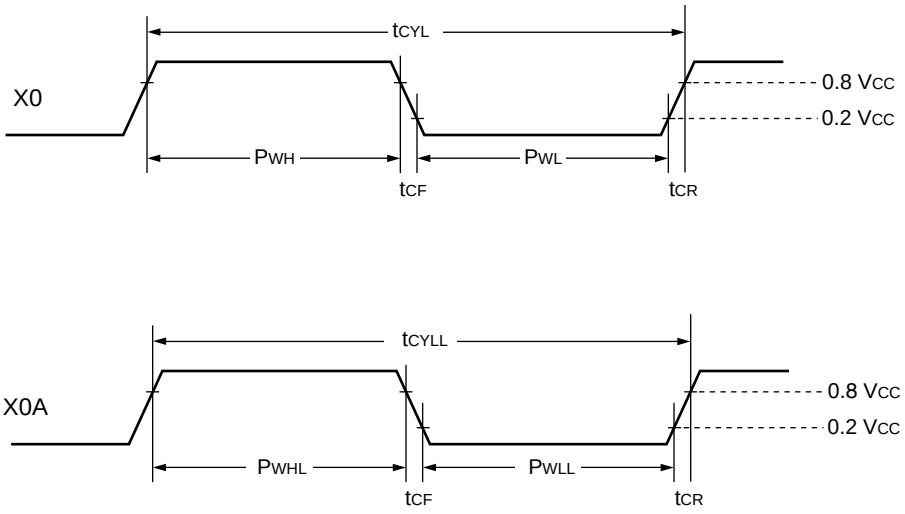
(1) Clock Timing

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0 V)

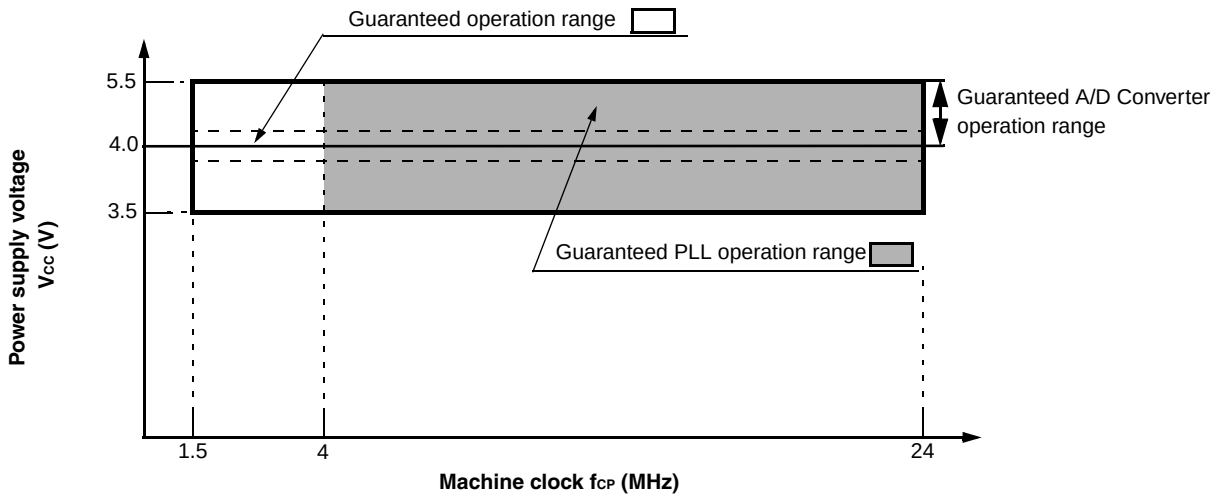
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3		16	MHz	When using an oscillation circuit
			4		16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4		12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4		8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4		6	MHz	PLL multiplied by 4 When using an oscillation circuit
					4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3		24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5		333	ns	When using an oscillation circuit
		X0, X1	41.67		333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10			ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2		µ s	
Input clock rise and fall time	t_{CR}, t_{CF}	X0			5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}		1.5		24	MHz	When using main clock
	f_{CPL}			8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}		41.67		666	ns	When using main clock
	t_{CPL}		20	122.1		µ s	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

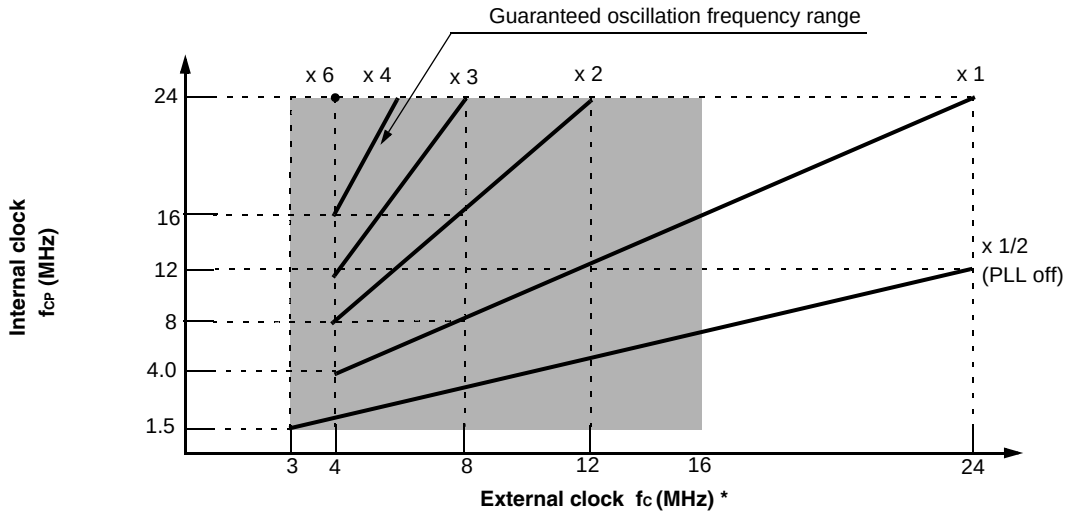
Clock Timing



Guaranteed PLL operation range



Guaranteed operation range of MB90340E series



* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

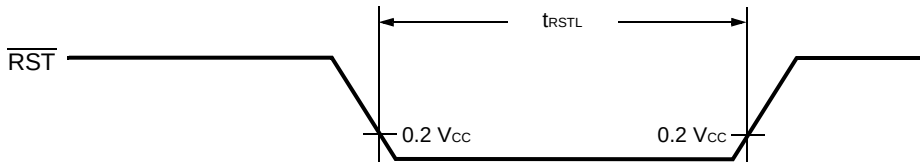
(2) Reset Standby Input

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

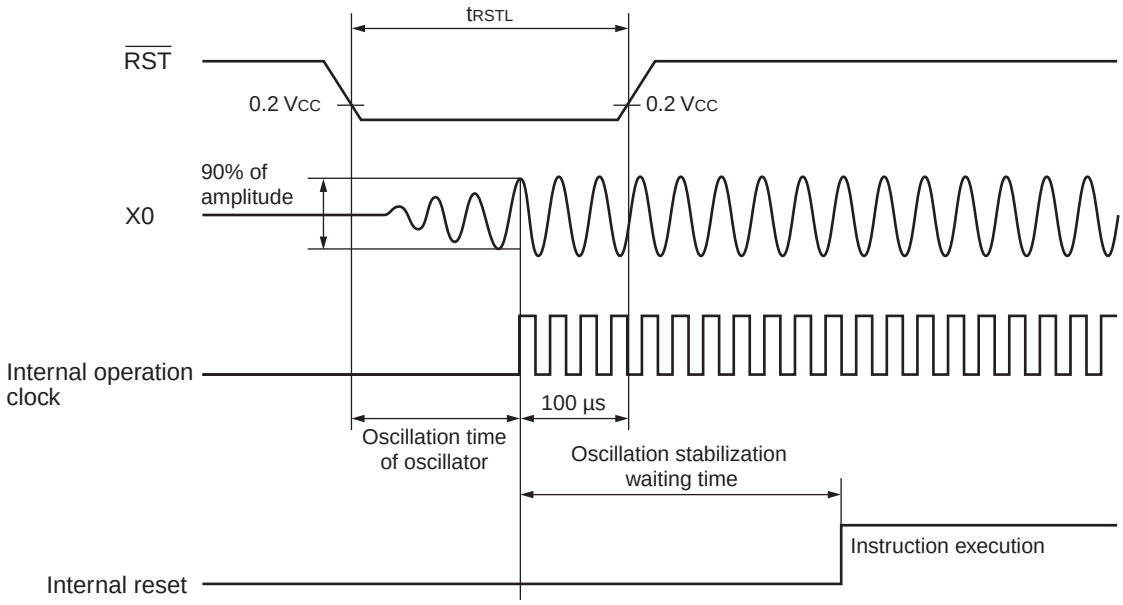
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500		ns	Under normal operation
			Oscillation time of oscillator* + 100 µs		µ s	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100		µ s	In Time Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

€ **Under normal operation:**



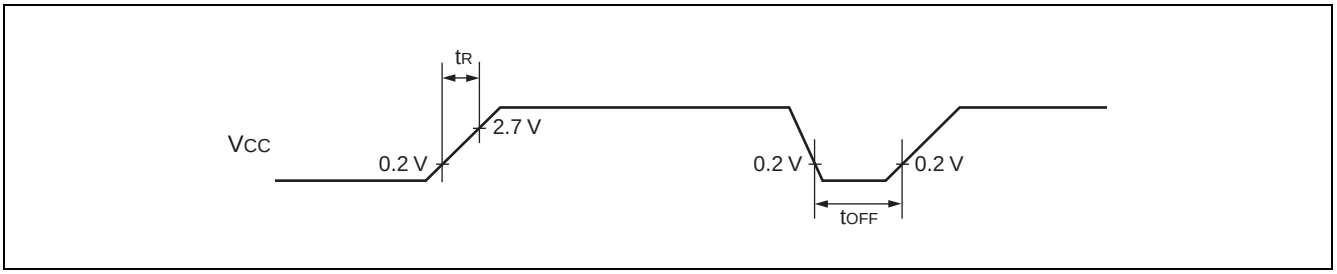
€ **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



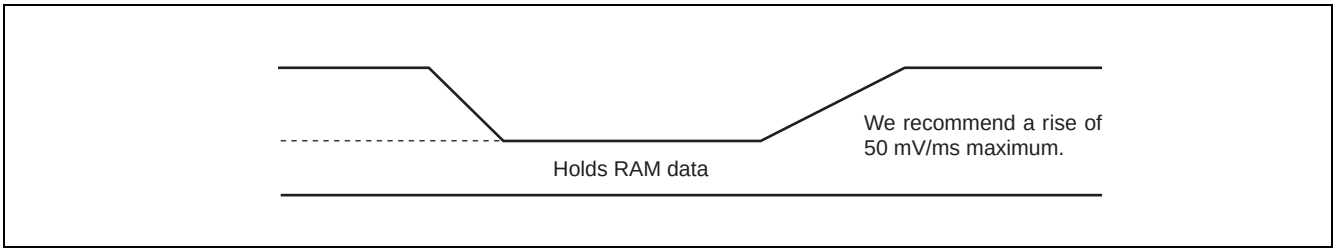
(3) Power On Reset

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}		0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1		ms	Waiting time until power-on



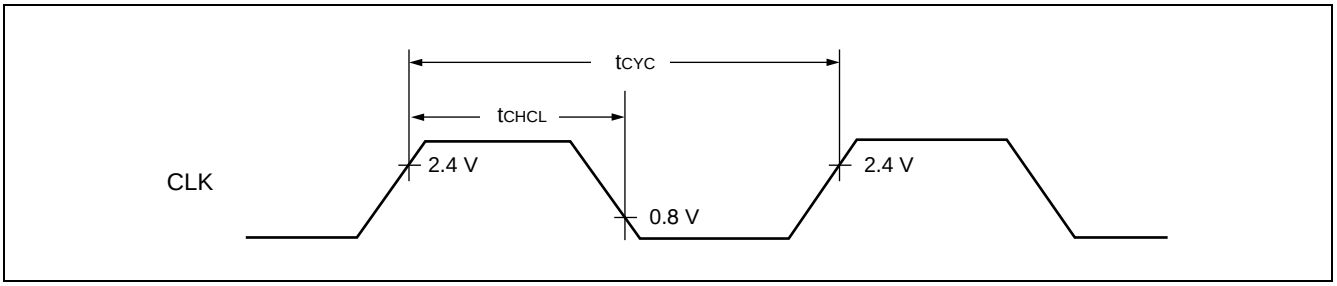
Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



(4) Clock Output Timing

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} 24 MHz)

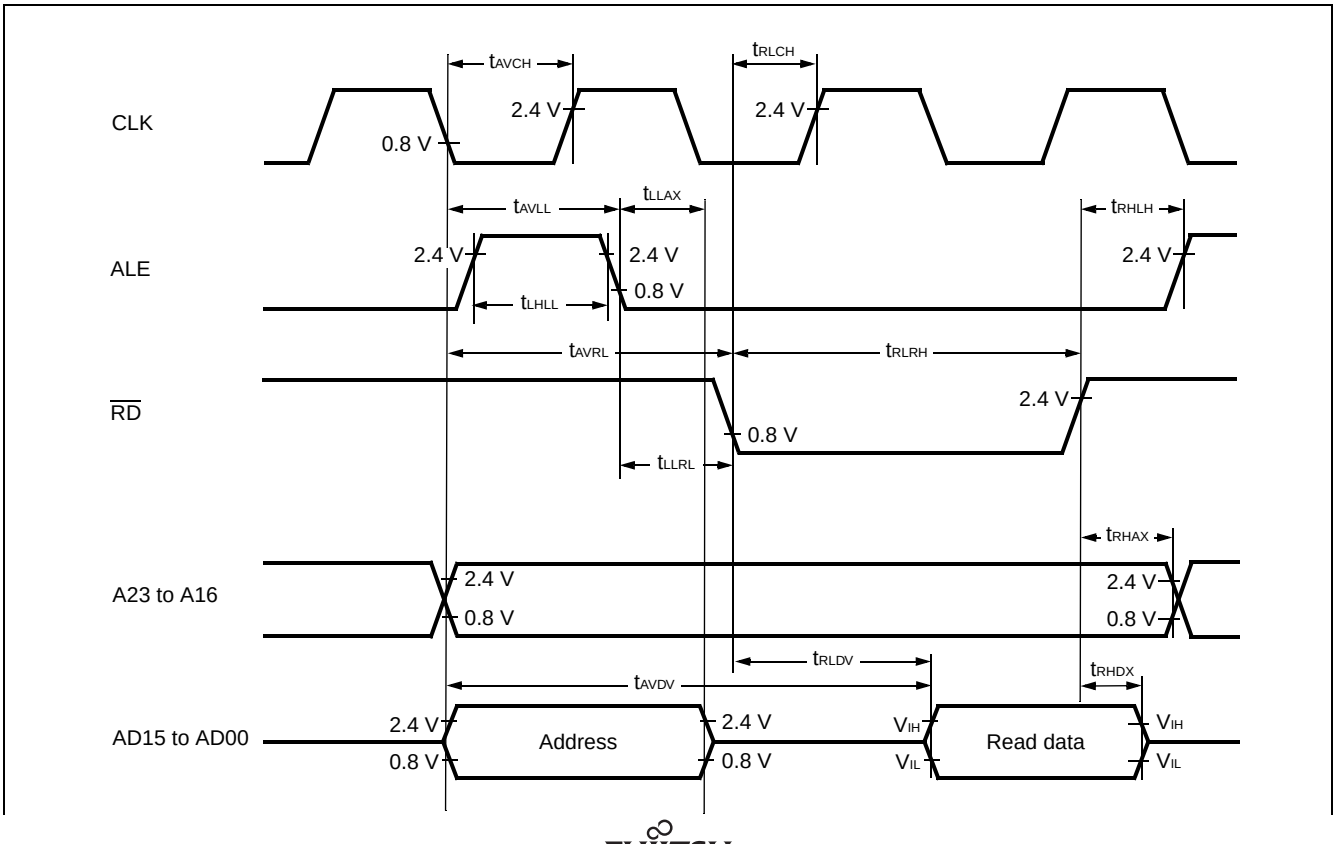
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK		62.5		ns	f_{CP} = 16 MHz
				41.67		ns	f_{CP} = 24 MHz
CLK CLK	t_{CHCL}	CLK		20		ns	f_{CP} = 16 MHz
				13		ns	f_{CP} = 24 MHz



(5) Bus Timing (Read)

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} 24 MHz)

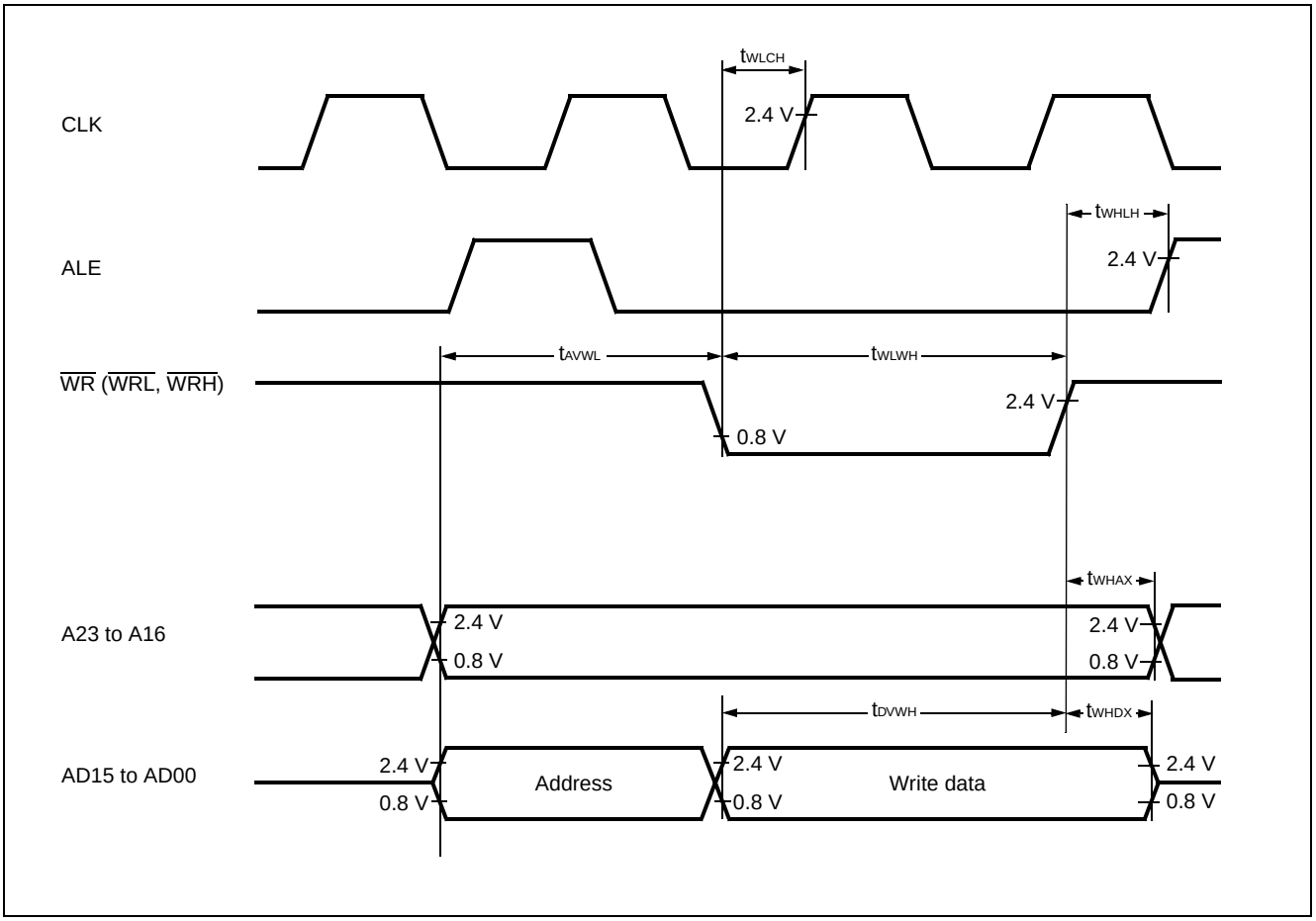
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE		t_{CP}/2 Š 10		ns
Valid address ALE time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		t_{CP}/2 Š 20		ns
ALE Address valid time	t_{LLAX}	ALE, AD15 to AD00		t_{CP}/2 Š 15		ns
Valid address $\overline{RD}$ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$		t_{CP} Š 15		ns
Valid address Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00			5 t_{CP}/2 Š 60	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		3 t_{CP}/2 Š 20		ns
$\overline{RD}$ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00			3 t_{CP}/2 Š 50	ns
$\overline{RD}$ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0		ns
$\overline{RD}$ ALE time	t_{RHLH}	$\overline{RD}$, ALE		t_{CP}/2 Š 15		ns
$\overline{RD}$ Address valid time	t_{RHAX}	$\overline{RD}$, A23 to A16		t_{CP}/2 Š 10		ns
Valid address CLK time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		t_{CP}/2 Š 16		ns
$\overline{RD}$ CLK time	t_{RLCH}	$\overline{RD}$, CLK		t_{CP}/2 Š 15		ns
ALE $\overline{RD}$ time	t_{LLRL}	ALE, $\overline{RD}$		t_{CP}/2 Š 15		ns



(6) Bus Timing (Write)

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\overline{WR}$ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$		t_{CP}Š15		ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 Š 20		ns
Valid data output $\overline{WR}$ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 Š 20		ns
$\overline{WR}$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15		ns
$\overline{WR}$ Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 Š 10		ns
$\overline{WR}$ ALE time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 Š 15		ns
$\overline{WR}$ CLK time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 Š 15		ns

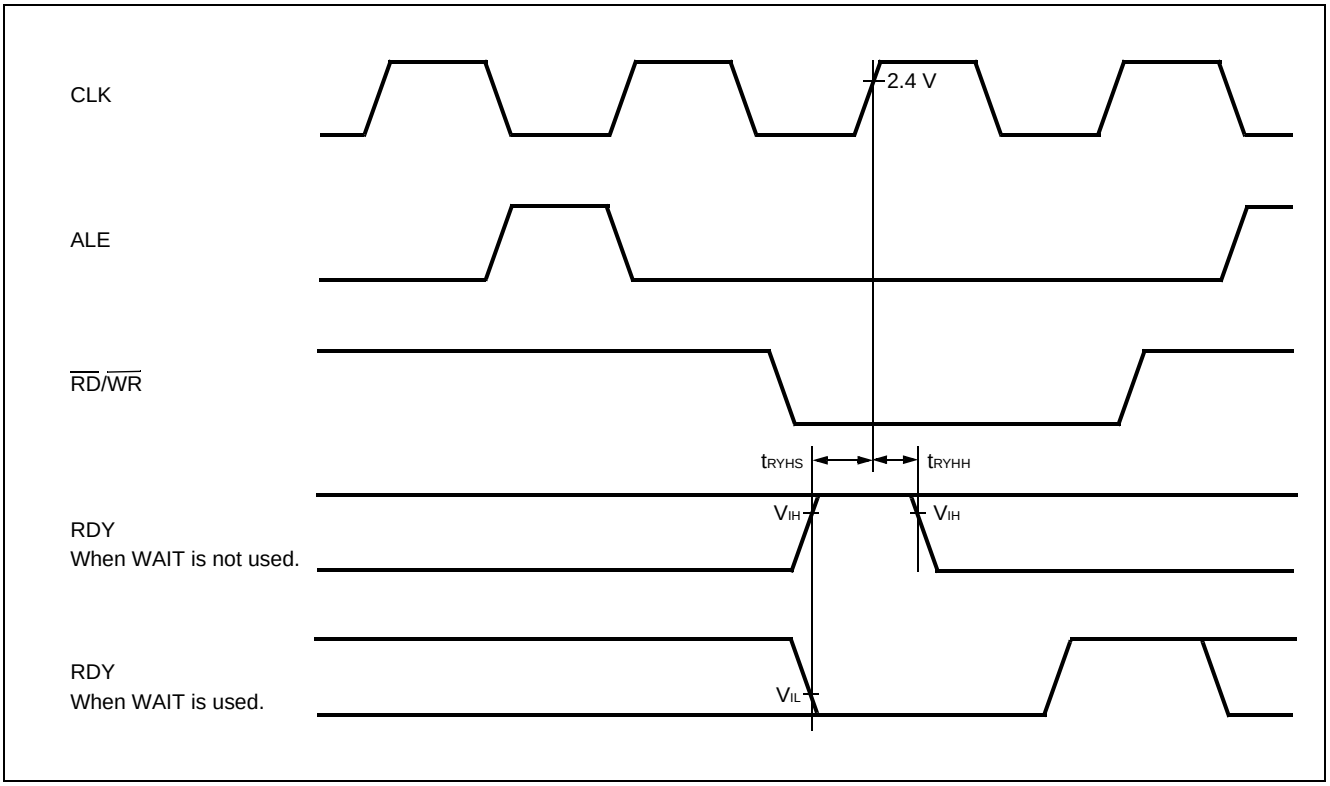


(7) Ready Input Timing

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY		45		ns	f_{CP} = 16 MHz
				32		ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0		ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

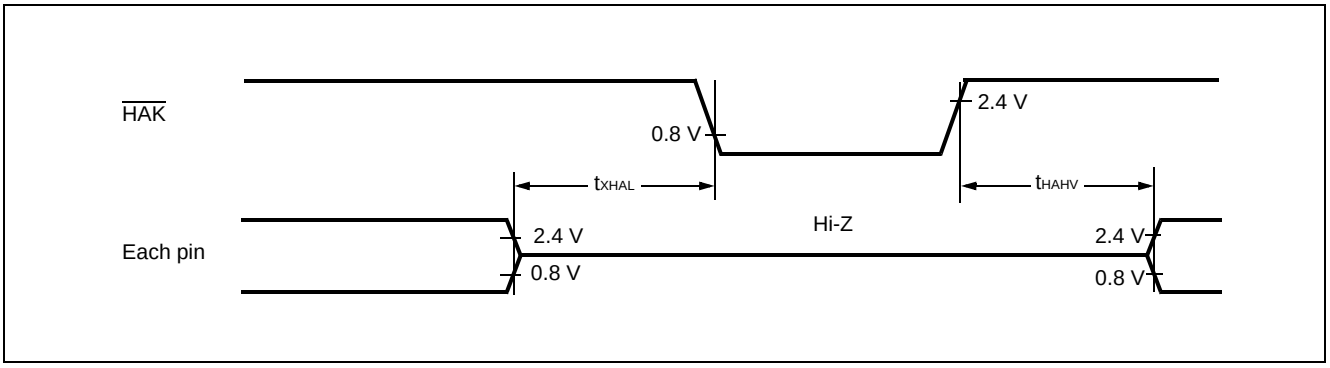


(8) Hold Timing

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating $\overline{HAK}$ time	t_{XHAL}	$\overline{HAK}$		30	t_{CP}	ns
$\overline{HAK}$ time Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.



(9) LIN-UART0/1/2/3

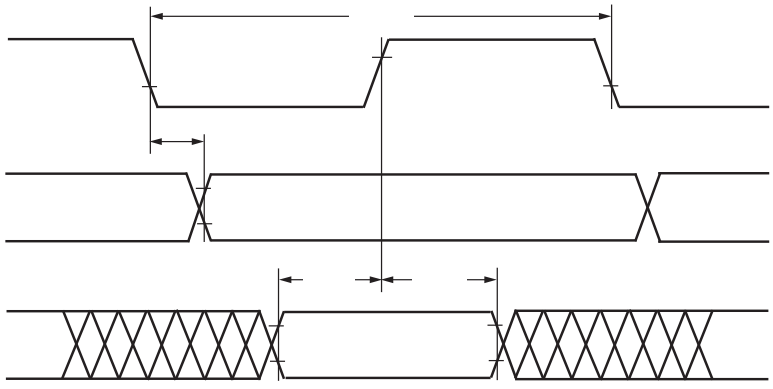
- **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0 V)

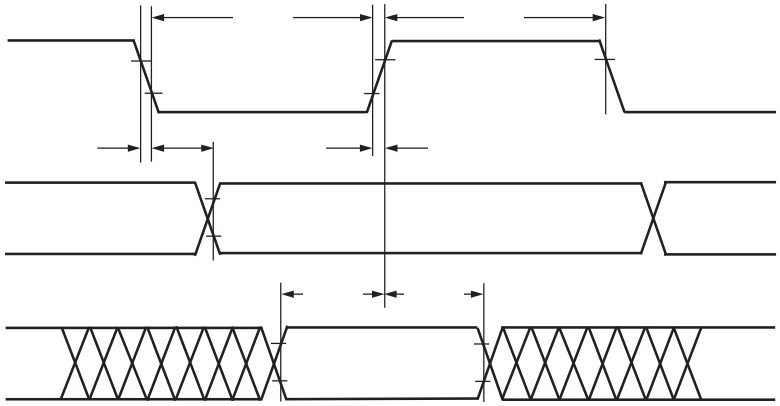
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}		ns
SCK SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		Š50	+50	ns
Valid SIN SCK	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80		ns
SCK Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0		ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R		ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10		ns
SCK SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3			2 t_{CP} + 60	ns
Valid SIN SCK	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30		ns
SCK Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t_{CP} + 30		ns
SCK fall time	t_F	SCK0 to SCK3			10	ns
SCK rise time	t_R	SCK0 to SCK3			10	ns

Notes : € AC characteristic in CLK synchronized mode.
€ C_L is load capacity value of pins when testing.
€ t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

€ Internal Shift Clock Mode



€ External Shift Clock Mode



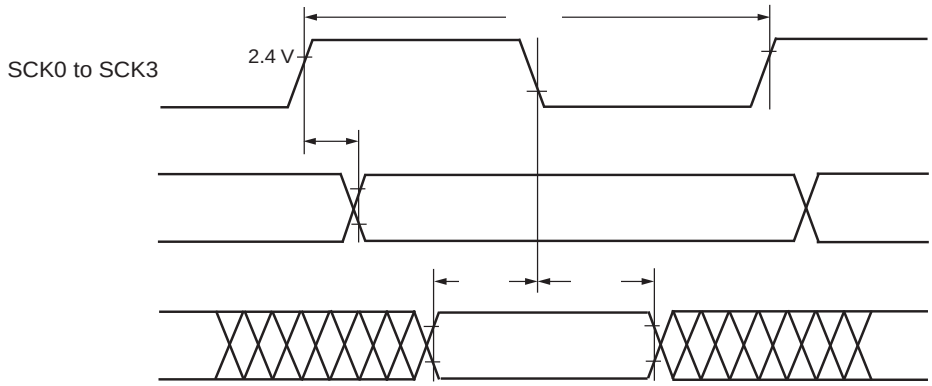
- **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0**

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0 V)

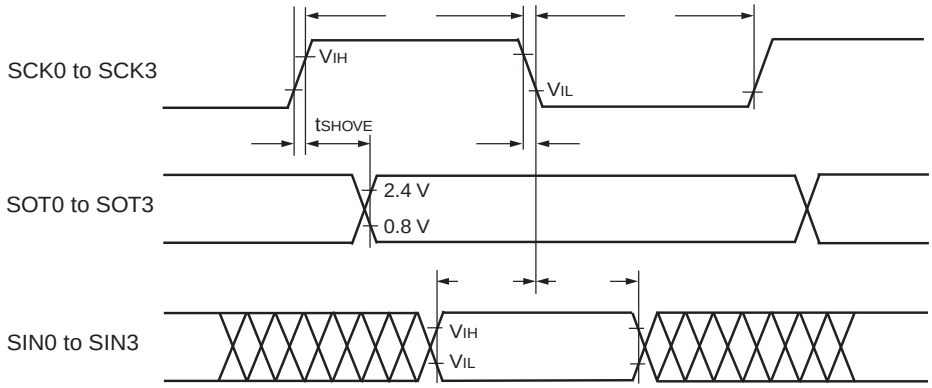
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}		ns
SCK SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		Š50	+50	ns
Valid SIN SCK	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80		ns
SCK Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0		ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R		ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10		ns
SCK SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3			2 t_{CP} + 60	ns
Valid SIN SCK	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30		ns
SCK Valid SIN hold time	t_{SLIXE}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 30		ns
SCK fall time	t_F	SCK0 to SCK3			10	ns
SCK rise time	t_R	SCK0 to SCK3			10	ns

Notes : € C_L is load capacity value of pins when testing.
€ t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

€ Internal Shift Clock Mode



€ External Shift Clock Mode

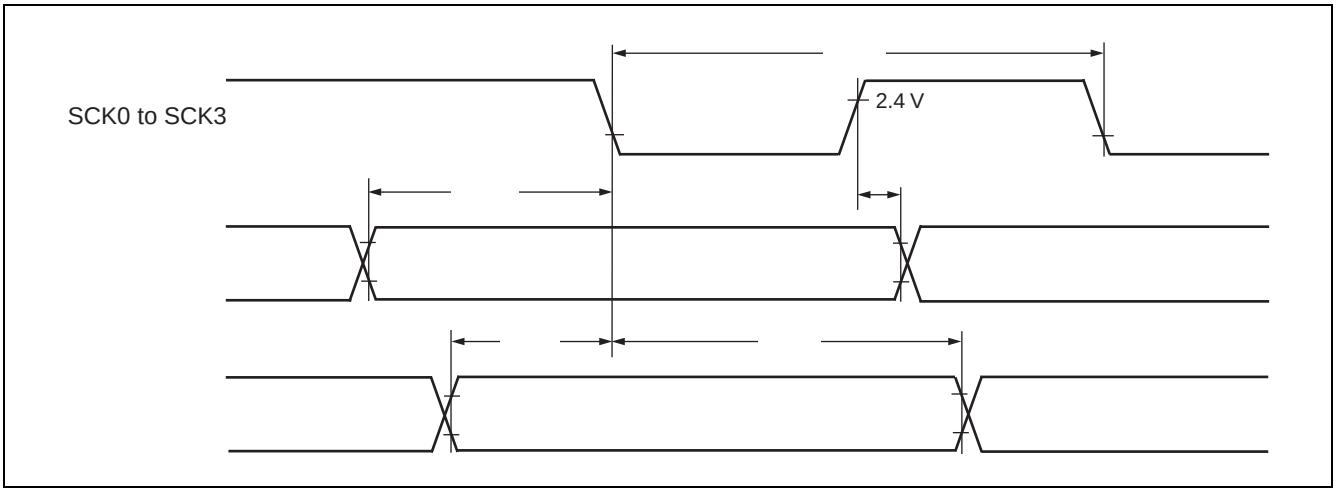


- **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}		ns
SCK SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		Š50	+50	ns
Valid SIN SCK	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80		ns
SCK Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0		ns
SOT SCK delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} Š 70		ns

Notes : € C_L is load capacity value of pins when testing.
€ t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

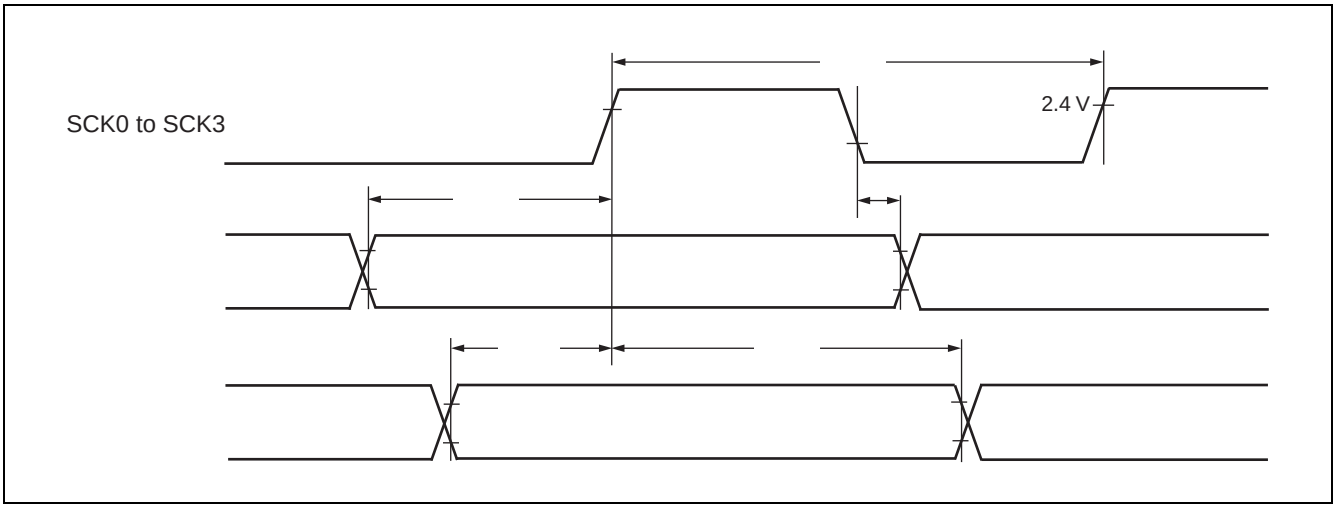


- **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1**

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}		ns
SCK SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		Š50	+50	ns
Valid SIN SCK	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80		ns
SCK Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0		ns
SOT SCK delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} Š 70		ns

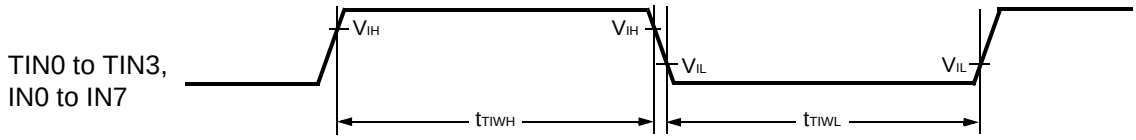
Notes : € C_L is load capacity value of pins when testing.
€ t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



(11) Timer Related Resource Input Timing

(T_A = Š40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0 V)

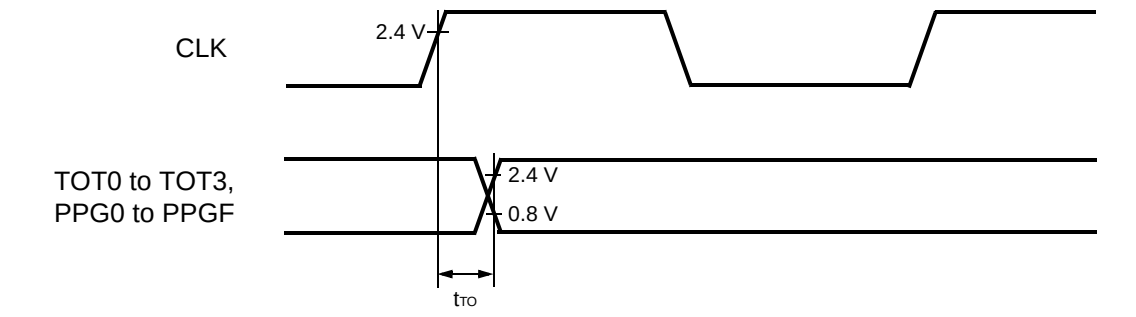
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN0 to TIN3, IN0 to IN7		4 t_{CP}		ns
	t_{TIWL}					



(12) Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF		30		ns



5. A/D Converter

(T_A = Š40 °C to +105 °C, 3.0 V AVRH Š AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution					10	bit	
Total error				±	3.0	LSB	
Nonlinearity error				±	2.5	LSB	
Differential nonlinearity error				±	1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL Š 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH Š 3.5 × LSB	AVRH Š 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time			1.0		16500	µs	4.5 V AV_{CC} 5.5 V
			2.0				4.0 V AV_{CC} < 4.5 V
Sampling time			0.5			µs	4.5 V AV_{CC} 5.5 V
			1.2				4.0 V AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	Š0.3		+ 0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL		AVRH	V	
Reference voltage range		AVRH	AVRL + 2.7		AV_{CC}	V	
		AVRL	0		AVRH Š 2.7	V	
Power supply current	I_A	AV_{CC}		3.5	7.5	mA	
	I_{AH}	AV_{CC}			5	µA	*
Reference voltage current	I_R	AVRH		600	900	µA	
	I_{RH}	AVRH			5	µA	*
Offset between input channels		AN0 to AN23			4	LSB	

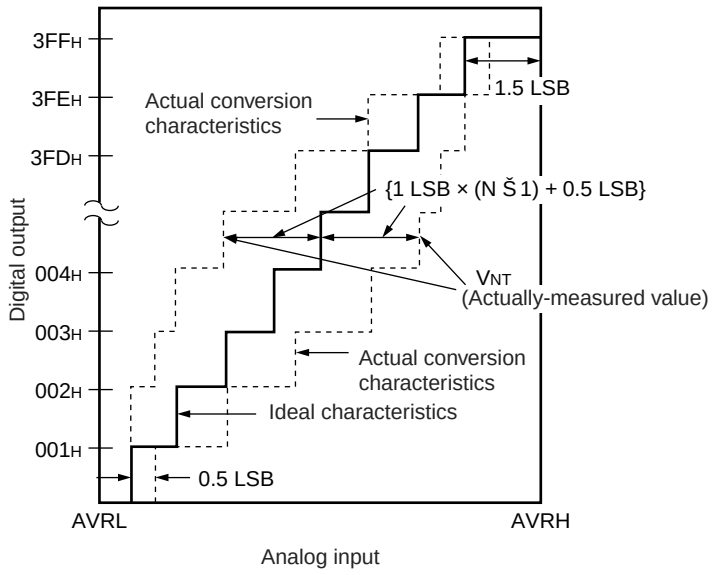
*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Note: The accuracy gets worse as |AVRH Š AVRL| becomes smaller.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by the A/D converter.
Non linearity error	:	The deviation between the actual conversion characteristics and a line that joins the zero-transition line (“00 0000 0000” “00 0000 0001”) to the full-scale transition line (“11 1111 1110” “11 1111 1111”) .
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH Š 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H.

(Continued)

7. Notes on A/D Converter Section

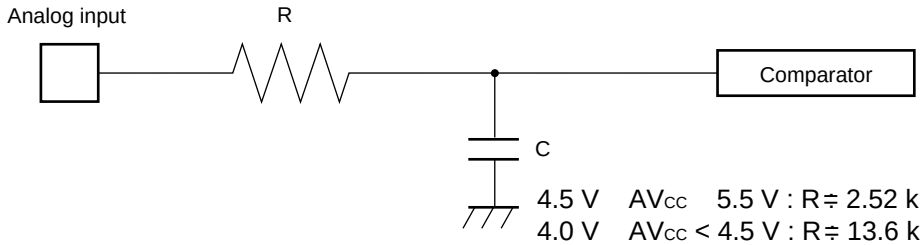
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 k or lower (4.0 V AV_{CC} 5.5 V, sampling period = 0.5 µs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model



4.5 V AV_{CC} 5.5 V : R ≒ 2.52 k , C ≒ 10.7 pF
4.0 V AV_{CC} < 4.5 V : R ≒ 13.6 k , C ≒ 10.7 pF

Note : Use the values in the figure only as a guideline.

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V		1	15	s	Excludes programming prior to erasure
Chip erase time			9		s	Excludes programming prior to erasure
Word (16-bit width) programming time			16	3600	µs	Except for the over head time of the system
Program/Erase cycle		10000			cycle	
Flash Data Retention Time	Average T_A = +85 °C	20			year	*

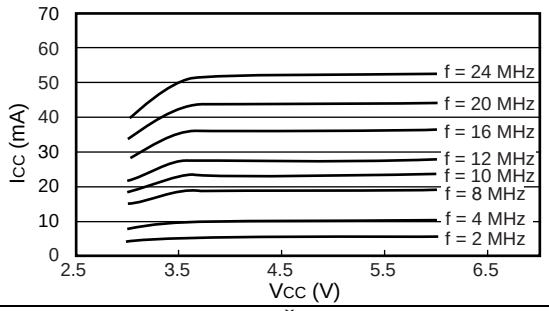
* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ EXAMPLE CHARACTERISTICS

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

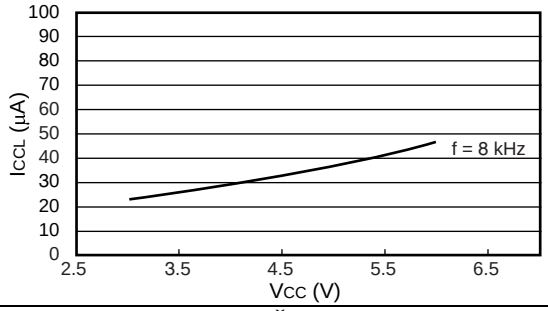
I_{CC} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



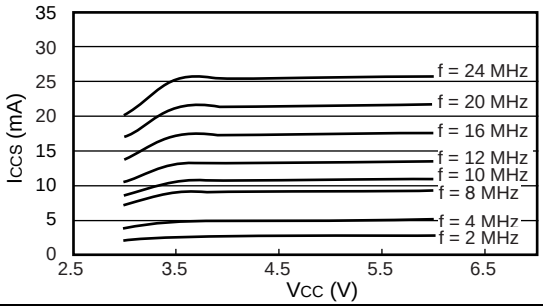
I_{CCL} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



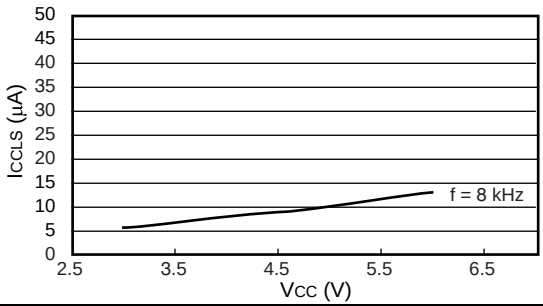
I_{CCS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



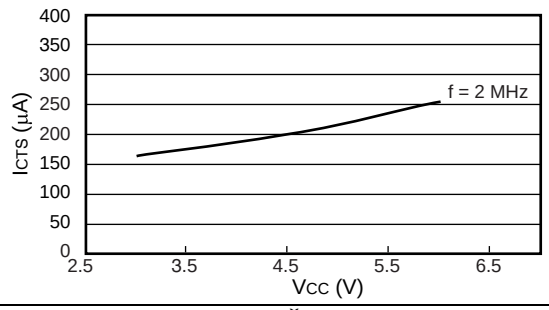
I_{CCLS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



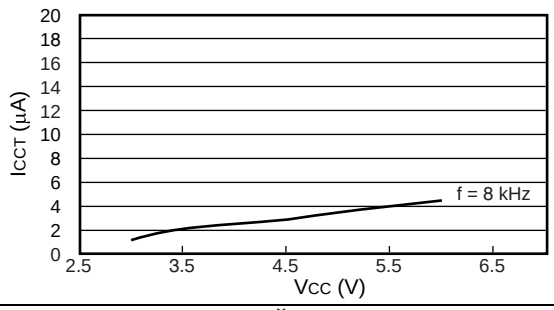
I_{CTS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



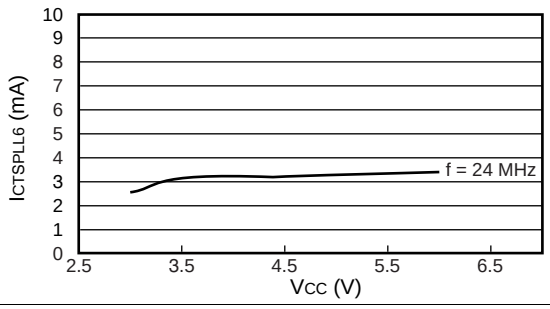
I_{CCT} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



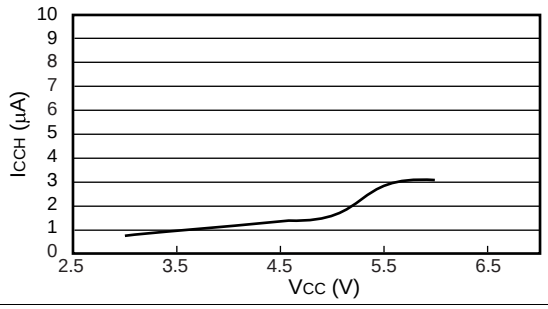
$I_{CTSPLL6}$ – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



I_{CCH} – V_{CC}

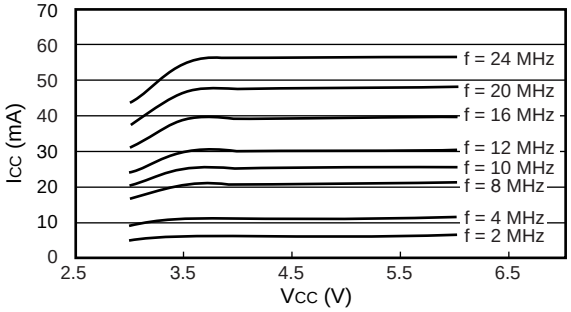
T_A = +25 °C, stopped



- MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES

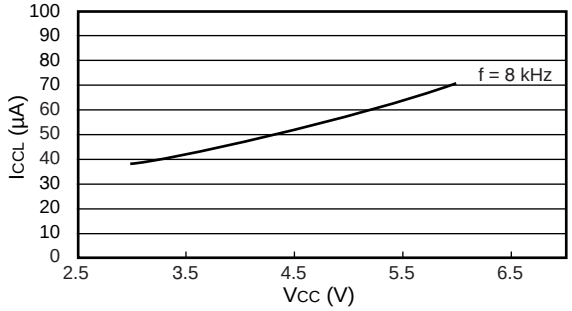
I_{CC} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



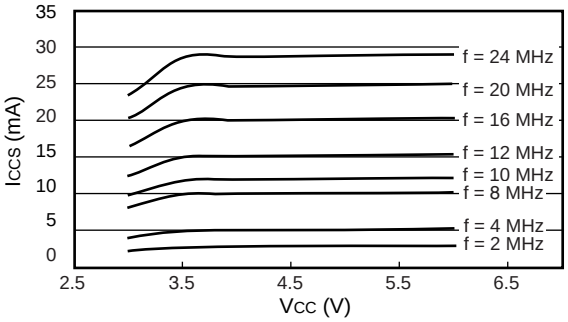
I_{CCL} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



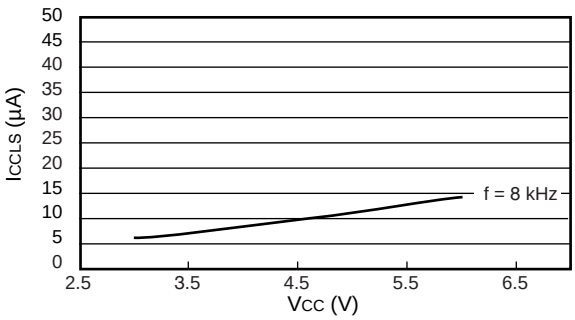
I_{CCS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



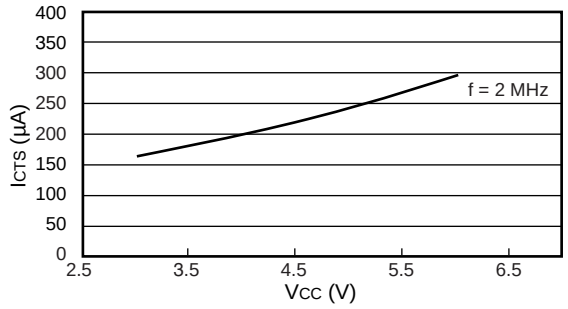
I_{CCLS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



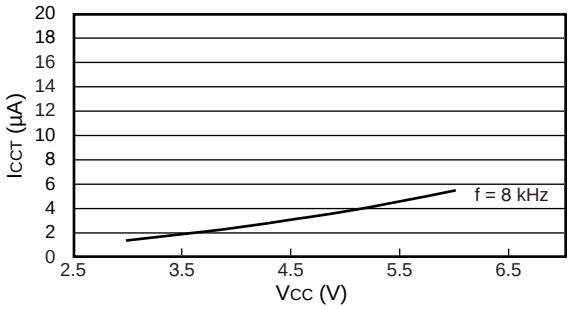
I_{CTS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



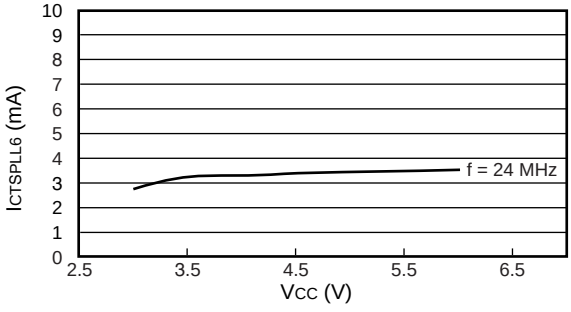
I_{CCT} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



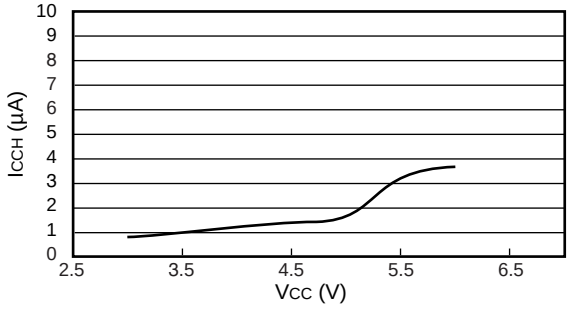
$I_{CTSPLL6}$ – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



I_{CCH} – V_{CC}

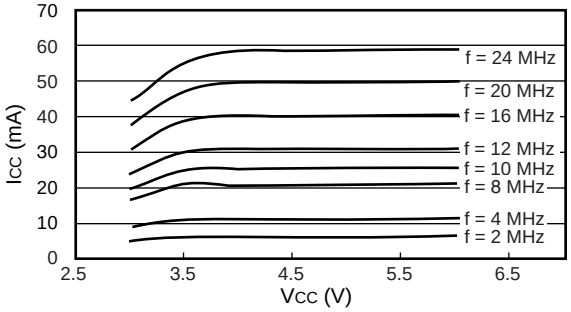
T_A = +25 °C, stopped



- MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

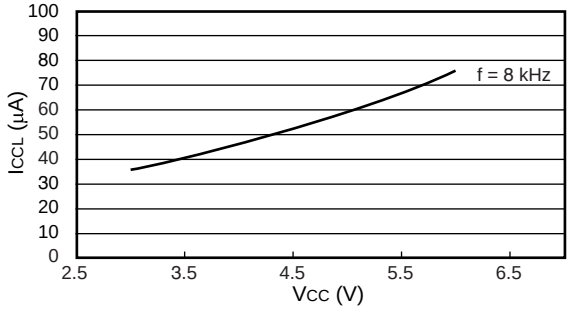
I_{CC} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



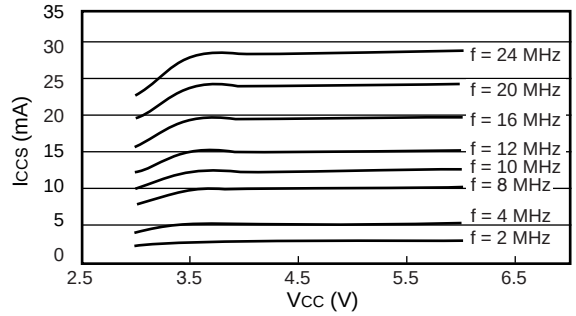
I_{CCL} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



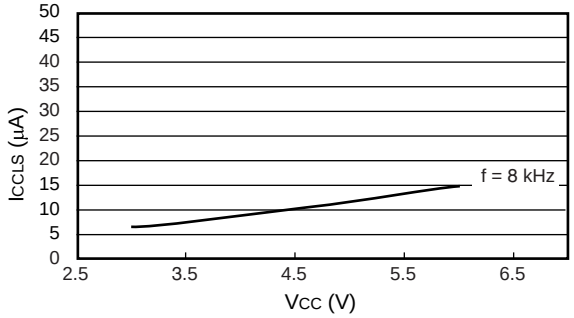
I_{CCS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



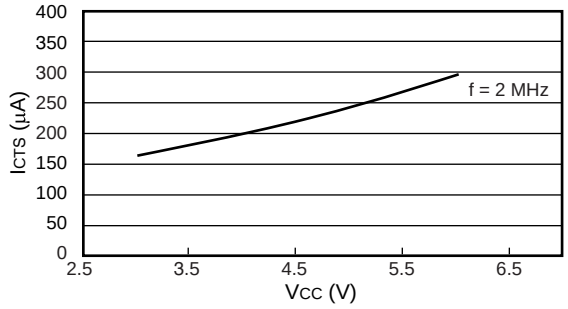
I_{CCLS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



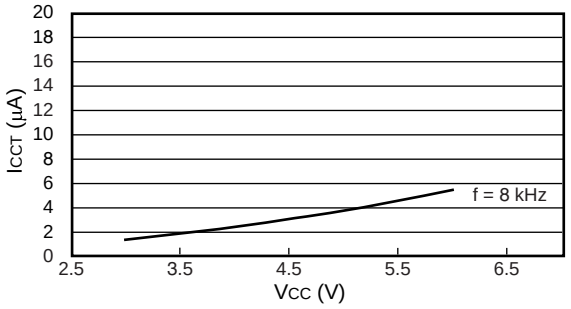
I_{CTS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



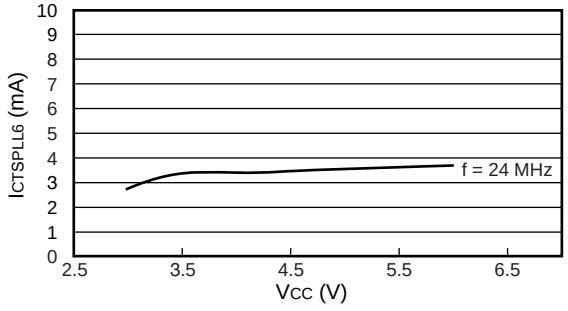
I_{CCT} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



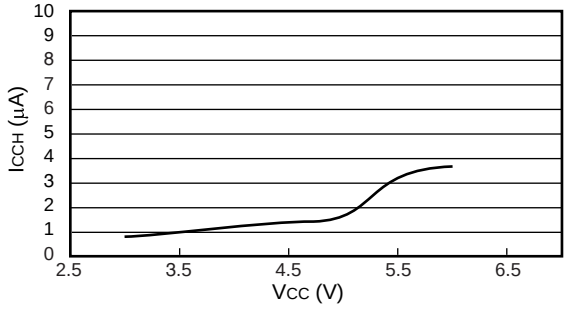
$I_{CTSPLL6}$ – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



I_{CCH} – V_{CC}

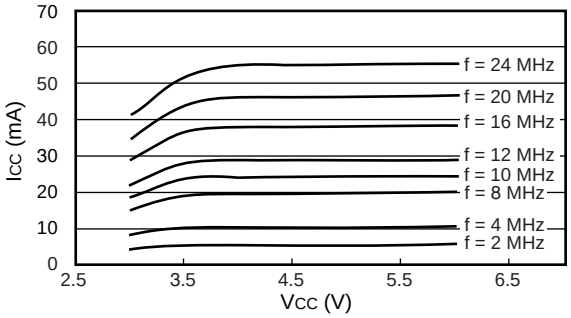
T_A = +25 °C, stopped



- MB90346E, MB90346ES, MB90346CE, MB90346CES

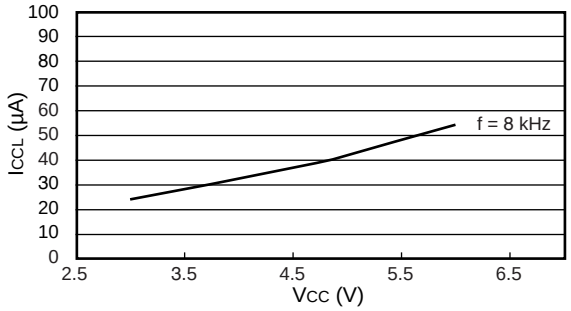
I_{CC} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



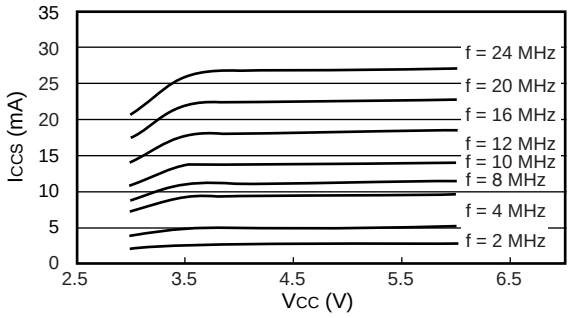
I_{CCL} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



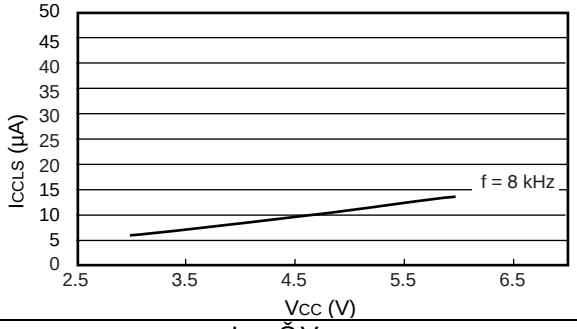
I_{CCS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



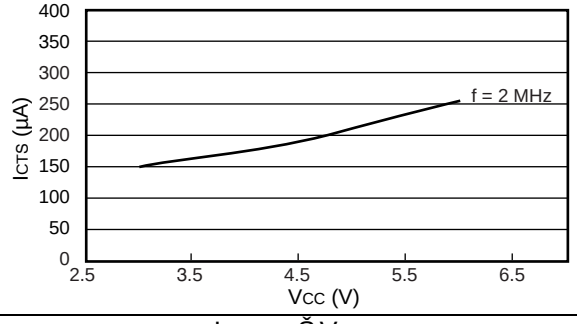
I_{CCLS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



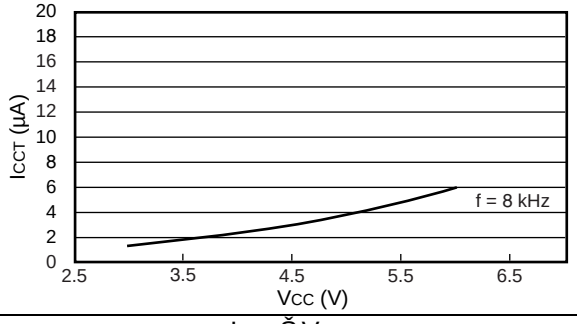
I_{CTS} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



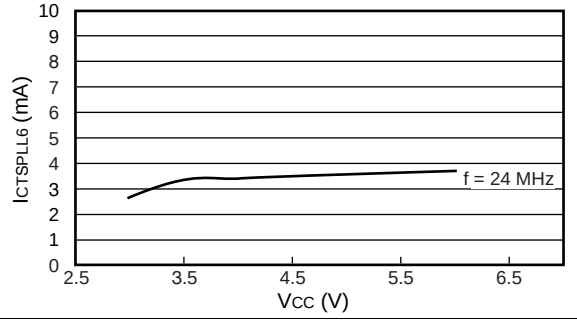
I_{CCT} – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



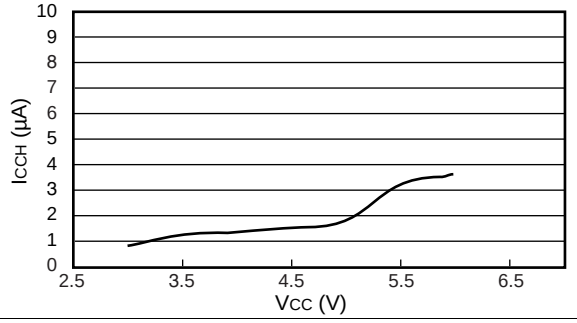
$I_{CTSPLL6}$ – V_{CC}

T_A = +25 °C, external clock operation
f = Internal operation frequency



I_{CCH} – V_{CC}

T_A = +25 °C, stopped



■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

(Continued)

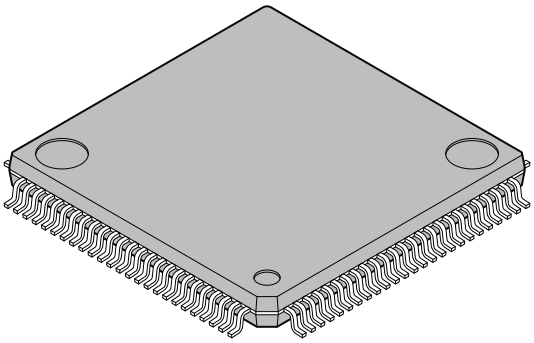
Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

(Continued)

(Continued)

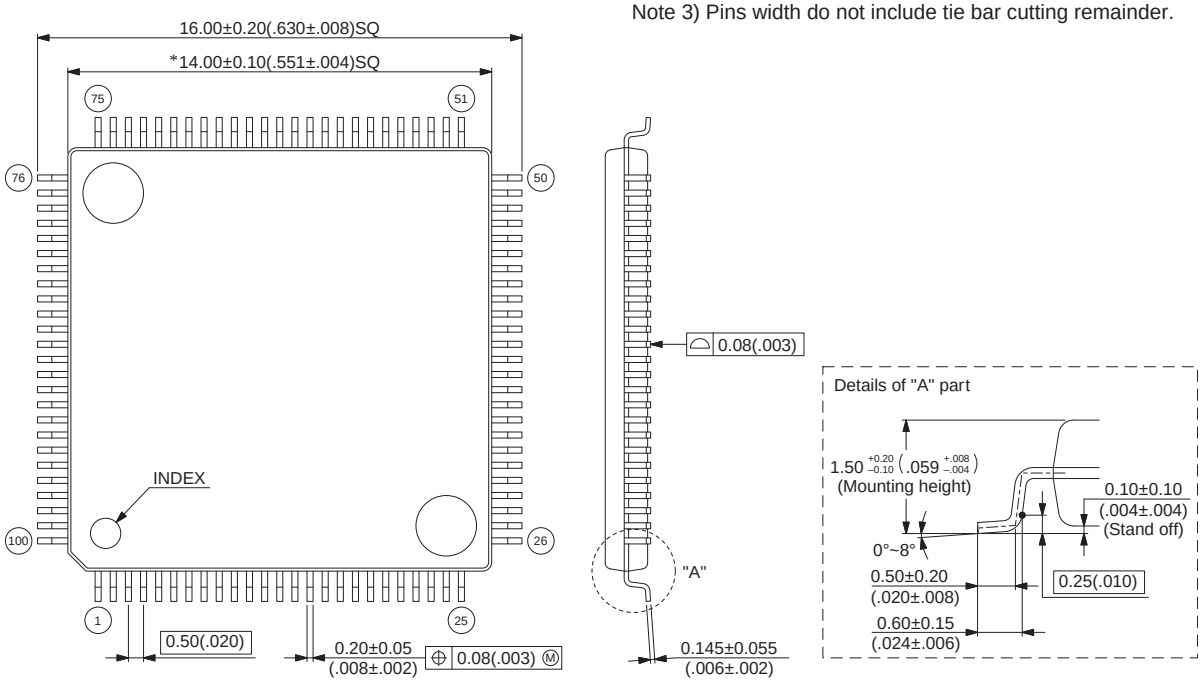
Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		

■ PACKAGE DIMENSIONS

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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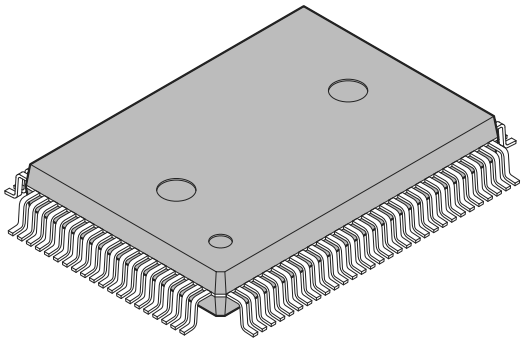
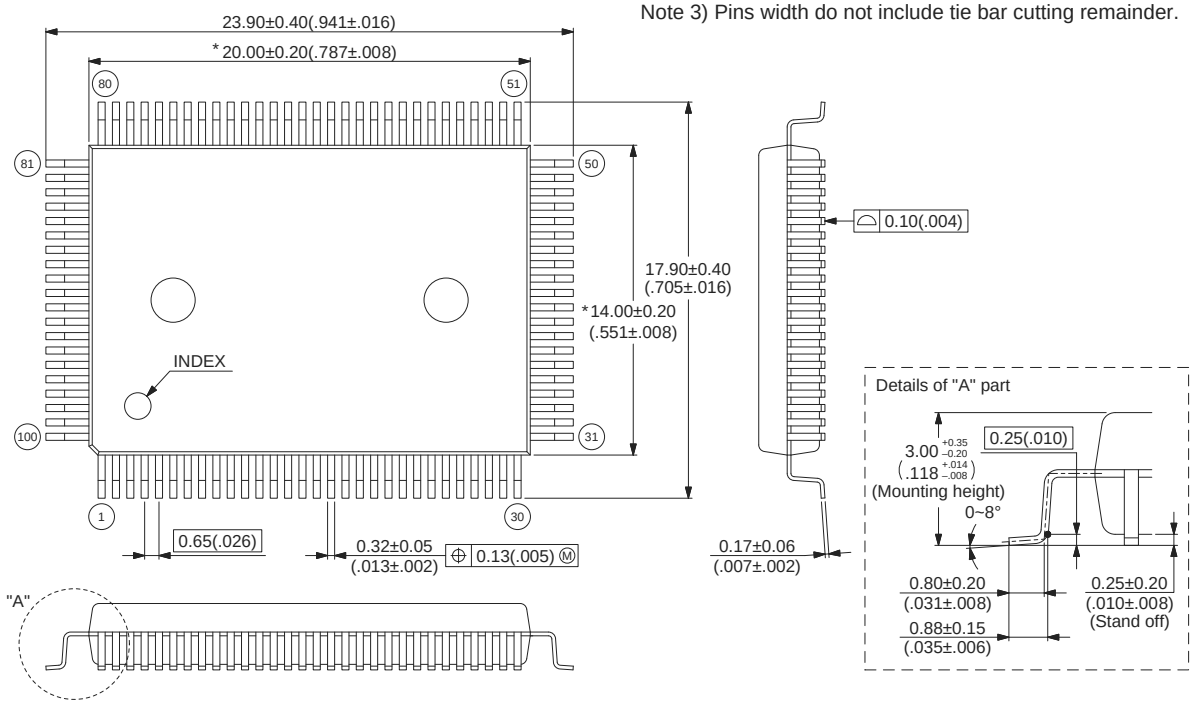
100-pin plastic QFP		
 (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
		Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Added “*6” in remark for “L" level maximum output current and “H” level maximum output current. Added “*7” in remark for “L" level average output current and “H” level average output current. Added “*8” in remark for “L"level average overall output current and “H” level average overall output current.
52		Added as follows. “*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

The vertical lines marked in the left side of the page show the changes.

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