Voltage Supervisor with 8-Kb and 16-Kb SPI Serial CMOS EEPROM

HALOGEN FREE LEAD FREE™ RoHS Compliance

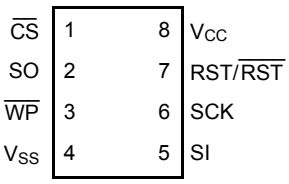
FEATURES

- **Precision Power Supply Voltage Monitor**
  - **5V, 3.3V, 3V & 2.5V systems**
  - **7 threshold voltage options**
- **Active High or Low Reset**
  - **Valid reset guaranteed at V_{CC} = 1V**
- **10MHz SPI compatible**
- **32-byte page write buffer**
- **Low power CMOS technology**
- **1,000,000 Program/Erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-pin SOIC package**

For Ordering Information details, see page 14.

PIN CONFIGURATION

SOIC (W)



PIN FUNCTION

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
RST/$\overline{RST}$	Reset Output
V_{CC}	Power Supply

DESCRIPTION

The CAT15008/16 (see table below) are memory and supervisory solutions for microcontroller based systems. A CMOS serial EEPROM memory and a system power supervisor with brown-out protection are integrated together. Memory interface is via SPI bus serial interface.

The CAT15008/16 provides a precision V_{CC} sense circuit with two reset output options: CMOS active low output or CMOS active high. The RESET output is active whenever V_{CC} is below the reset threshold or falls below the reset threshold voltage.

The power supply monitor and reset circuit protect system controllers during power up/down and against brownout conditions. Seven reset threshold voltages support 5V, 3.3V, 3V and 2.5V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 240ms after the supply voltage exceeds the reset threshold level.

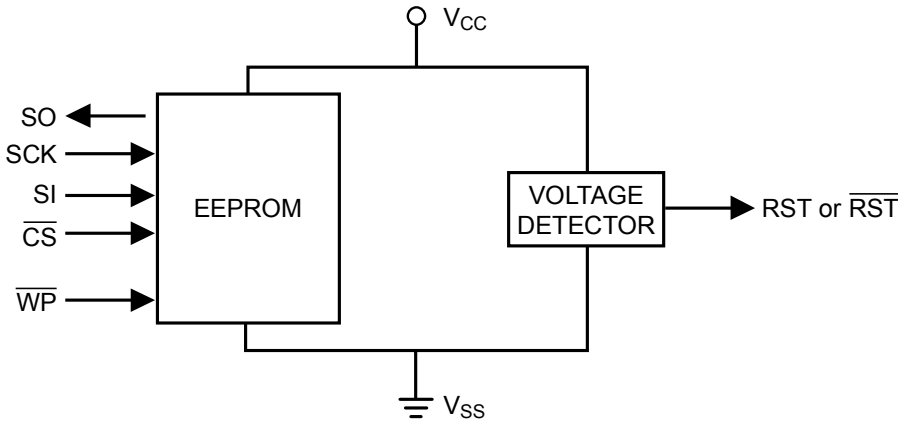
MEMORY SIZE SELECTOR

Product	Memory density
15008	8-Kbit
15016	16-Kbit

THRESHOLD SUFFIX SELECTOR

Nominal Threshold Voltage	Threshold Suffix Designation
4.63V	L
4.38V	M
4.00V	J
3.08V	T
2.93V	S
2.63V	R
2.32V	Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground[2]	-0.5 to +6.5	V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
NEND[4]	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +5.5V unless otherwise specified.

Symbol	Parameter	Limits			Test Condition	Units
		Min.	Typ.	Max.		
I_{CC}	Supply Current			2	Read or Write at 10MHz, SO open	mA
I_{SB}	Standby Current		12	25	V_{CC} < 5.5V; V_{IN} = V_{SS} or V_{CC}, $\overline{CS}$ = V_{CC}	µA
			10	20	V_{CC} < 3.6V; V_{IN} = V_{SS} or V_{CC}, $\overline{CS}$ = V_{CC}	
I_L	I/O Pin Leakage			2	Pin at GND or V_{CC}	µA
V_{IL}	Input Low Voltage	-0.5		0.3 V_{CC}		V
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5		V
V_{OL}	Output Low Voltage			0.4	V_{CC} ≥ 2.5V, I_{OL} = 3.0mA	V
V_{OH}	Output High Voltage	V_{CC} - 0.8			V_{CC} ≥ 2.5V, I_{OH} = -1.6mA	V

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5V or higher than V_{CC} + 0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than V_{CC} + 1.5V, for periods of less than 20ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5V, 25°C

A.C. CHARACTERISTICS (MEMORY)[1]

V_{CC} = 2.5V to 5.5V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	DC	10	MHz
t_{SU}	Data Setup Time	20		ns
t_H	Data Hold Time	20		ns
t_{WH}	SCK High Time	40		ns
t_{WL}	SCK Low Time	40		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		25	ns
t_{RI}[2]	Input Rise Time		2	µs
t_{FI}[2]	Input Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		ns
t_V	Output Valid from Clock Low		40	ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		25	ns
t_{CS}	$\overline{CS}$ High Time	15		ns
t_{CSS}	$\overline{CS}$ Setup Time	15		ns
t_{CSH}	$\overline{CS}$ Hold Time	15		ns
t_{WPS}	$\overline{WP}$ Setup Time	10		ns
t_{WPH}	$\overline{WP}$ Hold Time	10		ns
t_{WC}[4]	Write Cycle Time		5	ms
t_{PU}[2] [3]	Power-up to Ready Mode		1	ms

Notes:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this parameter.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Levels	0.3 V_{CC} to 0.7 V_{CC}
Timing Reference Levels	0.5 V_{CC}
Output Load	Current Source: I_{OL} max/ I_{OH} max; C_L = 50pF

ELECTRICAL CHARACTERISTICS (SUPERVISORY FUNCTION)

V_{CC} = Full range, T_A = -40ºC to +85ºC unless otherwise noted. Typical values at T_A = +25ºC and V_{CC} = 5V for L/M/J versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version and V_{CC} = 2.5V for Z version.

Symbol	Parameter	Threshold	Conditions	Min	Typ	Max	Units
V_{TH}	Reset Threshold Voltage	L	T_A = +25ºC	4.56	4.63	4.70	V
			T_A = -40ºC to +85ºC	4.50		4.75	
		M	T_A = +25ºC	4.31	4.38	4.45	
			T_A = -40ºC to +85ºC	4.25		4.50	
		J	T_A = +25ºC	3.93	4.00	4.06	
			T_A = -40ºC to +85ºC	3.89		4.10	
		T	T_A = +25ºC	3.04	3.08	3.11	
			T_A = -40ºC to +85ºC	3.00		3.15	
		S	T_A = +25ºC	2.89	2.93	2.96	
			T_A = -40ºC to +85ºC	2.85		3.00	
		R	T_A = +25ºC	2.59	2.63	2.66	
			T_A = -40ºC to +85ºC	2.55		2.70	
		Z	T_A = +25ºC	2.28	2.32	2.35	
			T_A = -40ºC to +85ºC	2.25		2.38	

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
	Reset Threshold Tempco			30		ppm/ºC
t_{RPD}	V_{CC} to Reset Delay[2]	V_{CC} = V_{TH} to (V_{TH} -100mV)		20		µs
t_{PURST}	Reset Active Timeout Period	T_A = -40ºC to +85ºC	140	240	460	ms
V_{OL}	$\overline{\text{RESET}}$ Output Voltage Low (Push-pull, active LOW, CAT150xx9)	V_{CC} = V_{TH} min, I_{SINK} = 1.2mA R/S/T/Z			0.3	V
		V_{CC} = V_{TH} min, I_{SINK} = 3.2mA J/L/M			0.4	
		V_{CC} > 1.0V, I_{SINK} = 50µA			0.3	
V_{OH}	$\overline{\text{RESET}}$ Output Voltage High (Push-pull, active LOW, CAT150xx9)	V_{CC} = V_{TH} max, I_{SOURCE} = -500µA R/S/T/Z	0.8V_{CC}			V
		V_{CC} = V_{TH} max, I_{SOURCE} = -800µA J/L/M	V_{CC} - 1.5			
V_{OL}	RESET Output Voltage Low (Push-pull, active HIGH, CAT150xx1)	V_{CC} > V_{TH} max, I_{SINK} = 1.2mA R/S/T/Z			0.3	V
		V_{CC} > V_{TH} max, I_{SINK} = 3.2mA J/L/M			0.4	
V_{OH}	RESET Output Voltage High (Push-pull, active HIGH, CAT150xx1)	1.8V < V_{CC} ≤ V_{TH} min, I_{SOURCE} = -150µA	0.8V_{CC}			V

Notes:

(1) Production testing done at T_A = +25ºC; limits over temperature guaranteed by design only.

(2) $\overline{\text{RESET}}$ output for the CAT150xx9; RESET output for the CAT150xx1.

PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: Reset output is available in two versions: CMOS Active Low (CAT150xx9) and CMOS Active High (CAT150xx1). Both versions are push-pull outputs for high efficiency.

SI: The serial data input pin accepts op-codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT15008/16.

$\overline{\text{CS}}$: The chip select input pin is used to enable/disable the CAT15008/16. When $\overline{\text{CS}}$ is high, the SO output is tri-stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). *Every communication session between host and CAT15008/16 must be preceded by a high to low transition and concluded with a low to high transition of the $\overline{\text{CS}}$ input.*

$\overline{\text{WP}}$: The write protect input pin will allow all write operations to the device when held high. When $\overline{\text{WP}}$ pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to "1", writing to the Status Register is disabled.

DEVICE OPERATION

The CAT15008/16 products combine the accurate voltage monitoring capabilities of a standalone voltage supervisor with the high quality and reliability of standard EEPROMs from Catalyst Semiconductor.

RESET CONTROLLER DESCRIPTION

The reset signal is asserted LOW for the CAT150xx9 and HIGH for the CAT150xx1 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140ms (t_{PURST}) after the power supply voltage has risen above the threshold. Reset output timing is shown in Figure 1.

The CAT15008/16 devices protect µPs against brown-out failure. Short duration V_{CC} transients of 4µsec or less and 100mV amplitude typically do not generate a Reset pulse.

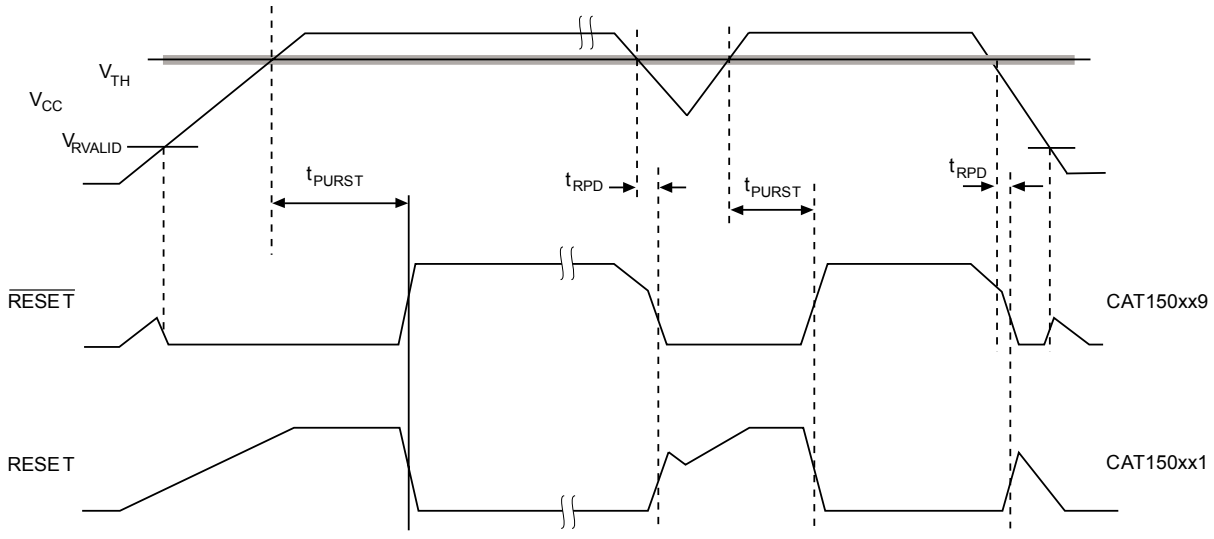


Figure 1. RESET Output Timing

Figure 2 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing V_{TH} - V_{CC}), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5V above the threshold and drops below it by the amplitude of the overdrive voltage (V_{TH} - V_{CC}).

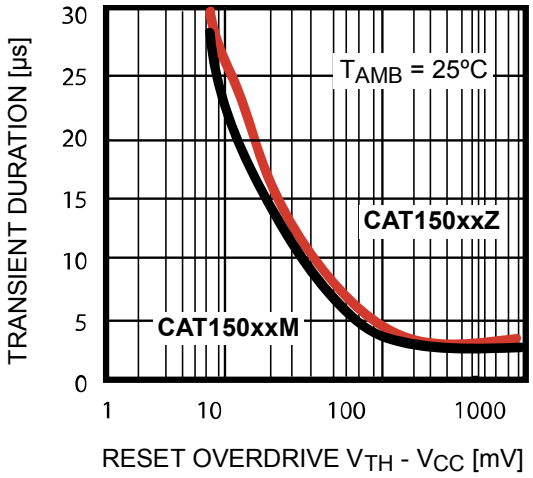


Figure 2. Maximum Transient Duration without Causing a Reset Pulse vs. Overdrive Voltage

EMBEDDED EEPROM DESCRIPTION

The CAT15008/16 devices support the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 1.

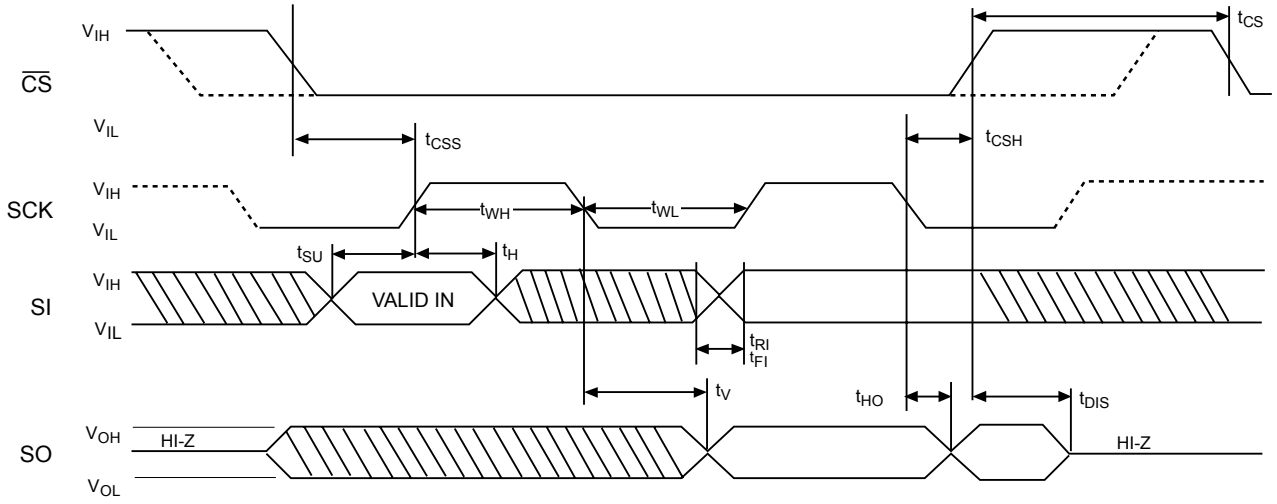
Reading data stored in the CAT15008/16 is accom–plished by simply providing the READ command and an address. Writing to the CAT15008/16, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the CAT15008/16 will accept any one of the six instruction op-codes listed in Table 1 and will ignore all other possible 8-bit combinations. The communication protocol follows the timing from Figure 3.

Table 1: Instruction Set

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

Figure 3. Synchronous Data Timing



Note: Dashed Line = mode (1, 1) - - - - - -

STATUS REGISTER

The Status Register, as shown in Table 2, contains a number of status and control bits.

The $\overline{RDY}$ (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non-volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 3. The protected blocks then become read-only.

The WPEN (Write Protect Enable) bit acts as an enable for the $\overline{WP}$ pin. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the $\overline{WP}$ pin is high or the WPEN bit is 0. The WPEN bit, $\overline{WP}$ pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 4.

Table 2. Status Register

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	$\overline{RDY}$

Table 3. Block Protection Bits

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	15008: 0300-03FF	Quarter Array Protection
		15016: 0600-07FF	
1	0	15008: 0200-03FF	Half Array Protection
		15016: 0400-07FF	
1	1	15008: 0000-03FF	Full Array Protection
		15016: 0000-07FF	

Table 4. Write Protect Enable Operation

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

WRITE OPERATIONS

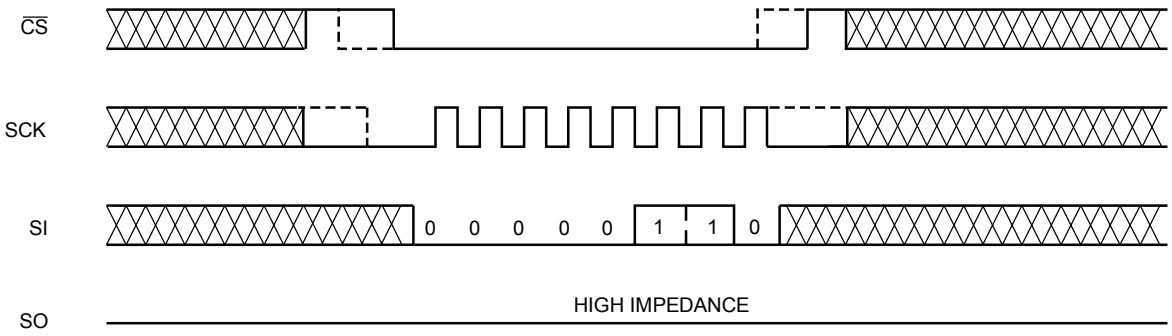
The CAT15008/16 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the CAT15008/16. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 4. The WREN instruction must be sent prior any WRITE or WRSR instruction.

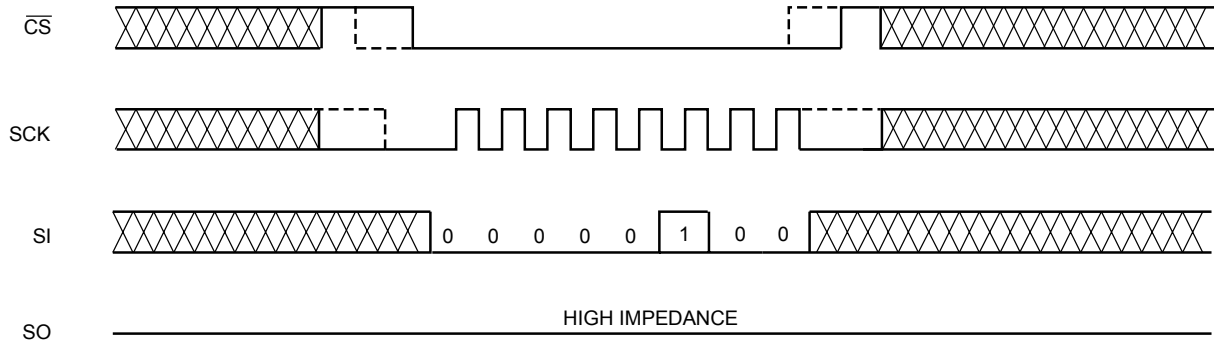
The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 5. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

Figure 4. WREN Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Figure 5. WRDI Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16-bit address and data as shown in Figure 6. Only 10 significant address bits are used by the CAT15008 and 11 by the CAT15016. The rest are don't care bits, as shown in Table 5. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the the device is ready to accept commands ($\overline{RDY}$ low).

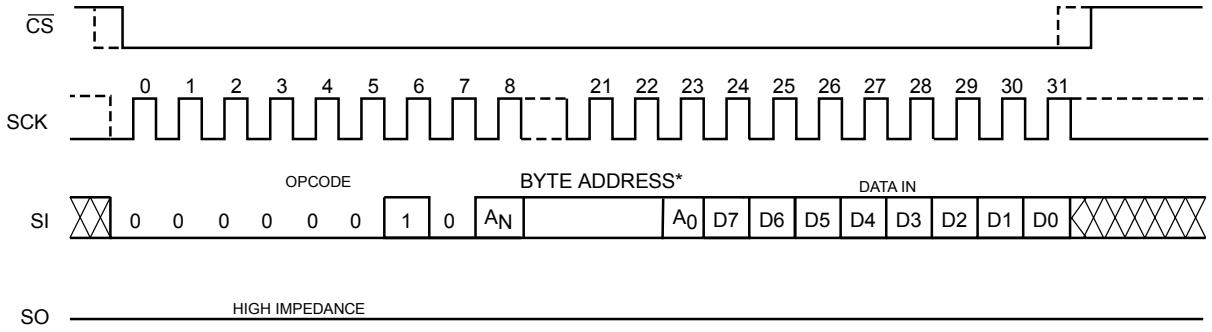
Page Write

After sending the first data byte to the CAT15008/16, the host may continue sending data, up to a total of 32 bytes, according to timing shown in Figure 7. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previoualy loaded data. Following completion of the write cycle, the CAT15008/16 is automatically returned to the write disable state.

Table 5. Byte Address

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulse
CAT15008	A9 - A0	A15 - A10	16
CAT15016	A10 - A0	A15 - A11	16

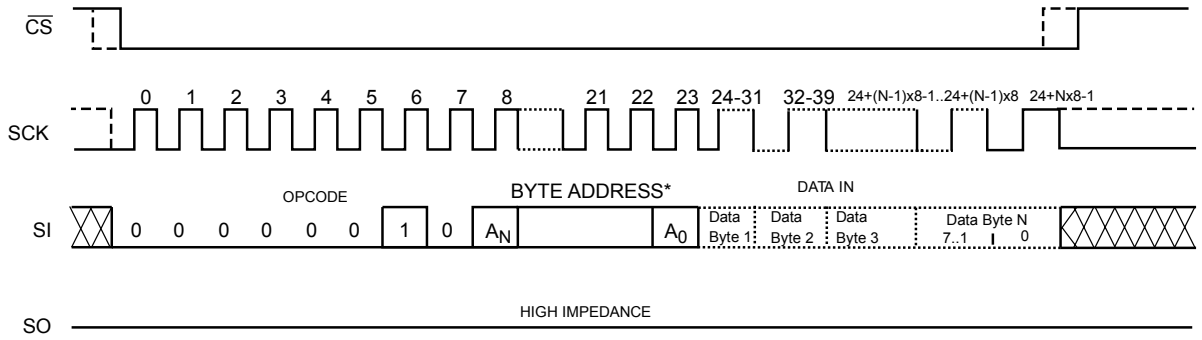
Figure 6. Byte WRITE Timing



* Please check the Byte Address Table (Table 5)

Note: Dashed Line = mode (1, 1) - - - - - -

Figure 7. Page WRITE Timing



*Please check the Byte Address Table. (Table 5)

Note: Dashed Line = mode (1, 1) - - - - - -

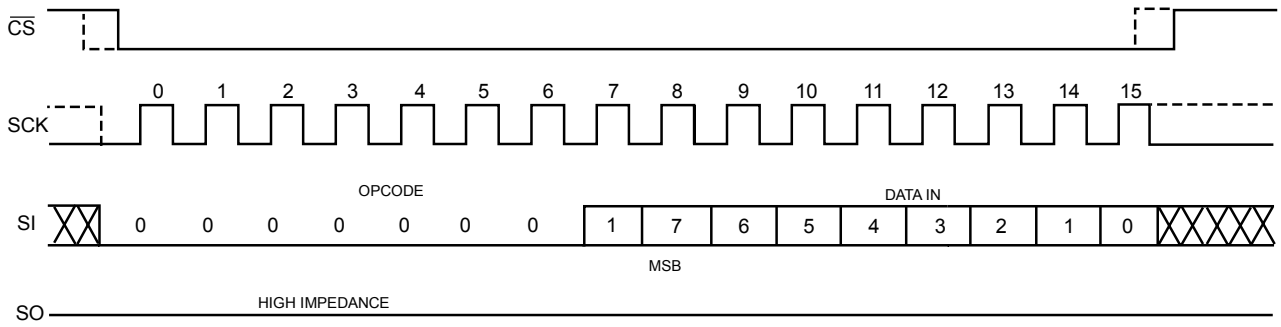
Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 8. Only bits 2, 3 and 7 can be written using the WRSR command.

Write Protection

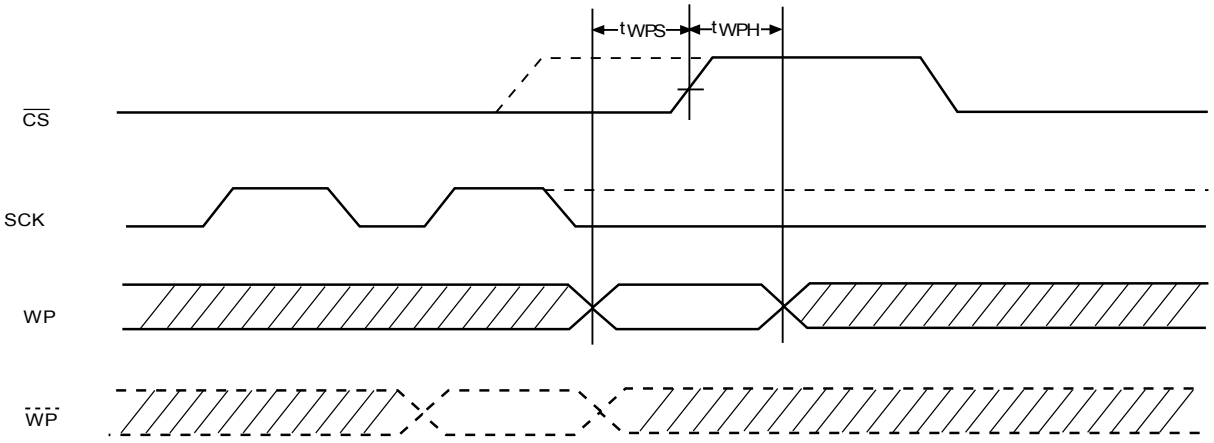
The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the WPEN bit is set to “1”, write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to “0”. The $\overline{WP}$ input timing is shown in Figure 9.

Figure 8. WRSR Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Figure 9. $\overline{WP}$ Timing



Note: Dashed Line = mode (1, 1) - - - - - -

READ OPERATIONS

Read from Memory Array

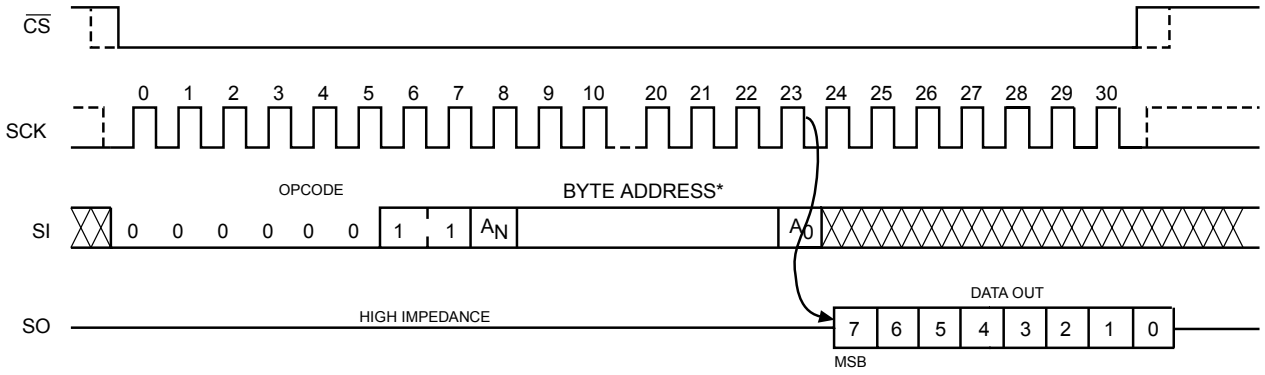
To read from memory, the host sends a READ instruction followed by a 16-bit address (see Table 5 for the number of significant address bits).

After receiving the last address bit, the CAT15008/16 will respond by shifting out data on the SO pin (as shown in Figure 10). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT15008/16 will shift out the contents of the status register on the SO pin (Figure 11). The status register may be read at any time, including during an internal write cycle.

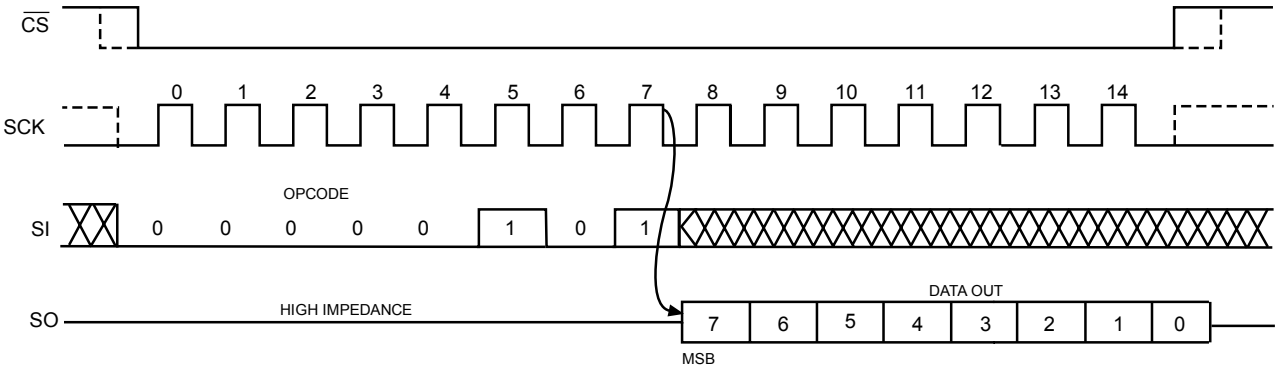
Figure 10. READ Timing



* Please check the Byte Address Table (Table 5).

Note: Dashed Line = mode (1, 1) - - - - - -

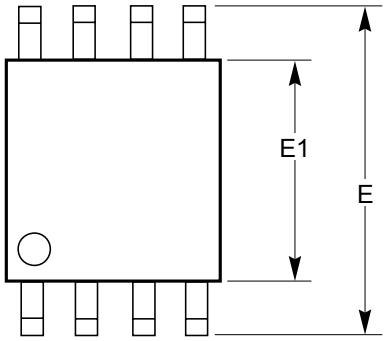
Figure 11. RDSR Timing

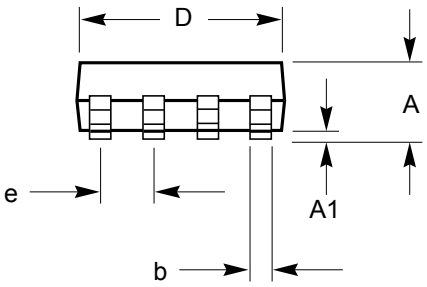


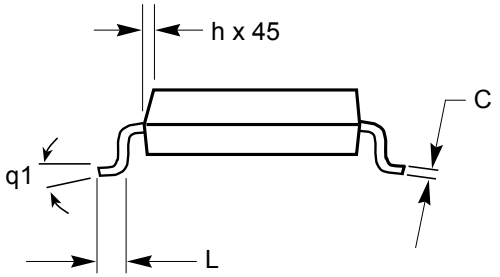
Note: Dashed Line = mode (1, 1) - - - - - -

PACKAGE OUTLINES

8-LEAD 150 MIL SOIC (W)







SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
q1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

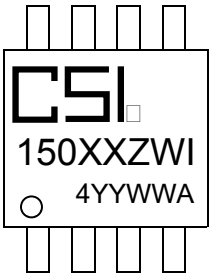
Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC specification MS-012 dimensions.

PACKAGE MARKING

8-LEAD SOIC

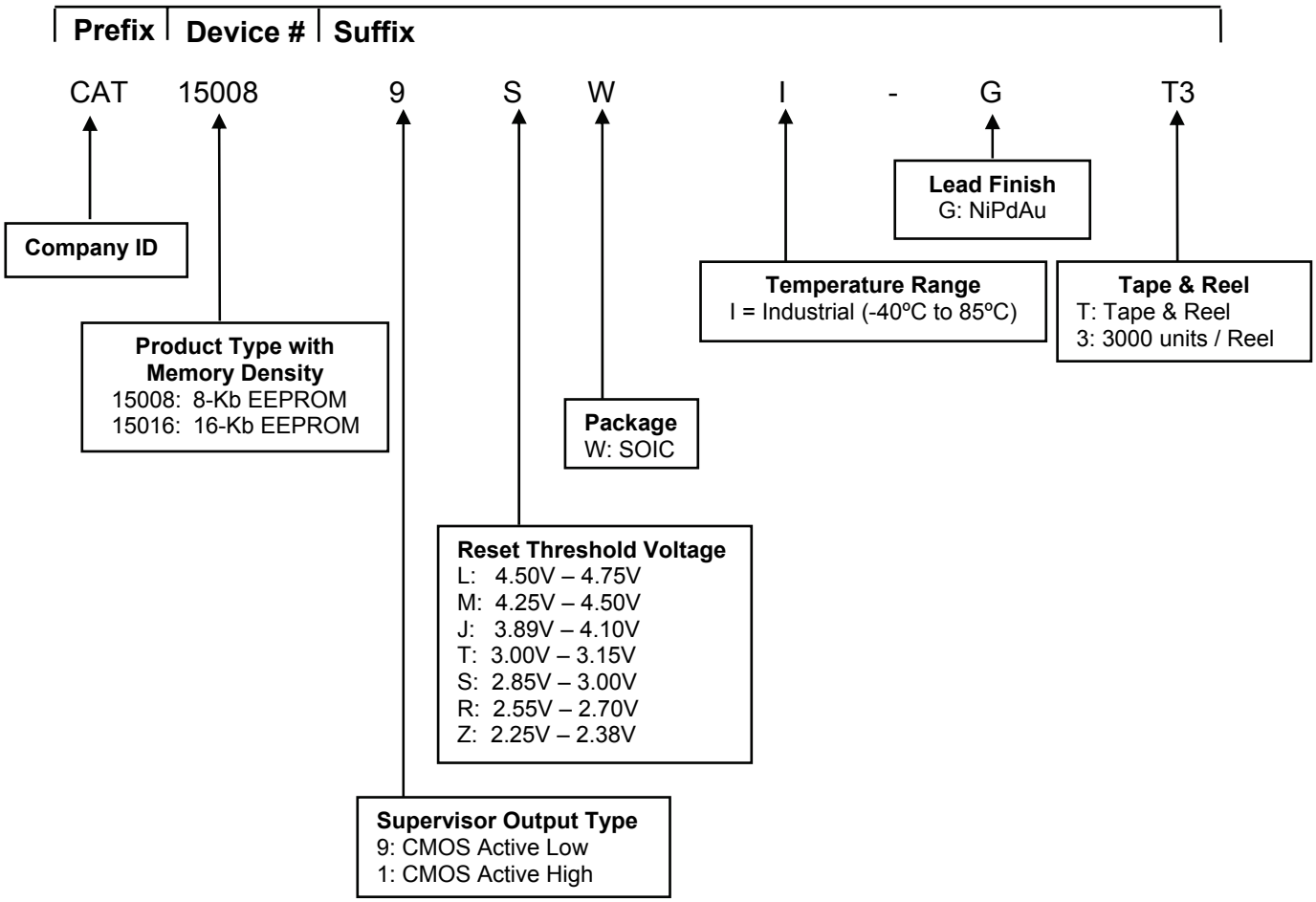


CSI = Catalyst Semiconductor, Inc.
XX = Device Code (see Marking Code table below)
Z = Supervisory Output Code (see Marking Code table below)
I = Temperature Range
YY = Production Year
WW = Production Week
A = Product Revision
4 = Lead Finish NiPdAu

	Device Marking Codes XX
15008	08
15016	16

	Supervisory Marking Codes Z
output active low	9
output active high	1

ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu pre-plated (PPF) lead frames.

(3) The device used in the above example is a CAT150089SWI-GT3 (8Kb EEPROM, with Active Low CMOS Reset output, with a reset threshold between 2.85V - 3.00V, SOIC package, Industrial Temperature, NiPdAu, Tape and Reel.

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Reason
01/15/07	A	Initial Issue

Catalyst Semiconductor, Inc.
Corporate Headquarters
2975 Stender Way
Santa Clara, CA 95054
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

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