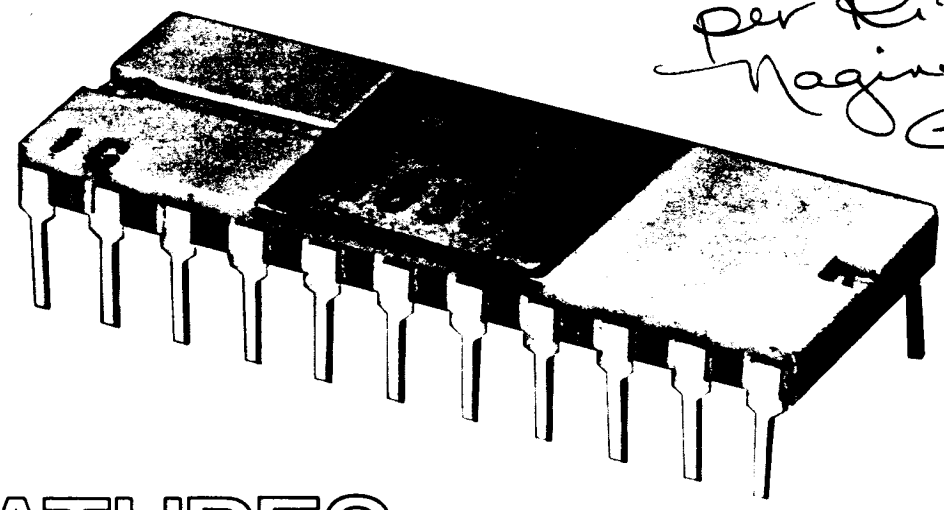
SEMI 4402A,B

100, 150 NSEC STATIC DIFFERENTIAL OUTPUT

4096 x 1 **N-MOS RAM**

OBSOLETE per Rich Naginski @ GTE 6/18/82



FEATURES

- ☐ STATIC – NO REFRESH OR CHARGE PUMP OSCILLATOR REQUIRED
- ☐ 4096 WORD x 1 BIT ORGANIZATION
- ☐ 100 NSEC ACCESS, 300 NSEC CYCLE – 4402B
- ☐ 150 NSEC ACCESS, 350 NSEC CYCLE – 4402A
- ☐ ON-CHIP ADDRESS REGISTER
- ☐ TTL COMPATIBLE ADDRESS AND DATA INPUTS
- ☐ LOW OPERATING POWER 450 MW TYP.
- ☐ DATA RETENTION TO V_{DD} = 4V
- ☐ STANDARD 22 PIN DIP, PIN AND VOLTAGE COMPATIBLE WITH POPULAR 4096 BIT DYNAMIC RAMS

The SEMI 4402 is an N-Channel MOS random access memory, organized as 4096 words by one bit. It uses a fully static memory cell which eliminates the need for any refresh or charge-pump circuitry.

The device is packaged in a standard 22-pin DIP. All inputs are TTL compatible except Chip Select, which requires a +12V level. Two complementary Data Out signals are provided, to drive a differential amplifier.

Simple memory expansion is made possible by the Chip Select input which causes the device to enter a standby state of low power and high output impedance when unselected. High impedance inputs and outputs enable memory expansion to be accomplished with a minimum of support circuitry.

Use of well-established technologies and conservative design rules contribute towards the high reliability of the 4402 product.

ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD}	-0.5 to +15	Vdc
	V_{BB}	+0.5 to -7	Vdc
Input & Output Voltages (except Chip Select)	V_I, V_O	V_{BB} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{BB} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMEND OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

Note 2: At 25°C ambient, Derate 13.5mw/°C.

RECOMMENDED OPERATING CONDITIONS T_A = 0°C to +70°C

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltages	V_{DD}	11.4	12	12.6	V
	V_{BB}	4.5	5	5.5	V
Logic Levels. Input High Voltage (except Chip Select)	V_{IH}	3	–	5.25	V
Input Low Voltage (except Chip Select)	V_{IL}	−1	–	0.7	V
Chip Select High Voltage	V_{CH}	V_{DD} −2	V_{DD}	V_{DD}+2V	V
Chip Select Low Voltage	V_{CL}	−.5	–	0.5	V

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Input Current (except Chip Select)	V_{IH} = 5.0V (V_{CS} = V_{CH})	I_{IH}	−20	5	+20	µA
	V_{IL} = 0.5V (V_{CS} = V_{CH})	I_{IL}	−20	−5	+20	µA
Chip Select High Input Current, DC (V_{CS} = 12V)		I_{CH}	–	2	3	mA
Chip Select High Input Current, (Pulse Peak) V_{CS} = 12V, T_{CR} = 25ns		I_{CP}	–	70	–	mA
Chip Select Low Input Current (V_{CS} = 0.5V)		I_{CL}	–	2	3	mA
Supply Current, (T_{AMB} =25° C; V_{DD}, V_{BB} = nominal; all VI = max V_{IL}; DO, $\overline{DO}$ terminated as shown in Figure 2)	Unselected (Chip Select = 0 V)	I_{DDU} 25°C	–	1	5	mA
		I_{DDU} 70°C	–	3	15	mA
		I_{BBU}	–	−2	-3	mA
*See IDD vs Cycle time curve Selected and Averaged Over One Cycle	Selected * CSW 200ns Cycle = 350ns	I_{DD}	–	36	50	mA
		I_{BB}	–	−2	−3	mA
Standby Current at Reduced Voltages V_{DD} = 4V, V_{BB} = −4.0, V_{CS} = 0V	25°C	I_{DDS}	–	.5	1.8	mA
	70°C	I_{DDS}	–	1.5	5.3	mA
Output Low Voltage Terminated per Figure 2TCSW ≤ 1µsec		V_{OL}	–	0	.1	V
Output High Voltage Terminated per Figure 2TCSW ≤ 1µsec		V_{OH}	.35	1	2	V
Output Disabled Current V_{CS} = 0V, V_O = 2V		I_{DO}	+10	–	−10	µA

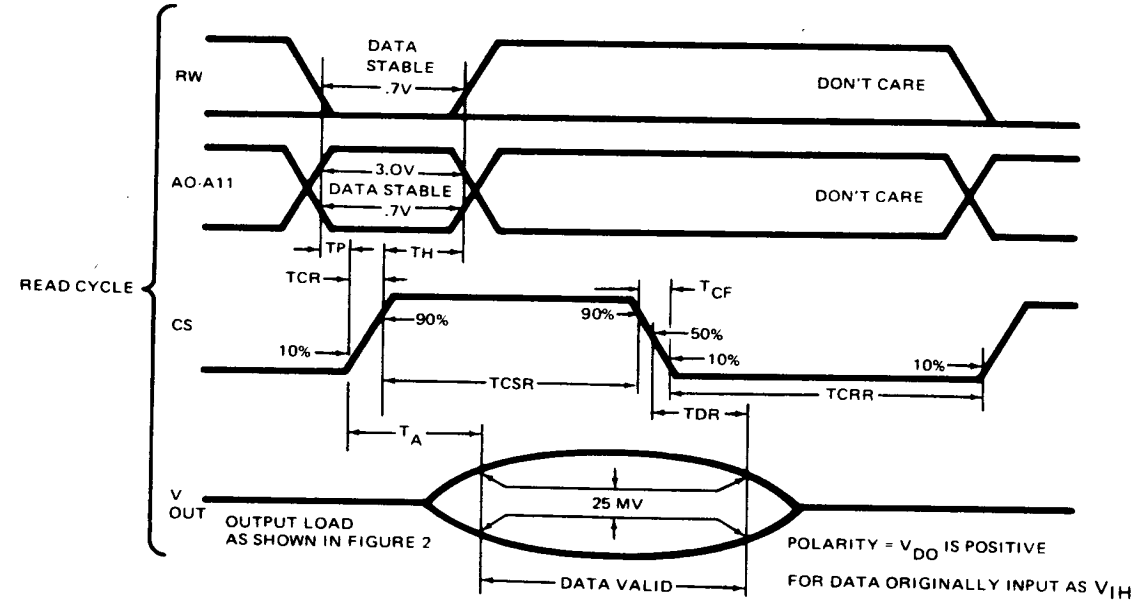
AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

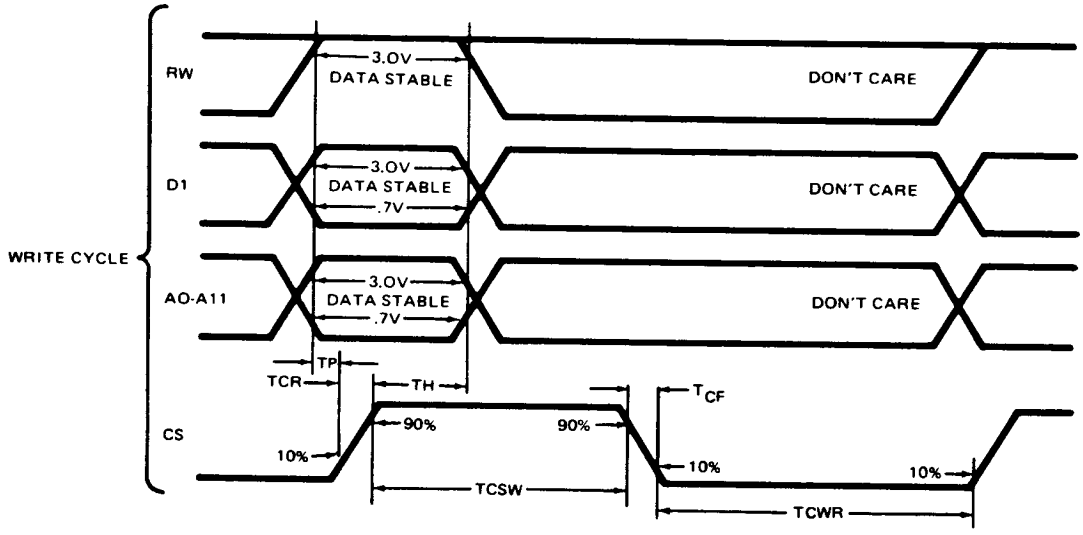
Characteristics		Symbol	Min	Typ	Max	Unit
Chip Select Read And Write Pulse Width	4402A	T_{CSR}, T_{CSW}	150	–		ns
	4402B		125	–		ns
Chip Select Read and Write Recovery Time	4402A	T_{CRR}, T_{CWR}	175	–		ns
	4402B		150	–		ns
Chip Select Rise And Fall Time		T_{CR}, T_{CF}		10	50	ns
Hold Time (Address And Data)		T_H	100	–		ns
Set Up Time		T_P	10	–		ns
Access Time (T_{CR} = 10ns)	4402A	T_A	–	–	150	ns
	4402B		–	–	100	ns
Cycle Time (Read or Write, T_{CR} = 10ns, T_{CF} = 10ns)	4402A	T_C	350	–	–	ns
	4402B		300	–	–	ns
Data Recovery		T_{DR}	10	15	–	ns

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

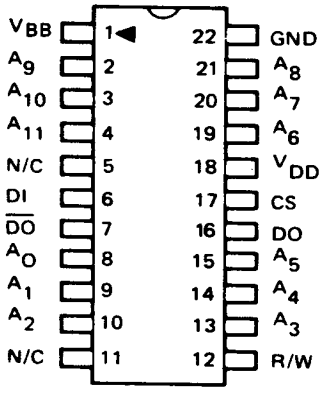
Characteristics	Symbol	Min	Typ	Max	Unit
Input Capacitance (except Chip Select) V_I = 2.4V, V_{CS} = 12V	C_I	–	4	6	pF
Chip Select Input Capacitance	C_{CS}	–	50	–	pF
Output Capacitance (V_O = 2.0V, V_{CS} = 0 V)	C_O	–	4	6	pF

TIMING DIAGRAMS



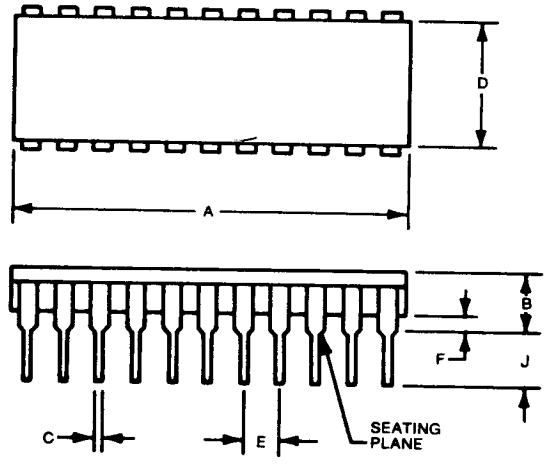


TOP VIEW



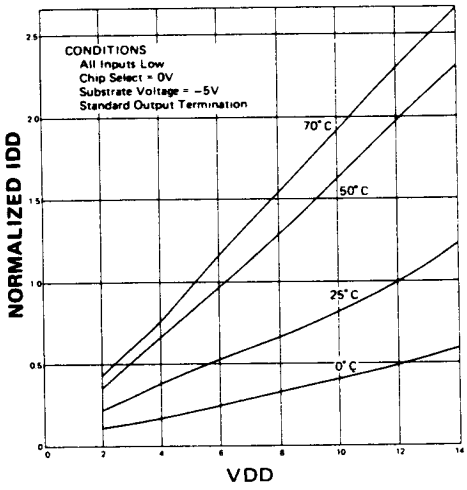
PIN ASSIGNMENT

CERAMIC PACKAGE DIMENSIONS

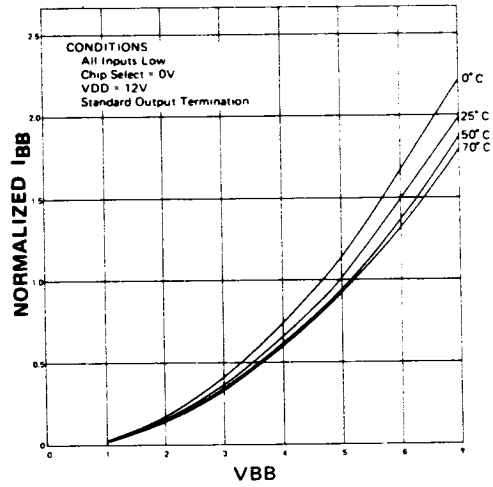


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.1	27.8	1.065	1.095
B	—	3.56	—	0.140
C	0.38	0.53	0.015	0.023
D	8.64	10.8	0.340	0.425
E	2.29	2.79	0.090	0.110
F	0.64	1.65	0.025	0.065
G	0.20	0.30	0.008	0.012
J	2.54	3.81	0.100	0.150
K	10.2 REF		0.4 REF	

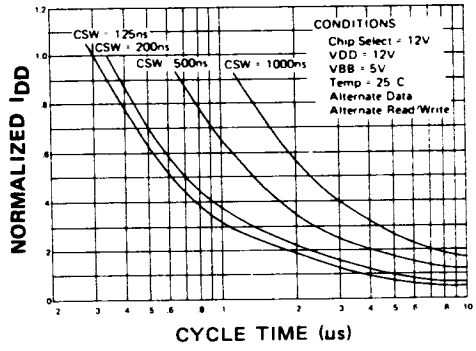
IDD vs VDD AT VARIABLE TEMPERATURE



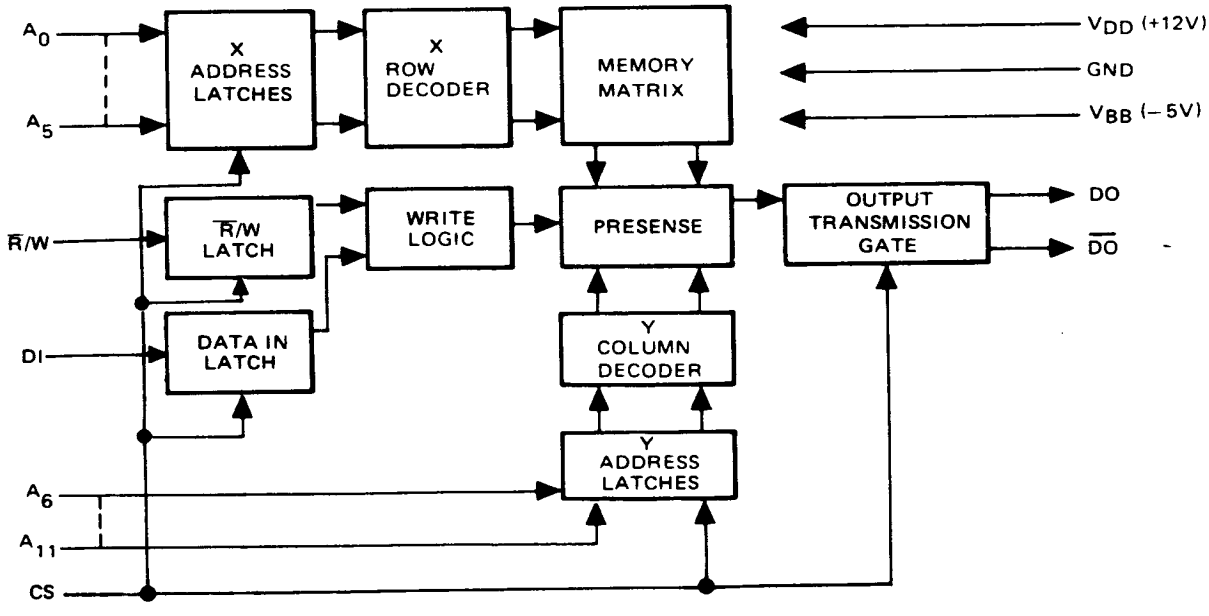
I_{BB} vs V_{BB} AT VARIABLE TEMPERATURE



AVERAGE I_{DD} VS. CYCLE TIME



BLOCK DIAGRAM



DEVICE OPERATION

Basic Operation

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns. The memory cells are loaded or interrogated by simultaneously decoding the X address A_0 through A_5 for the rows (see Block Diagram) and the Y address A_6 through A_{11} for the columns. Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output stage. Each bit or memory cell is a standard flip flop consisting of R_1, R_2, Q2D, and Q4D with two access devices Q1D and Q3D (See Figure 1). The load resistors R_1 and R_2 are 60 megohms typical and connect to the V_{DD} supply. Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high. In the read mode the cell will pull one of the sense lines low from its normally high state. The selected presense circuit will detect the differential voltage on the sense lines and amplify it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines.

Chip Select

The chip select controls the operation of the memory. When the chip select is low the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements. When the Chip Select goes high the memory is enabled. The Chip Select pulse clocks the TTL logic level addresses, $\overline{R}/W$, and data input into "D" type flip flops and enables the output stage.

Data Output

One of the two outputs will source current (DO for data originally input as V_{IH}, $\overline{DO}$ for data originally input as V_{IL}). With the output load as shown in Figure 2, the voltage at the output sourcing current (V_{OH}) will approach a value between 0.35V and 2V (typically 1V) above ground. The voltage at the other output (V_{OL}) will be below 100mV. A differential amplifier is used to detect the polarity of the signal. A differential output of 25mV (V_{OUT}) or more is considered a valid output.

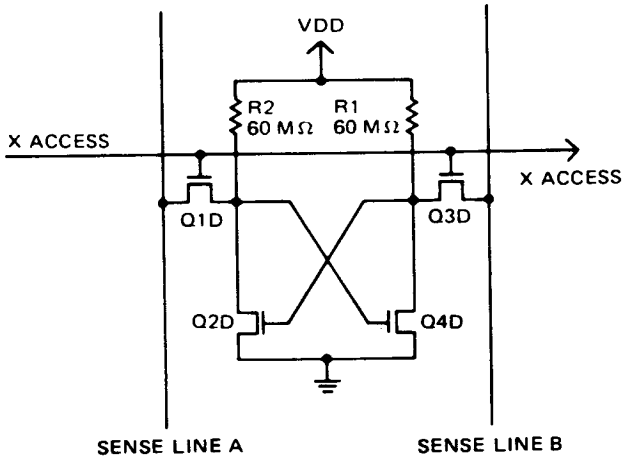


Figure 1. MEMORY CELL

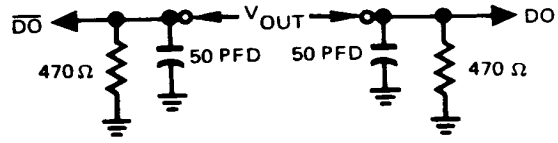


Figure 2. OUTPUT LOAD

Note: The resistence shown is the recommended termination. The capacitive loading is used to simulate the effect of seven additional outputs plus one TTL load.

Battery Operation/Power Failure Data Retention

The memory cells (because they are cross coupled high impedance static cells) will retain data down to V_{DD} = 4V. At V_{DD} = 4V, the typical power dissipated is 1 μw/bit.

Input Circuits — R/W Select, Data In and Address Input

The input signal is latched by Chip Select and can change after Chip Select is high. The inputs can be driven from standard TTL open collector outputs with pull-up resistors. The input does not put any DC loading on the TTL driver.

Read/Write Mode Select

To WRITE, the R/W Input should be HIGH prior to Chip Select. To READ, the R/W Input should be LOW prior to Chip Select. When Chip Select is high, R/W is latched into a register.

Data In

During a WRITE cycle the Data in (either HIGH or LOW) should be stable prior to Chip Select. When Chip Select is high, Data In is latched into a register.

Address

Addresses should be stable prior to Chip Select. When Chip Select is HIGH all addresses are latched into an Address Register.

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