M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V408B is a family of low voltage 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5V408B is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

M5M5V408B is packaged in 32-pin plastic SOP, 32-pin plastic TSOP and 32-pin 8mm x 13.4mm STSOP packages. Two types of TSOPs and two types of STSOPs are available, M5M5V408BTP (normal-lead-bend TSOP), M5M5V408BRT (reverse-lead-bend TSOP), M5M5V408BKV (normal-lead-bend STSOP) and M5M5V408BKR (reverse-lead-bend STSOP). These two types TSOPs and two types STSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single +2.7~+3.6V power supply
- Small stand-by current: 0.3µA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS
- Package:
  M5M5V408BFP: 32 pin 525 mil SOP
  M5M5V408BTP/RT: 32 PIN 400mil TSOP(II)
  M5M5V408BKV/KR: 32 pin 8mm x13.4mm STSOP

PART NAME TABLE

Version, Operating temperature	Part name (## stands for "FP","TP", "RT","KV"or"KR")	Power Supply	Access time max.	Stand-by current Icc(PD), Vcc=3.0V						Active current Icc1 (3.0V, typ.)
				typical *		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5V408B## -70L	2.7 ~ 3.6V	70ns	---	---	---	---	30µA	---	30mA (10MHz) 5mA (1MHz)
	M5M5V408B## -85L		85ns							
	M5M5V408B## -70H	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	---	
	M5M5V408B## -85H		85ns							
W-version -20 ~ +85°C	M5M5V408B## -70LW	2.7 ~ 3.6V	70ns	---	---	---	---	30µA	60µA	
	M5M5V408B## -85LW		85ns							
	M5M5V408B## -70HW	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	30µA	
	M5M5V408B## -85HW		85ns							
I-version -40 ~ +85°C	M5M5V408B## -70LI	2.7 ~ 3.6V	70ns	---	---	---	---	30µA	60µA	
	M5M5V408B## -85LI		85ns							
	M5M5V408B## -70HI	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	30µA	
	M5M5V408B## -85HI		85ns							

* "typical" parameter is sampled, not 100% tested.

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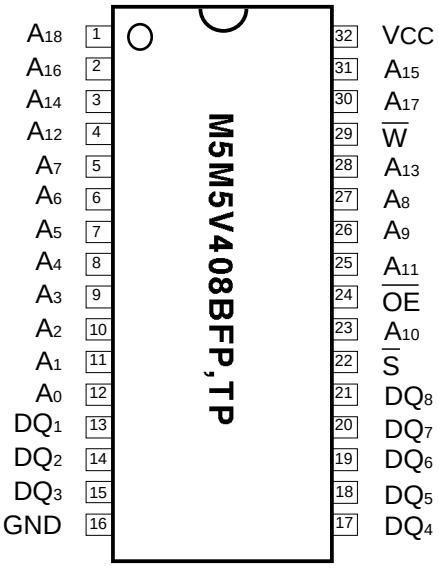
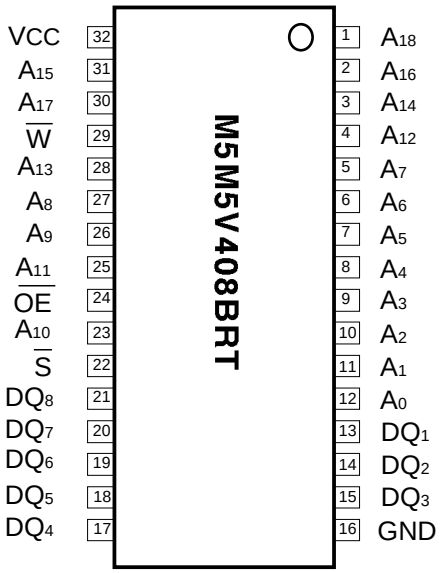
4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

PIN CONFIGURATION (TOP VIEW)

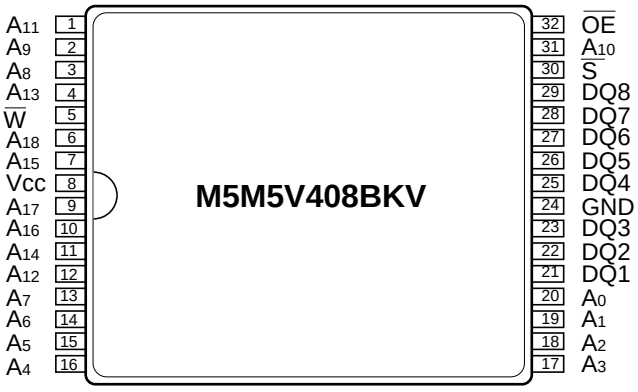
Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
$\overline{S}$	Chip select input
$\overline{W}$	Write control input
$\overline{OE}$	Output inable input
Vcc	Power supply
GND	Ground supply



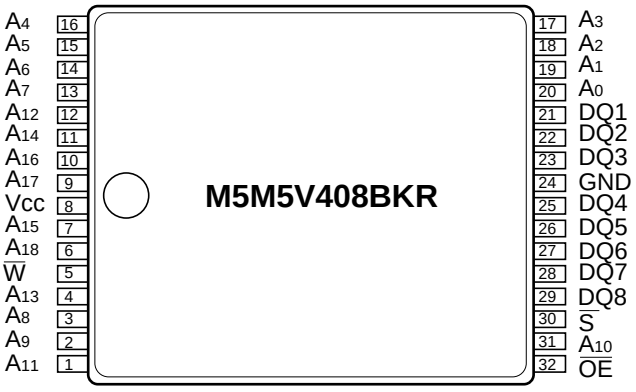
Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J (RT)



Outline 32P3K-B



Outline 32P3K-C

M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,RT,KV,KR is organized as 524,288-words by 8-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while S are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

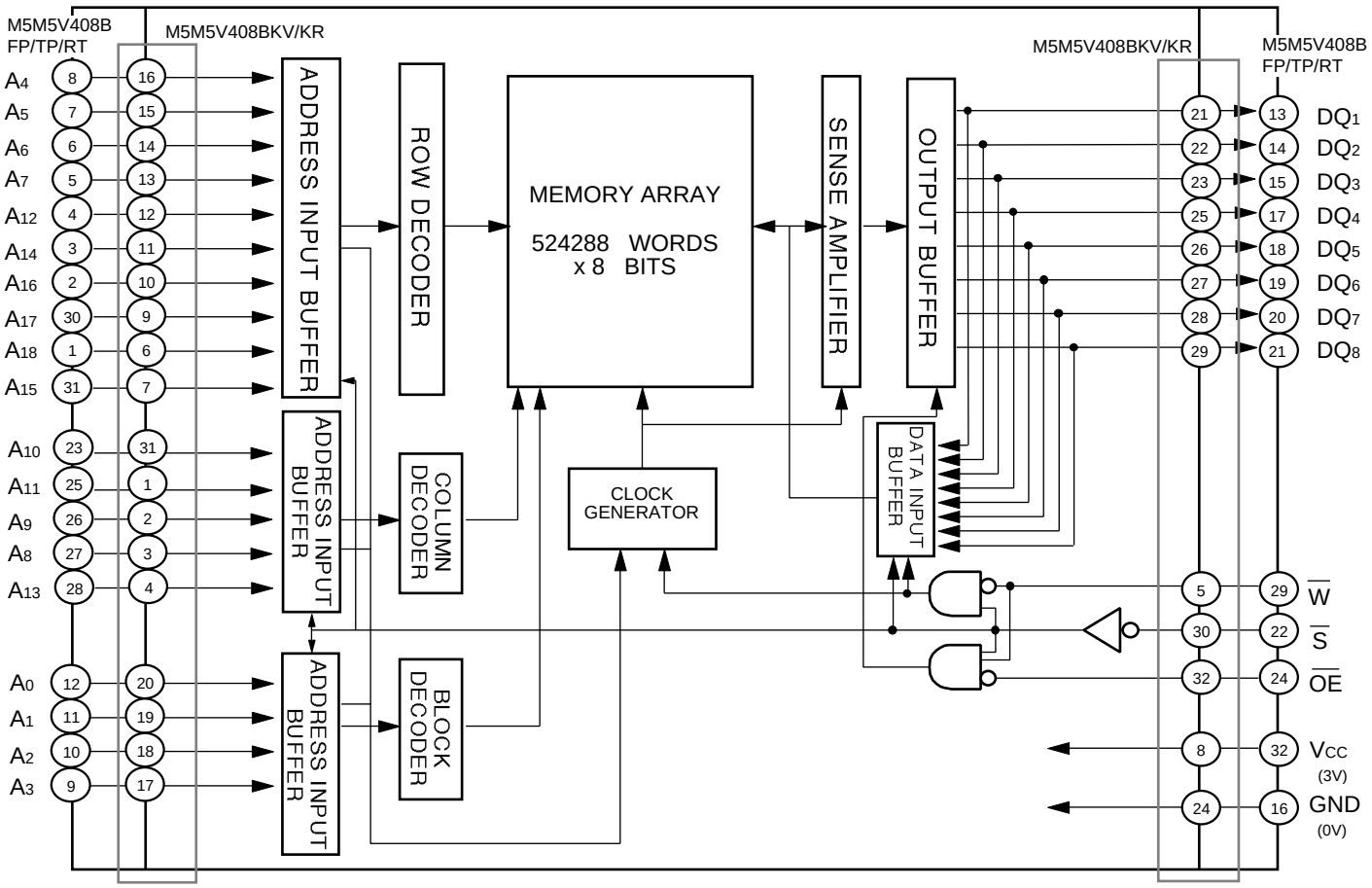
The power supply current is reduced as low as 0.3µA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	Data input (D)	Active
L	H	L	Read	Data output (Q)	Active
L	H	H	Read	High-impedance	Active

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
$\overline{S}$	Chip select input
$\overline{W}$	Write control input
$\overline{OE}$	Output inable input
Vcc	Power supply
GND	Ground supply

BLOCK DIAGRAM



M5M5V408BFP,TP,RT,KV

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V_I	Input voltage	With respect to GND	-0.5* ~ Vcc + 0.5	
V_O	Output voltage	With respect to GND	0 ~ Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T_{stg}	Storage temperature		-65 ~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions			Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage				2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage				-0.3 *		0.6	
V_{OH1}	High-level output voltage 1	I_{OH}= -0.5mA			2.4			
V_{OH2}	High-level output voltage 2	I_{OH}= -0.05mA			Vcc-0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA					0.4	
I_I	Input leakage current	V_I=0 ~ Vcc					±1	µA
I_O	Output leakage current	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 ~ Vcc					±1	
Icc1	Active supply current (AC, CMOS-level)	$\overline{S}$ ≤0.2V Output-open Other inputs ≤0.2V or ≥Vcc-0.2V		f= 10MHz	-	30	40	mA
				f= 1MHz	-	5	7	
Icc2	Active supply current (AC,TTL-level)	$\overline{S}$=VIL Output-open Other inputs=V_{IH} or V_{IL}		f= 10MHz	-	30	40	
				f= 1MHz	-	5	7	
Icc3	Stand by supply current (CMOS-level input)	Vcc=3.6V, max. $\overline{S}$ ≥Vcc-0.2V Other inputs=0~Vcc	-LW, -LI	+85°C	-	-	80	µA
			-L, -LW, -LI	+70°C	-	-	40	
			-HW, -HI	+85°C	-	-	40	
			-H, -HW, -HI	+70°C	-	-	20	
				+40°C	-	1	5	
			-H	0 ~ +25°C	-	0.3	2	
			-HW	-20 ~ +25°C	-	0.3	2	
			-HI	-40 ~ +25°C	-	0.3	2	
Icc4	Stand by supply current (TTL-level input)	$\overline{S}$=V_{IH} ,Other inputs= 0 ~ Vcc			-	-	0.5	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

Note 2: Typical value is for Vcc=3.0V

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE

(Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Units
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			8	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	

AC ELECTRICAL CHARACTERISTICS (Vcc=2.7 ~ 3.6V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	2.7V~3.6V
Input pulse	V_{IH}=2.4V,V_{IL}=0.4V
Input rise time and fall time	5ns
Reference level	V_{OH}=V_{OL}=1.5V Transition is measured ±500mV from steady state voltage.(for t_{en},t_{dis})
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)

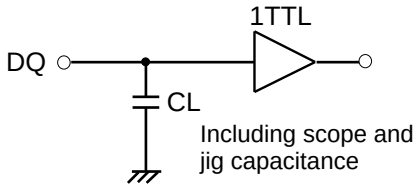


Fig.1 Output load

(2) READ CYCLE

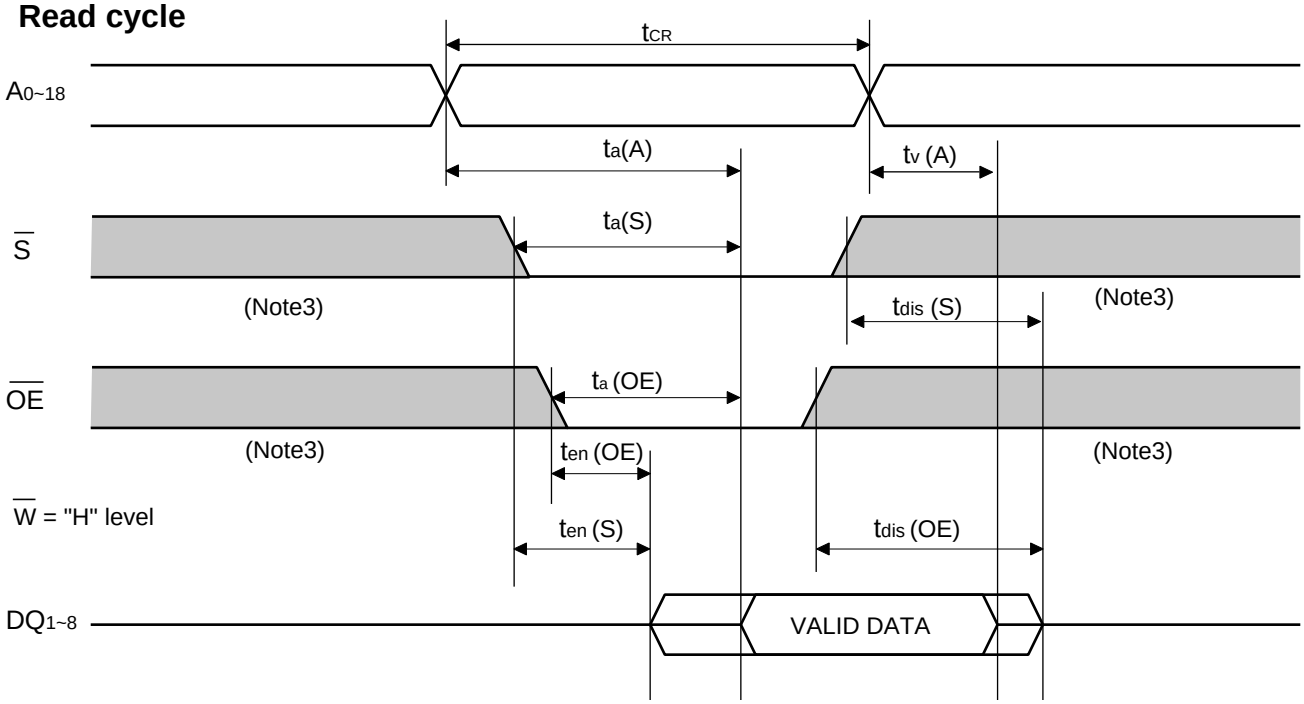
Symbol	Parameter	Limits				Units
		M5M5V408B FP,TP,RT,KV,KR-70		M5M5V408B FP,TP,RT,KV,KR-85		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		ns
t_a(A)	Address access time		70		85	ns
t_a(S)	Chip select access time		70		85	ns
t_a(OE)	Output enable access time		35		45	ns
t_{dis}(S)	Output disable time after $\overline{S}$ high		25		30	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		25		30	ns
t_{en}(S)	Output enable time after $\overline{S}$ low	10		10		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		ns
t_v(A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

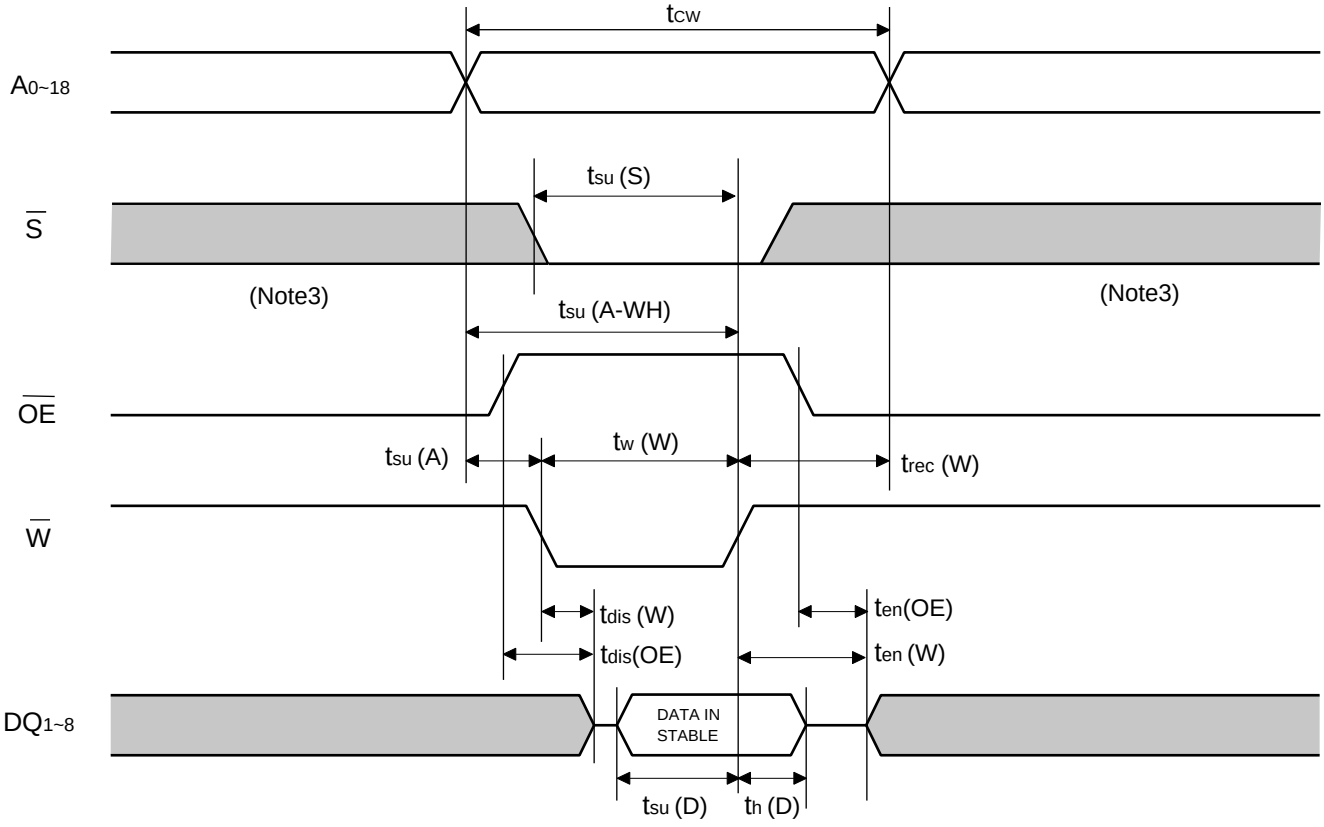
Symbol	Parameter	Limits				Units
		M5M5V408B FP,TP,RT,KV,KR-70		M5M5V408B FP,TP,RT,KV,KR-85		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		ns
t_w(W)	Write pulse width	55		60		ns
t_{su}(A)	Address set up time	0		0		ns
t_{su}(A-WH)	Address set up time with respect to $\overline{W}$ high	65		70		ns
t_{su}(S)	Chip select set up time	65		70		ns
t_{su}(D)	Data set up time	35		35		ns
t_h(D)	Data hold time	0		0		ns
t_{rec}(W)	Write recovery time	0		0		ns
t_{dis}(W)	Output disable time after $\overline{W}$ low		25		30	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		25		30	ns
t_{en}(W)	Output enable time after $\overline{W}$ high	5		5		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		ns

(4)TIMING DIAGRAMS

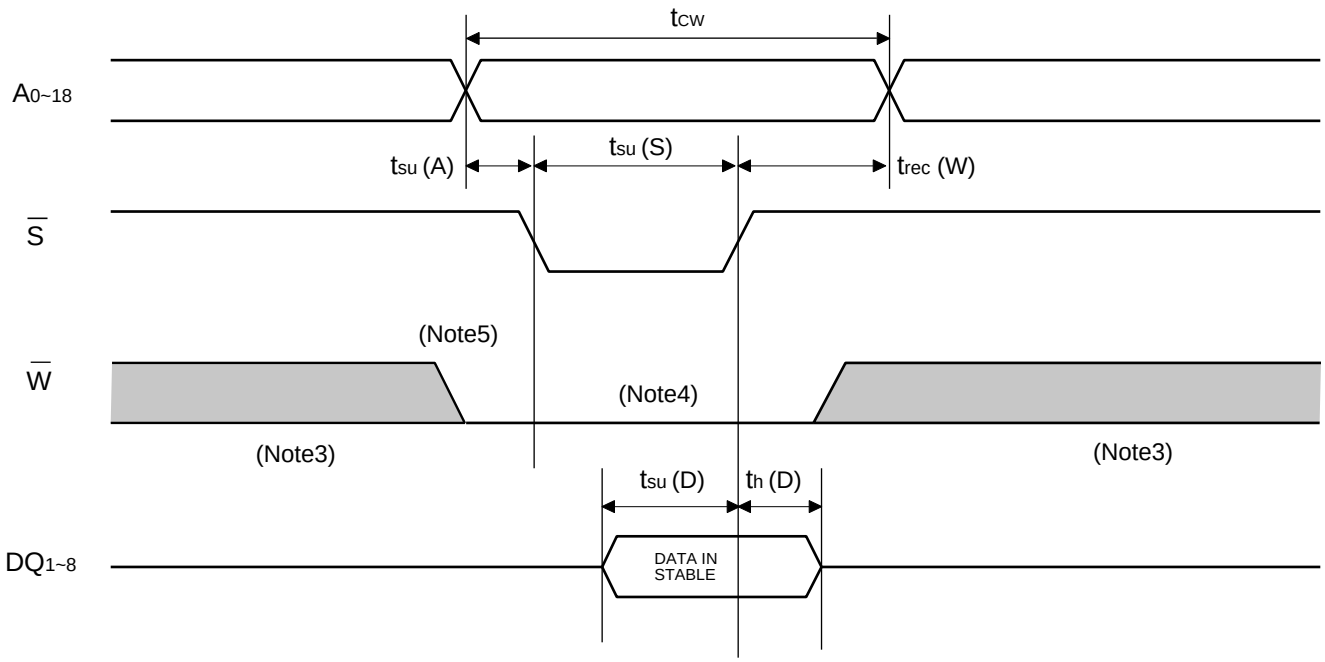
Read cycle



Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

Note 5: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$,the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage				2.0			V
$V_{I\ (\overline{S})}$	Chip select input $\overline{S}$				2.0			V
Icc (PD)	Power down supply current	Vcc=3.0V, $\overline{S}$≥Vcc-0.2V, Other inputs = 0 ~ Vcc	-LW, -LI	+85°C	-	-	60	µA
			-L, -LW, -LI	+70°C	-	-	30	µA
			-HW, -HI	+85°C	-	-	30	µA
			-H, -HW, -HI	+70°C	-	-	15	µA
				+40°C	-	1	3	µA
			-H	0 ~ +25°C	-	0.3	1	µA
			-HW	-20 ~ +25°C	-	0.3	1	µA
			-HI	-40 ~ +25°C	-	0.3	1	µA

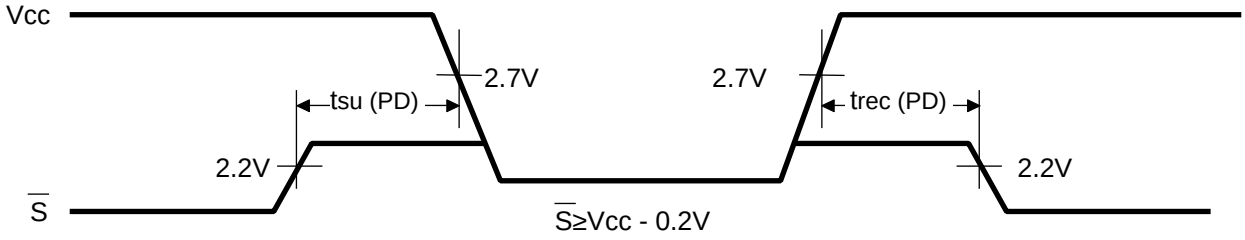
Typical value is based on sampling.

(2) TIMING REQUIREMINTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) TIMING DIAGRAM

$\overline{S}$ control mode



M5M5V408BFP,TP,RT,KV

Revision History

Revision No.	History	Date	Remarks
K0.1e	The first edition	'98.3.05	Preliminary
K0.2e	Added M5M5V408BFP/TP/RT	'98.7.30	Preliminary
K1.0e	The first product version	'98.9.7	---
K2.0e	1) Speed items revised: 70ns added and 100ns deleted 2) Icc3 and Icc(PD) limits revised	'99.3.10	---

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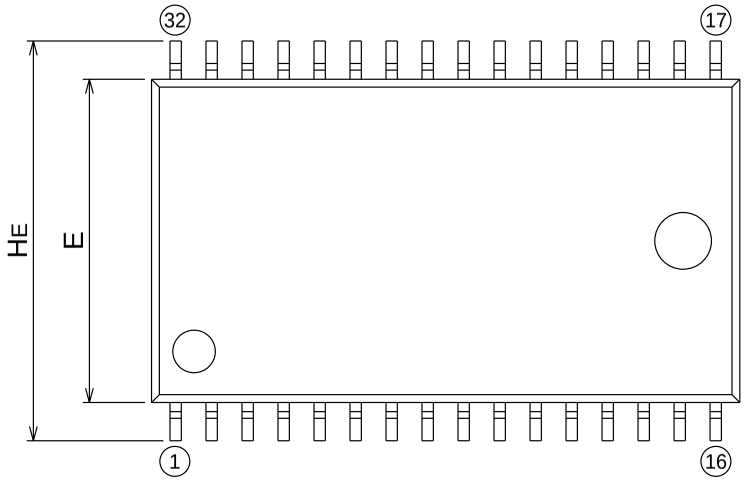
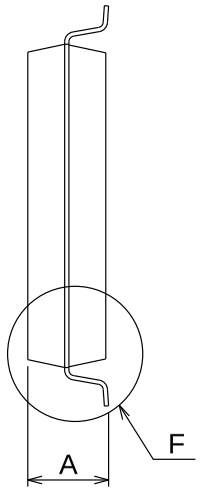
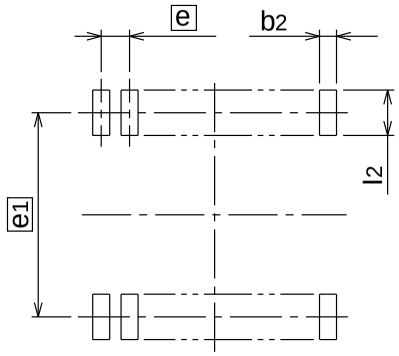
32P2M-A

Plastic 32pin 525mil SOP

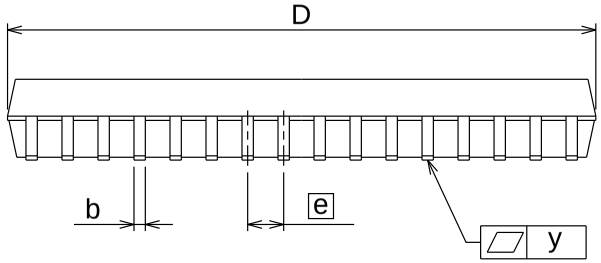
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-525-1.27	–	1.29	Alloy 42

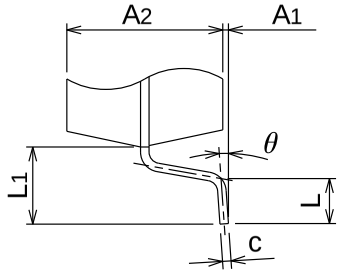






Recommended Mount Pad





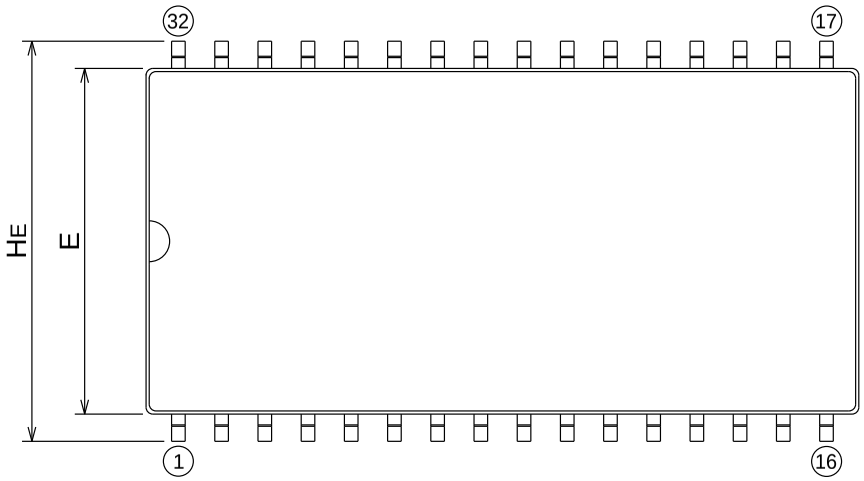
Detail F

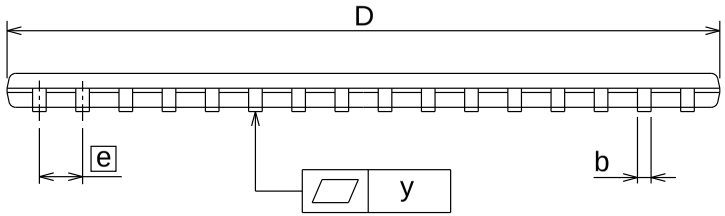
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.75	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	20.55	20.75	20.95
E	11.3	11.4	11.5
e	–	1.27	–
HE	13.8	14.1	14.4
L	0.6	0.8	1.0
L1	–	1.35	–
y	–	–	0.15
θ	0°	–	8°
b2	–	0.76	–
e1	–	13.34	–
l2	1.27	–	–

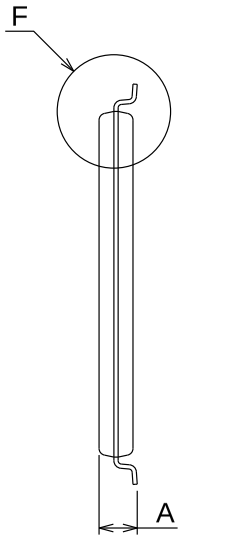
32P3Y-H

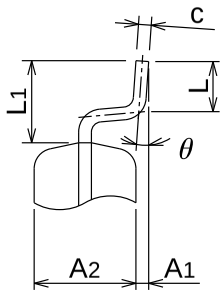
Plastic 32pin 400mil TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII32-P-400-1.27	–	0.53	Alloy 42

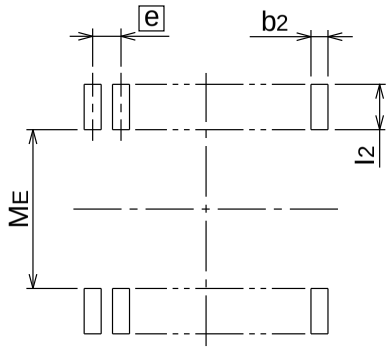








Detail F



Recommended Mount Pad

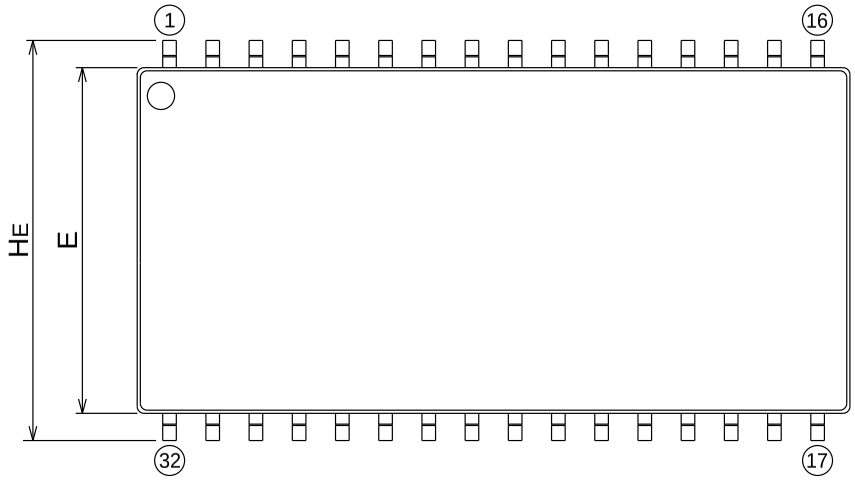
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.2
A_2	–	1.0	–
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	–	1.27	–
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	10.36	–
l_2	0.9	–	–
b_2	–	0.76	–

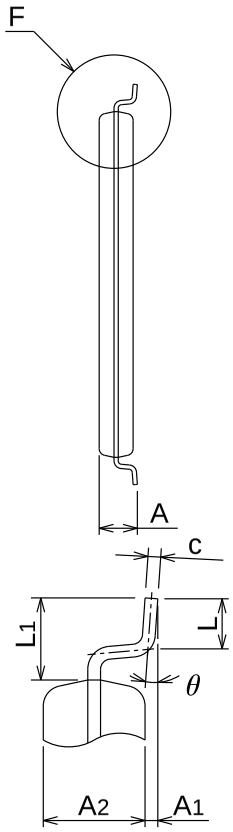
Mar.'98

32P3Y-J

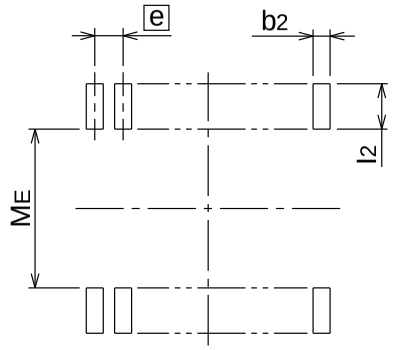
Plastic 32pin 400mil TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII32-P-400-1.27	–	0.53	Alloy 42





Detail F



Recommended Mount Pad

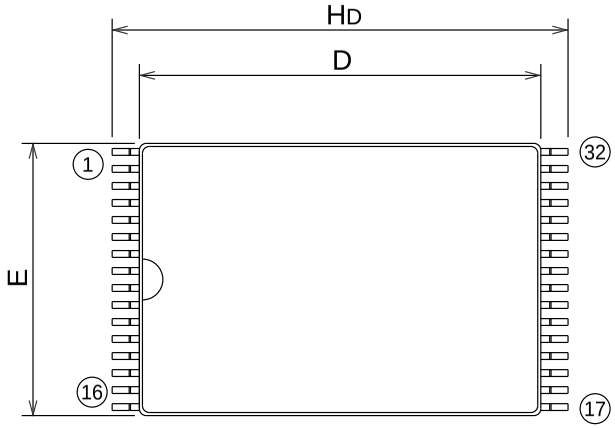
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.2
A_2	–	1.0	–
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	–	1.27	–
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	10.36	–
l_2	0.9	–	–
b_2	–	0.76	–

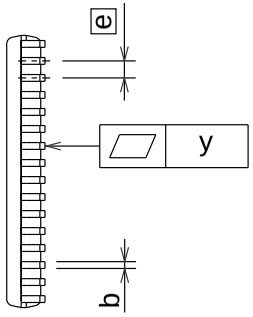
Mar.'98

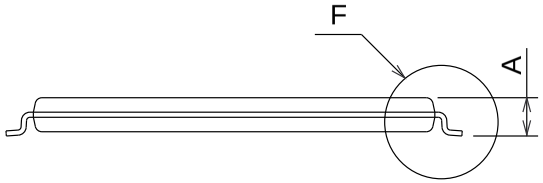
32P3K-B

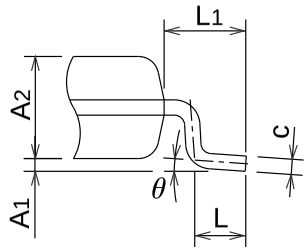
Plastic 32pin 8X13.4mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
–	–		Alloy 42

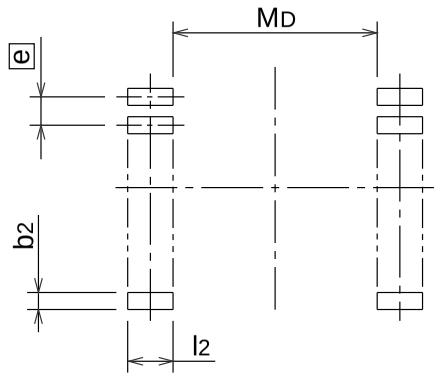








Detail F



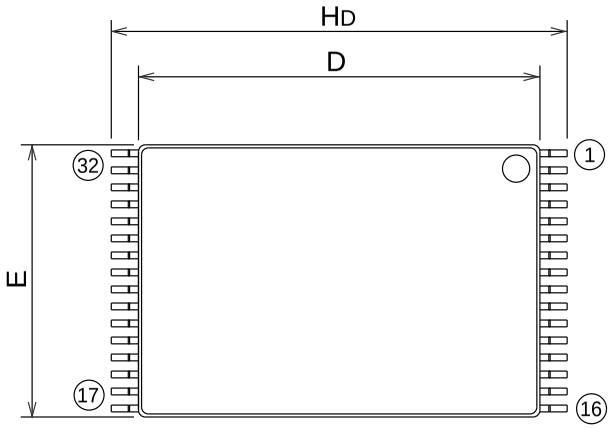
Recommended Mount Pad

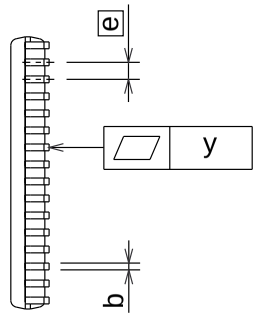
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A1	0.05	0.125	0.2
A2	–	1.0	–
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	–	0.5	–
HD	13.2	13.4	13.6
L	0.4	0.5	0.6
L1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.0	–

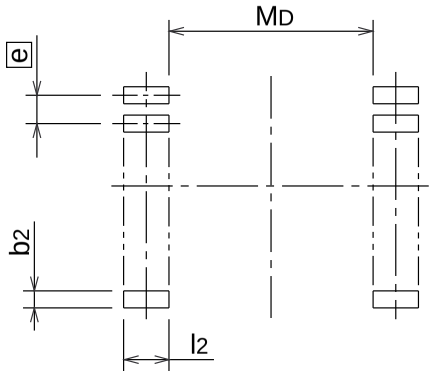
32P3K-C

Plastic 32pin 8X13.4mm TSOP(I)

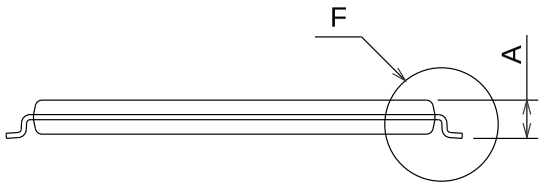
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
–	–		Alloy 42

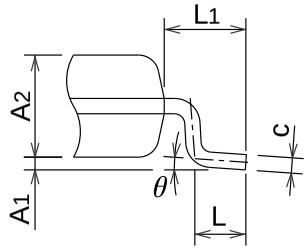






Recommended Mount Pad





Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A1	0.05	0.125	0.2
A2	–	1.0	–
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	–	0.5	–
HD	13.2	13.4	13.6
L	0.4	0.5	0.6
L1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.0	–