Dual Channel PWM Controller with 3/2/1 Phase for CORE VR and Single Phase for AXG VR

General Description

The RT8876A is a VR12/IMVP7 compliant CPU power controller which includes two channels : a 3/2/1 phase with 3 integrated drivers synchronous Buck controller for the CORE VR, and a single phase Buck controller for the AXG VR. The RT8876A adopts G-NAVP™ (Green Native Adaptive Voltage Positioning), which is Richtek's proprietary topology derived from a finite DC gain compensator with current mode control, making it an easy setting PWM controller, meeting all Intel CPU requirements of AVP. Based on the G-NAVP™ topology, the RT8876A also features a quick response mechanism for optimizing AVP performance during load transient. The RT8876A supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT8876A to communicate with Intel VR12/IMVP7 compliant CPU. The RT8876A supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT8876A varies with VID, load and input voltage to further enhance the efficiency even in CCM. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT8876A integrates a high accuracy ADC for platform setting functions, such as no-load offset or over current level.

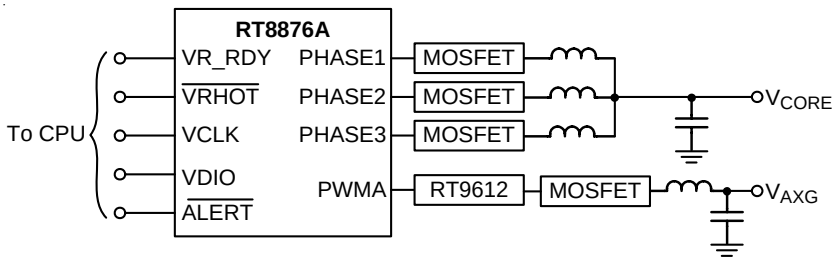
Features

- **VR12/IMVP7 Compatible Power Management**
- **3/2/1 Phase for CORE VR and Single Phase for AXG VR**
- **3 Embedded MOSFET Drivers at the CORE VR**
- **G-NAVP™ Topology**
- **Serial VID Interface**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Single Phase**
- **Fast Transient Response**
- **1.1$V_{INITIAL}$ / 0.0$V_{INITIAL}$ for both Rails at Startup**
- **Power Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, UVP, OCP, OTP, UVLO**
- **External No-load Offset Setting for both Rails**
- **DVID Enhancement**
- **56-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- VR12/IMVP7 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT8876A□□

Package Type
QW : WQFN-56L 7x7 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

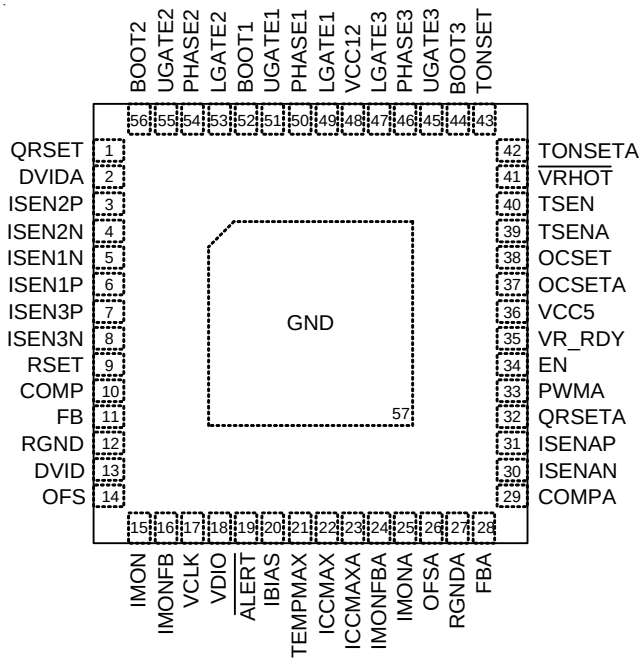
Marking Information

RT8876AGQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-56L 7x7

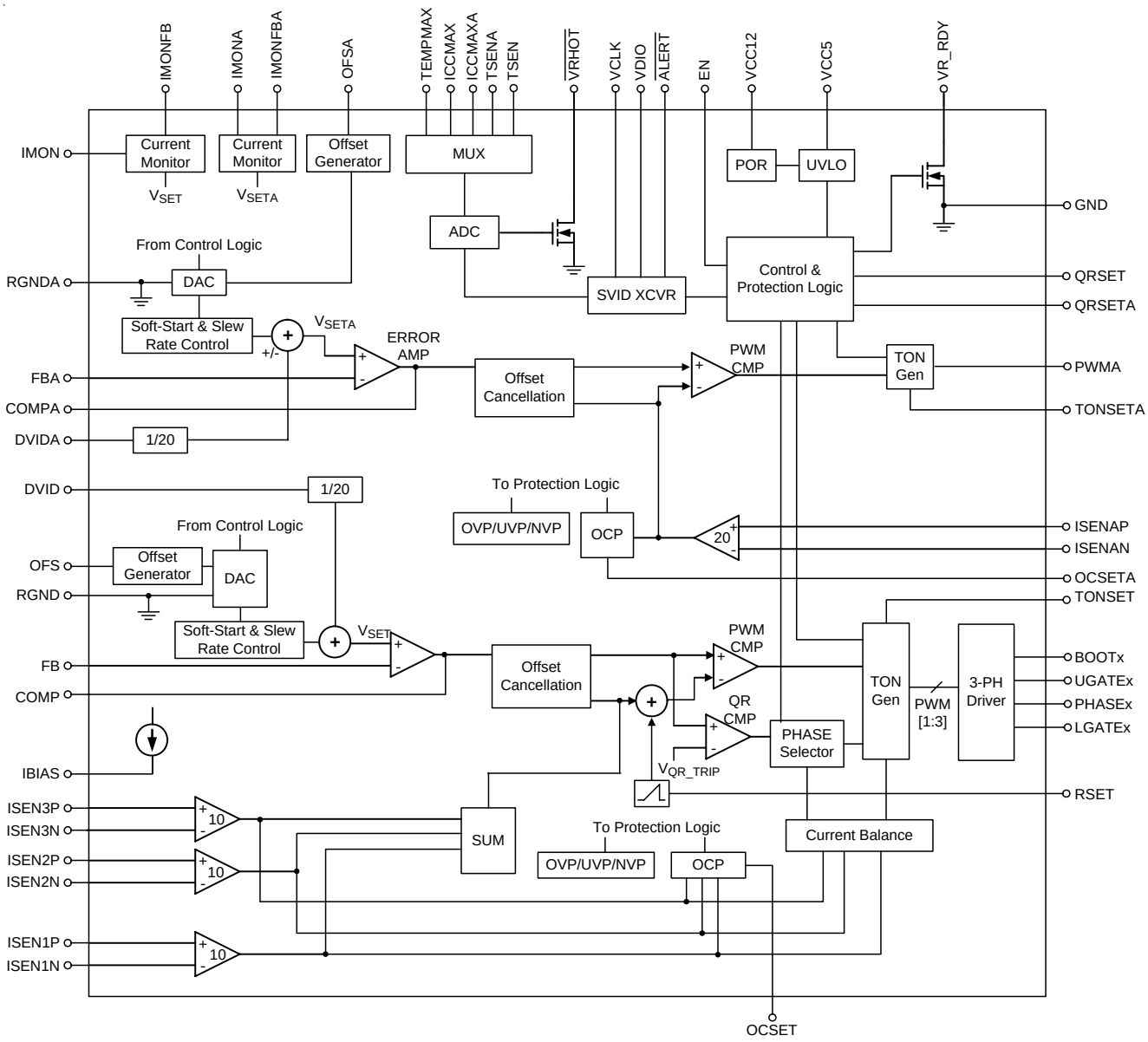
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	QRSET	Multi-phase CORE VR channel quick response time setting and initial voltage ($V_{INITIAL}$) setting.
2	DVIDA	Place a resistor and a capacitor from this pin to GND to enhance DVID performance. Short this pin to GND if not use.
5, 4, 8	ISEN [1:3] N	Negative Current Sense Pin of Phase 1, 2, 3 for CORE VR.
6, 3, 7	ISEN [1:3] P	Positive Current Sense Pin of Phase 1, 2, 3 for CORE VR.
9	RSET	Multi-Phase CORE VR Ramp Setting. This is used to set the multi-phase CORE VR loop external ramp slope.
10	COMP	Multi-Phase CORE VR Compensation Node. This pin is the output node of the error amplifier.
11	FB	Multi-Phase CORE VR Feedback Input. This is the negative input node of the error amplifier.
12	RGND	Return Ground for Multi-Phase CORE VR. This pin is the negative node of the differential remote voltage sensing.
13	DVID	Place a Resistor and a Capacitor from this Pin to GND to enhance DVID Performance. Short this pin to GND if not use.
14	OFS	Output Voltage Offset Setting.
15	IMON	Current Monitor Output. This pin outputs a voltage proportional to the output current.
16	IMONFB	Current Monitor Output Gain External Setting. Connect this pin with one resistor to CPU V_{CC_SENSE} while IMON pin is connected to ground with one another resistor. The current monitor output gain can be set by the ratio of these two resistors.

Pin No.	Pin Name	Pin Function
17	VCLK	Synchronous Clock from the CPU.
18	VDIO	Controller and CPU Data Transmission Interface.
19	$\overline{\text{ALERT}}$	SVID Alert Pin. (Active Low)
20	IBIAS	Internal Bias Current Setting. Connecting this pin to GND by a resistor can set the internal current.
21	TEMPMAX	ADC Input for Multi-Phase CORE VR Maximum Temperature Setting.
22	ICCMAX	ADC Input for Multi-Phase CORE VR Maximum Current Setting.
23	ICCMAXA	ADC Input for Single Phase AXG VR Maximum Current Setting.
24	IMONFBA	Single Phase AXG VR Current Monitor Output Gain External Setting. Connect this pin with one resistor to AXG rail V_{CCAXG_SENSE} while IMONA pin is connected to ground with another resistor. The current monitor output gain can be set by the ratio of these two resistors.
25	IMONA	Single Phase AXG VR Current Monitor Output. This pin outputs a voltage proportional to the output current.
26	OFSA	Set the AXG No-Load Offset.
27	RGNDA	Return Ground for Single Phase AXG VR. This pin is the negative node of the differential remote voltage sensing.
28	FBA	Single Phase AXG VR Feedback Input. This is the negative input node of the error amplifier.
29	COMPA	Single Phase AXG VR Compensation Node. This pin is the output node of the error amplifier.
30	ISENAN	Negative Current Sense Pin for Single Phase AXG VR.
31	ISENAP	Positive Current Sense Pin for Single Phase AXG VR.
32	QRSETA	Single Phase AXG VR Quick Response Time Setting and Address Flipping Setting.
33	PWMA	PWM Output for Single Phase AXG VR.
34	EN	Voltage Regulator Enabler.
35	VR_RDY	Power Ready Indicator of Multi-Phase CORE VR.
36	VCC5	Chip Power. Connect this pin to GND by a ceramic cap larger than 1μF.
37	OCSETA	Single Phase AXG VR Over Current Protection Setting. Connect a resistor voltage divider from VCC to ground, the joint of the resistor divider is connected to OCSETA pin, with a voltage V_{OCSETA}, to set the over current threshold I_{LIMIT_AXG}.
38	OCSET	Multi-Phase CORE VR Over Current Protection Setting. Connect a resistor voltage divider from VCC to ground, the joint of the resistor divider is connected to OCSET pin, with a voltage V_{OCSET}, to set the over current threshold I_{LIMIT_CORE}.
39	TSENA	Thermal Monitor Sense Point of AXG VR.
40	TSEN	Thermal Monitor Sense Point of CORE VR.
41	$\overline{\text{VRHOT}}$	Thermal Monitor Output (Active Low).
42	TONSETA	Single Phase AXG VR On-time Setting. Connect this pin to VIN with one resistor to set ripple size in PWM-mode.
43	TONSET	Multi-Phase CORE VR On-time Setting. Connect this pin to VIN with one resistor to set ripple size in PWM-mode.
48	VCC12	Driver Power. Connect this pin to GND by a ceramic cap larger than 1μF.

Pin No.	Pin Name	Pin Function
49, 53, 47	LGATE [1:3]	Low Side Drive Output. This pin drives the gate of low side MOSFET.
50, 54, 46	PHASE [1:3]	Switch node of High Side Driver. Connect the pin to high side MOSFET source together with the low side MOSFET drain and the inductor.
51, 55, 45	UGATE [1:3]	High Side Drive Output. Connect the pin to the gate of high side MOSFET.
52, 56, 44	BOOT [1:3]	Bootstrap Power Pin. This pin powers high side MOSFET driver.
57 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

PWM CMP

Generate a signal to trigger Ton pulse.

TON GEN

Generate the PWM1 to PWM4 sequentially according to the phase control signal from the Loop control protection logic.

Control and Protection Logic

Execute the command from CPU.

The control logic also generates the digital code of the VID.

Control the power on sequence

Control the protection behavior.

Control the operational phase number.

Current Balance

Generate the signal to control Ton to achieve current balance.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the DVD and VCC voltage and issue POR signal as they are large enough.

DAC

Generate a analog signal according to the digital code generated by Control Logic.

Soft-Start and Slew Rate Control

Control the Dynamic VID slew rate of V_{SET} according to the SetVID fast or SetVID slow.

3-PHASE Driver

Generate UGATE [1:3] and LGATE [1:3] signal by PWM [1:3] signal.

Table 1. VR12 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
0	0	1	0	1	0	0	0	2	8	0.445
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage (V)
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Table 2. Serial VID Command

Code	Commands	Master Payload Contents	Slave Payload Contents	Description
00h	Not Supported	N/A	N/A	N/A
01h	SetVID_Fast	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “fast” slew rate 12.5mV/μs.
02h	SetVID_Slow	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “slow” slew rate 3.125mV/μs.
03h	SetVID_Decay	VID code	N/A	Set new target VID code, VR jumps to new VID target, but does not control the slew rate. The output voltage decays at a rate proportional to the load current
04h	SetPS	Byte indicating power states	N/A	Set power state
05h	SetRegADR	Pointer of registers in data table	N/A	Set the pointer of the data register
06h	SetRegDAT	New data register content	N/A	Write the contents to the data register
07h	GetReg	Pointer of registers in data table	Specified register contents	Slave returns the contents of the specified register as the payload.
08h - 1Fh	Not Supported	N/A	N/A	N/A

Table 3. SVID Data and Configuration Register

Index	Register Name	Description	Access	Default
00h	Vendor_ID	Vendor ID	RO	1Eh
01h	Product_ID	Product ID	RO	5Bh
02h	Product_Revision	Product Revision	RO	01h
05h	Protocol_Version	SVID Protocol version	RO	01h
06h	VR_Capability	Bit mapped register, identifies the SVID VR Capabilities and which of the optional telemetry registers is supported.	RO	81h
10h	Status_1	Data register containing the status of VR	R-M, W-PWM	00h
11h	Status_2	Data register containing the status of transmission.	R-M, W-PWM	00h
12h	Temperature_Zone	Data register showing temperature Zone that has been entered.	R-M, W-PWM	00h
15h	Output_Current	Data register showing direct ADC conversion of output current, scaled to ICC_MAX = ADC full range. Binary format (IE : 64h = 100/255 ICC_MAX)	R-M, W-PWM	00h
1Ch	Status_2_Lastread	The register contains a copy of the Status_2	R-M, W-PWM	00h
21h	ICC_Max	Data register containing the maximum ICC the platform supports. Binary format in A. (IE : 64h = 100A)	RO, Platform	N/A
22h	Temp_Max	Data register containing the maximum temperature the platform supports. Binary format in °C. (IE : 64h = 100°C) Not supported by AXG VR.	RO, Platform	N/A
24h	SR_fast	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/μs. (IE : 0Ah = 10mV/μs)	RO	0Ah
25h	SR_slow	Data register containing the capability of slow slew rate. Binary format in mV/μs. (IE : 02h = 2mV/μs)	RO	02h
30h	VOUT_Max	The register is programmed by the master and sets the maximum VID.	RW, Master	FBh
31h	VID_Setting	Data register containing currently programmed VID	RW, Master	00h
32h	Power_State	Register containing the current programmed power state	RW, Master	00h
33h	Offset	Set offset in VID steps	RW, Master	00h
34h	Multi_VR_Config	Bit mapped data register which configures multiple VRs' behavior on the same bus	RW, Master	00h
35h	Pointer	Scratch pad register for temporary storage of the SetRegADR pointer register	RW, Master	30h

Notes :
RO = Read Only
RW = Read/Write
R-M = Read by Master
W-PWM = Write by PWM only
Platform = programmed by platform
Master = programmed by the master
PWM = programmed by the VR control IC

Absolute Maximum Ratings (Note 1)

- VCC12 to GND ---------- –0.3V to 15V
- VCC5 to GND ---------- –0.3V to 6.5V
- RGND, RGNDA to GND ---------- –0.3V to 0.3V
- TONSET, TONSETA to GND ---------- –0.3V to 28V
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –10V to 35V
- LGATEx to GND
  - DC ---------- (GND – 0.3V) to (VCC12 + 0.3V)
  - <20ns ---------- (GND – 2V) to (VCC12 + 0.3V)
- UGATEx to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - <20ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- PWMA to GND ---------- –0.3V to 7V
- Other Pins ---------- –0.3V to (VCC5 + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–56L 7x7 ---------- 3.226W
- Package Thermal Resistance (Note 2)
  - WQFN–56L 7x7, θ_{JA} ---------- 31°C/W
  - WQFN–56L 7x7, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC12 ---------- 4.5V to 13.2V
- Supply Voltage, VCC5 ---------- 4.5V to 5.5V
- Input Voltage, (V_{IN} + VCC12) ---------- <35V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC5} = 5V, V_{CC12} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
VCC12 Supply Voltage	V_{CC12}		4.5	--	13.2	V
VCC5 Supply Voltage	V_{CC5}		4.5	5	5.5	V
VCC12 Supply Current	I_{VCC12}	V_{CC12} = 12V, V_{BOOTx} = 12V	--	1.2	--	mA
VCC5 Supply Current	I_{VCC5}	EN = 1.05V, Not Switching	--	12	20	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	--	5	μA
Power On Reset (POR)						
POR Threshold	V_{POR_r}	V_{CC12} Rising	3	--	4.4	V
POR Hysteresis	V_{POR_HYS}		--	0.5	--	V
Reference and DAC						
DC Accuracy		V_{DAC} = 1.000 to 1.520 (No Load, Active Mode)	–0.5	0	0.5	%VID
		V_{DAC} = 0.800 to 1.000	–5	0	5	mV
		V_{DAC} = 0.500 to 0.800	–8	0	8	
		V_{DAC} = 0.250 to 0.500	–8	0	8	
RGND Current						
RGND Current	I_{RGND}	EN = 1.05V, Not Switching	--	--	500	μA
Slew Rate						
Dynamic VID Slew Rate		SetVID Slow	2.5	3.125	3.75	mV/μs
		SetVID Fast	10	12.5	15	mV/μs
Error Amplifier						
DC Gain		R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF (gain = –4, R_F = 47k, V_{OUT} = 0.5V – 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.3	--	3.6	V
MAX Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	250	--	μA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–0.75	--	0.75	mV
Impedance at Neg. Input	R_{ISENxN}		1	--	--	mΩ
Impedance at Pos. Input	R_{ISENxP}		1	--	--	mΩ
DC Gain		CORE VR	--	10	--	V/V
		AXG VR	--	20	--	V/V
Input Range	V_{ISEN_in}		–50	--	100	mV
V_{ISEN} Linearity	V_{ISEN_ACC}	–30mV < V_{ISEN_in} < 50mV	–1	--	1	%
Ton Setting						
TONSET/TONSETA pin Voltage	V_{Ton}	I_{RTON} = 80μA, V_{DAC} = 0.75V	--	0.75	--	V
CCM On-time Setting	T_{ON}	I_{RTON} = 80μA, PS0, PS1	275	305	335	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TONSET/TONSETA Input Current Range	I_{RTON}		25	--	280	μA
Ton in PS2 (CORE Only)	$T_{ON\ ps2}$	With Respect to PS0 Ton	--	85	--	%
Minimum Off-Time	T_{OFF_MIN}		--	250	--	ns
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6k	2.09	2.14	2.19	V
QRSET/QRSETA						
Quick Response Tonx	T_{ONx_QR}	V_{DAC} = 0.75V, Q_{RSET} = 1.2V, I_{RTON} = 80μA	--	305	--	ns
QRSET Source Current	I_{QRSET}	Before POR	--	80	--	μA
$V_{INITIAL}$ Threshold	V_{IH}		V_{CC5} – 0.5	--	--	V
	V_{IL}		--	--	V_{CC5} – 1.8	V
Non-flipping ADDR Threshold	V_{IH}		V_{CC5} – 0.5	--	--	V
	V_{IL}		--	--	V_{CC5} – 1.8	V
OFS/OFSA Function						
OFS Enable/Disable Threshold Voltage	V_{EN_OFS}	V_{OFS} > V_{EN_OFS} before EN rising	0.52	1.2	--	V
Set OFS/OFSA Voltage		V_{ID} = 1V, offset +400mV	1.58	1.6	1.62	V
		V_{ID} = 1V, offset –200mV	0.98	1	1.02	
		V_{ID} = 1V. No Offset Voltage	1.19	1.2	1.21	
Impedance	R_{OFS}		1	--	--	MΩ
RSET Setting						
RSET Voltage	V_{RSET}	V_{DAC} = 1V	--	1.000	--	V
Zero Current Detection						
Zero Current Detection Threshold	V_{ZCD}	ISEN1P – ISEN1N, ISENAP – ISENAN	--	1	--	mV
Protection						
Under Voltage Lockout (UVLO) Threshold	V_{UVLO}	Falling edge, 100mV Hysteresis	4.04	4.24	4.44	V
Absolute Over Voltage Protection Threshold	V_{OVABS}	With Respect to $V_{OUT(MAX)}$, pin offset is disabled	100	150	200	mV
Delay of UVLO	t_{UVLO}	Rising above Threshold	--	3	--	μs
Delay of OVP	t_{OV}	ISEN1N/ISENAN Rising above Threshold	--	1	--	μs
Under Voltage Protection (UVP) Threshold	V_{UV}	Measured at ISEN1N/ISENAN with respect to unloaded output voltage (UOV) (for 0.8V < UOV < 1.52V)	–350	–300	–250	mV
Delay of UVP	t_{UV}	ISEN1N/ISENAN Falling below Threshold	--	3	--	μs
Negative Voltage Protection Threshold	V_{NV}		–100	–50	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay of NVP	t_{NV}	ISEN1N/ISENAN Falling below Threshold	--	1	--	µs
Current Limit Threshold Voltage (Per Phase)		G_{ILIMT} = V_{OCSET} / (V_{ISENxP} – V_{ISENxN}) V_{OCSET} = 2.4V, (V_{ISENxP} – V_{ISENxN}) = 50mV	43.2	48	52.8	V/V
		G_{ILIMT} = V_{OCSETA} / (V_{ISENAP} –V_{ISENAN}) V_{OCSETA} = 2.4V, (V_{ISENAP} – V_{ISENAN}) = 25mV	86.4	96	105.6	
Current limit latch Counter (per phase)	N_{ILIMIT}	Continuous Current Limit Cycle	--	15	--	times
Logic Inputs						
EN Threshold Voltage	V_{IH_EN}		0.7	--	--	V
	V_{IL_EN}		--	--	0.3	
EN Hysteresis	V_{ENHYS}		--	30	--	mV
Leakage Current of EN	I_{EN}		–1	--	1	µA
VCLK, VDIO Threshold Voltage	V_{IH}		0.665	--	--	V
	V_{IL}		--	--	0.367	
VCLK, VDIO Hysteresis	V_{HYS}		--	70	--	mV
Leakage Current of VCLK, VDIO	I_{LEAK_IN}		–1	--	1	µA
$\overline{\text{ALERT}}$						
$\overline{\text{ALERT}}$ Low Voltage	$V_{\overline{ALERT}}$	$I_{\overline{ALERT}}$ = 4mA	--	--	0.4	V
Power On Sequence						
SVID Ready Delay Time	t_A	From EN to VR Controller is ready to accept SVID command	--	--	2	ms
VR Ready Trip Threshold	$V_{TH\_VR\_RDY}$	ISEN1N – 1st V_{DAC}	--	–100	--	mV
VR_RDY Low Voltage	V_{VR_RDY}	I_{VR_RDY} = 4mA	--	--	0.4	V
VR_RDY Delay	t_{VR_RDY}	ISEN1N = $V_{INITIAL}$ to VR_RDY high	--	100	--	µs
Thermal Throttling						
$\overline{\text{VRHOT}}$ Output Voltage	$V_{\overline{VRHOT}}$	$I_{\overline{VRHOT}}$ = 40mA	--	--	0.4	V
Current Monitor						
Current Monitor Maximum Output Voltage in Operating Range	V_{IMON}	V_{DAC} = 1V, $V_{RIMONFB}$ = 100mV, R_{IMONFB} = 10kΩ, R_{IMON} = 330kΩ	3.2	3.3	3.4	V
High Impedance Output						
Leakage Current of $\overline{\text{ALERT}}$, VR_RDY and $\overline{\text{VRHOT}}$ Pins	I_{LEAK_OUT}		–1	--	1	µA
SVID						
SVID Frequency	$f_{SVIDfreq}$		5	25	26.25	MHz
SVID Clock To Data Delay	t_{CO}		4	--	8.3	ns
Setup Time Of VDIO	t_{SU}		7	--	--	ns
Hold Time Of VDIO	t_{HLD}		14	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC						
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 12.74% x VCC5	29	32	35	decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 25.284% x VCC5	61	64	67	
	$C_{ICCMAX3}$	V_{ICCMAX} = 50.372% x VCC5	125	128	131	
Digital Code of ICCMAXA	$C_{ICCMAXA1}$	$V_{ICCMAXA}$ = 3.332% x VCC5	5	8	11	decimal
	$C_{ICCMAXA2}$	$V_{ICCMAXA}$ = 6.468% x VCC5	13	16	19	
	$C_{ICCMAXA3}$	$V_{ICCMAXA}$ = 12.74% x VCC5	29	32	35	
Digital Code of TEMPMAX	$C_{TEMPMAX1}$	$V_{TEMPMAX}$ = 33.516% x VCC5	82	85	88	decimal
	$C_{TEMPMAX2}$	$V_{TEMPMAX}$ = 39.396% x VCC5	97	100	103	
	$C_{TEMPMAX3}$	$V_{TEMPMAX}$ = 49.196% x VCC5	122	125	128	
Digital Code of Output Current Report	C_{OCR1}	$V_{IMONA} = V_{IMONA}$ = 3.3V	252	255	255	decimal
	C_{OCR2}	$V_{IMONA} = V_{IMONA}$ = 2.208V	167	170	173	
	C_{OCR3}	$V_{IMONA} = V_{IMONA}$ = 1.107V	82	85	88	
Updating Period of Output Current Report	t_{OCR}		--	--	500	μs
Tolerance Band of Temp. Zone Trip Points b7, b6, b5	t_{TSEN_TOL}		20	--	20	mV
Updating Period of Temperature Zone	t_{TZ}		--	--	500	μs
Timing						
UGATE Rise Time	t_{UGATEr}	3nF load	--	25	--	ns
UGATE Fall Time	t_{UGATEf}	3nF load	--	12	--	ns
LGATE Rise Time	t_{LGATEr}	3nF load	--	24	--	ns
LGATE Fall Time	t_{LGATEf}	3nF load	--	10	--	ns
Propagation Delay	$t_{UGATEpgh}$		--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
	$t_{LGATEpdh}$		--	20	--	
	$t_{LGATEpdl}$		--	8	--	
Output						
UGATE Drive Source Current	$I_{UGATEsr}$	$V_{BOOTx} - V_{PHASEx}$ = 12V, $V_{UGATEx} - V_{PHASEx}$ = 2V	--	2	--	A
UGATE Drive Sink Resistance	$R_{UGATEsk}$	$V_{BOOTx} - V_{PHASEx}$ = 12V	--	1.4	--	Ω
LGATE Drive Source Current	$I_{LGATEsr}$	V_{LGATEx} = 2V	--	2.2	--	A
LGATE Drive Sink Resistance	$R_{LGATEsk}$		--	1.1	--	Ω
UGATE Drive Source	$I_{UGATEsr}$	$V_{BOOTx} - V_{PHASEx}$ = 12V, $V_{UGATEx} - V_{PHASEx}$ = 2V	--	2	--	A
DVID, DVIDA, ICCMAX, ICCMAXA and TEMPMAX						
Current Sourcing Out from DVIDx Pin to GND	I_{DVIDx}	During dynamic VID fast event	6	8	10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sinking in from 5V to ICCMAX Pin	I_{CCMAX}	After EN	--	16	--	μA
Current Sinking in from 5V to ICCMAXA Pin	I_{CCMAXA}	After EN	--	128	--	μA
Current Sinking in from 5V to TEMPMAX Pin	$I_{TEMPMAX}$	After EN	--	16	--	μA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

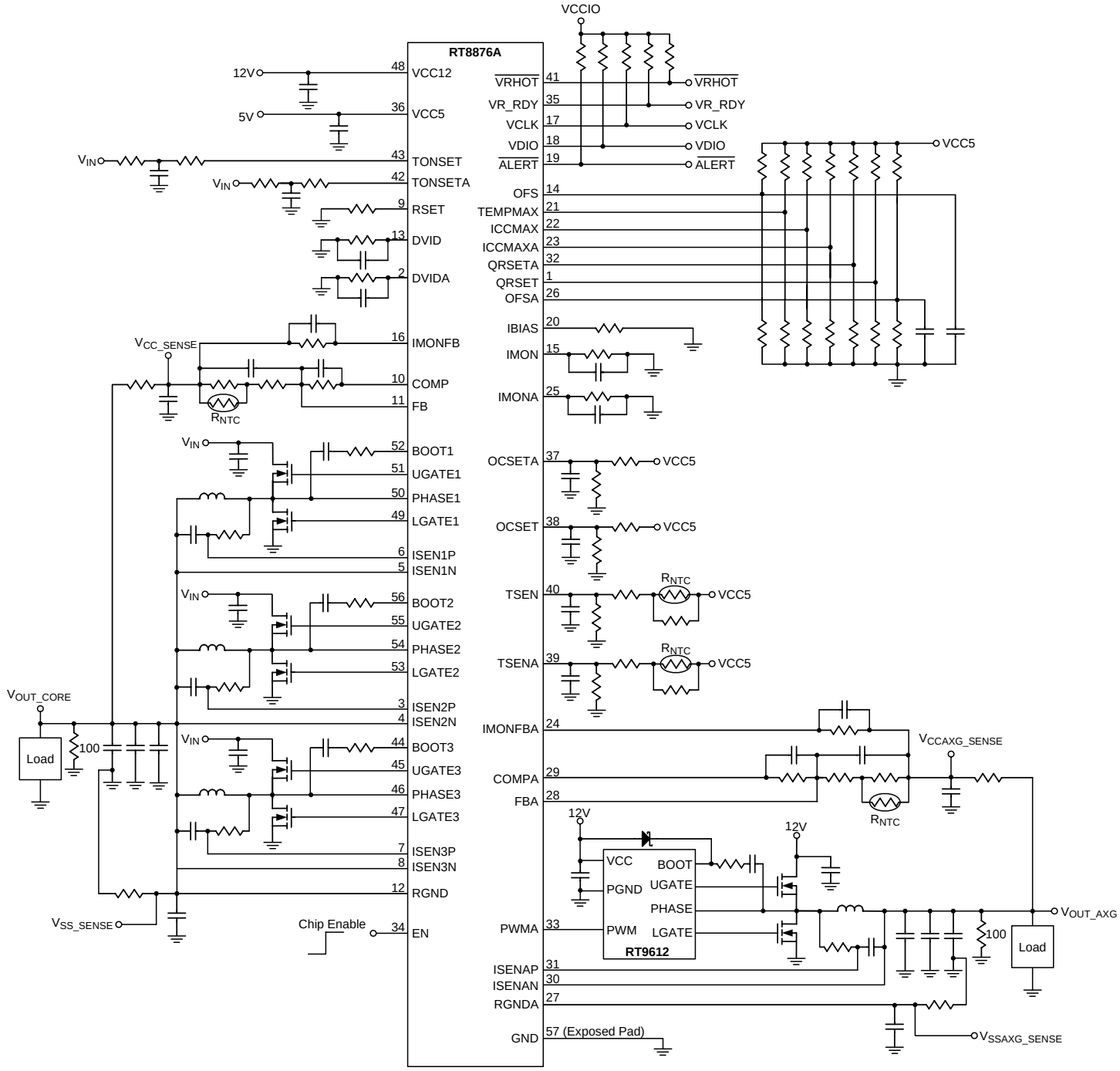


Figure 1. Thernal Compersation at Voltage Loop for AXG VR

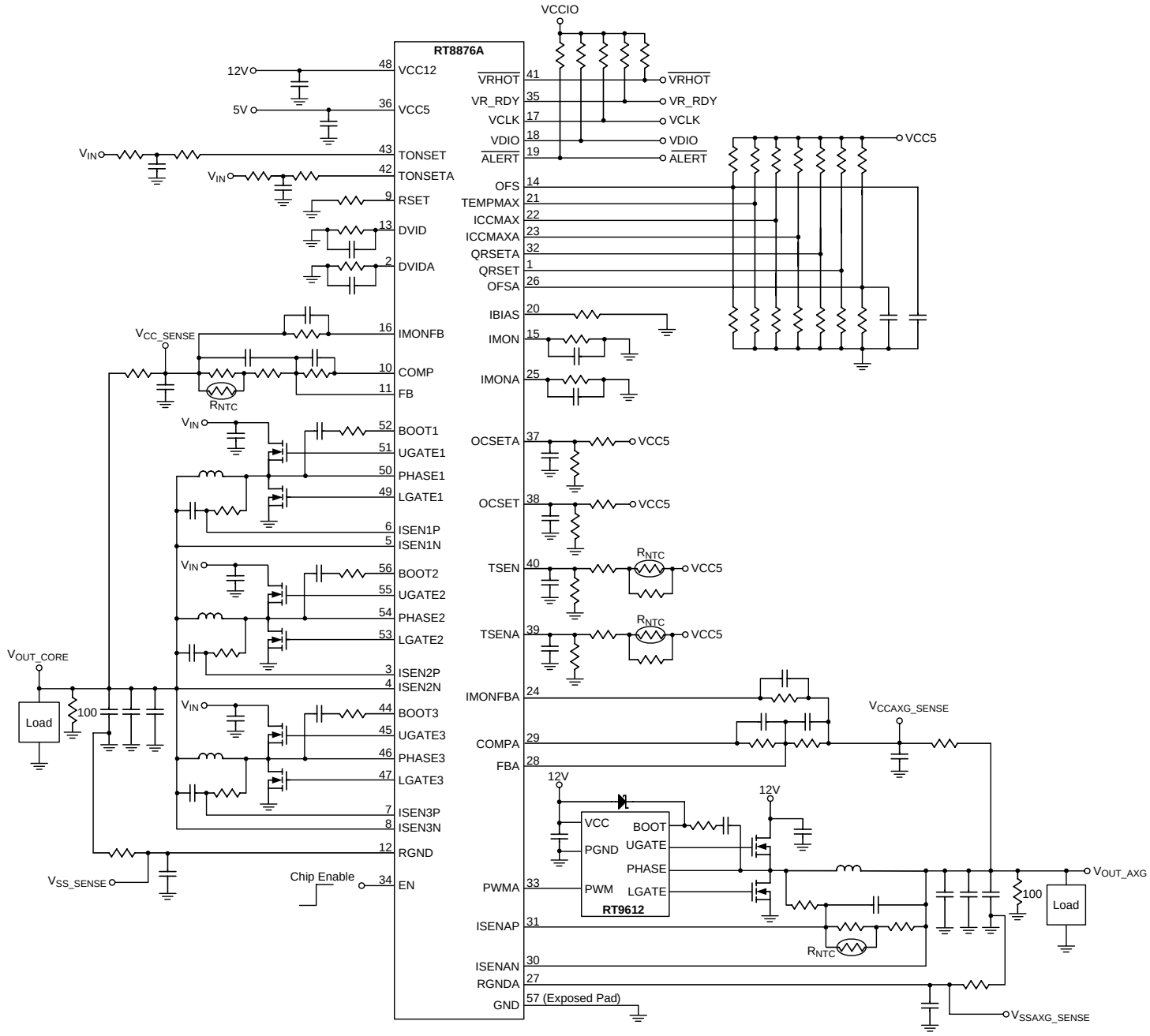


Figure 2. Thernal Compersation at Current Loop for AXG VR

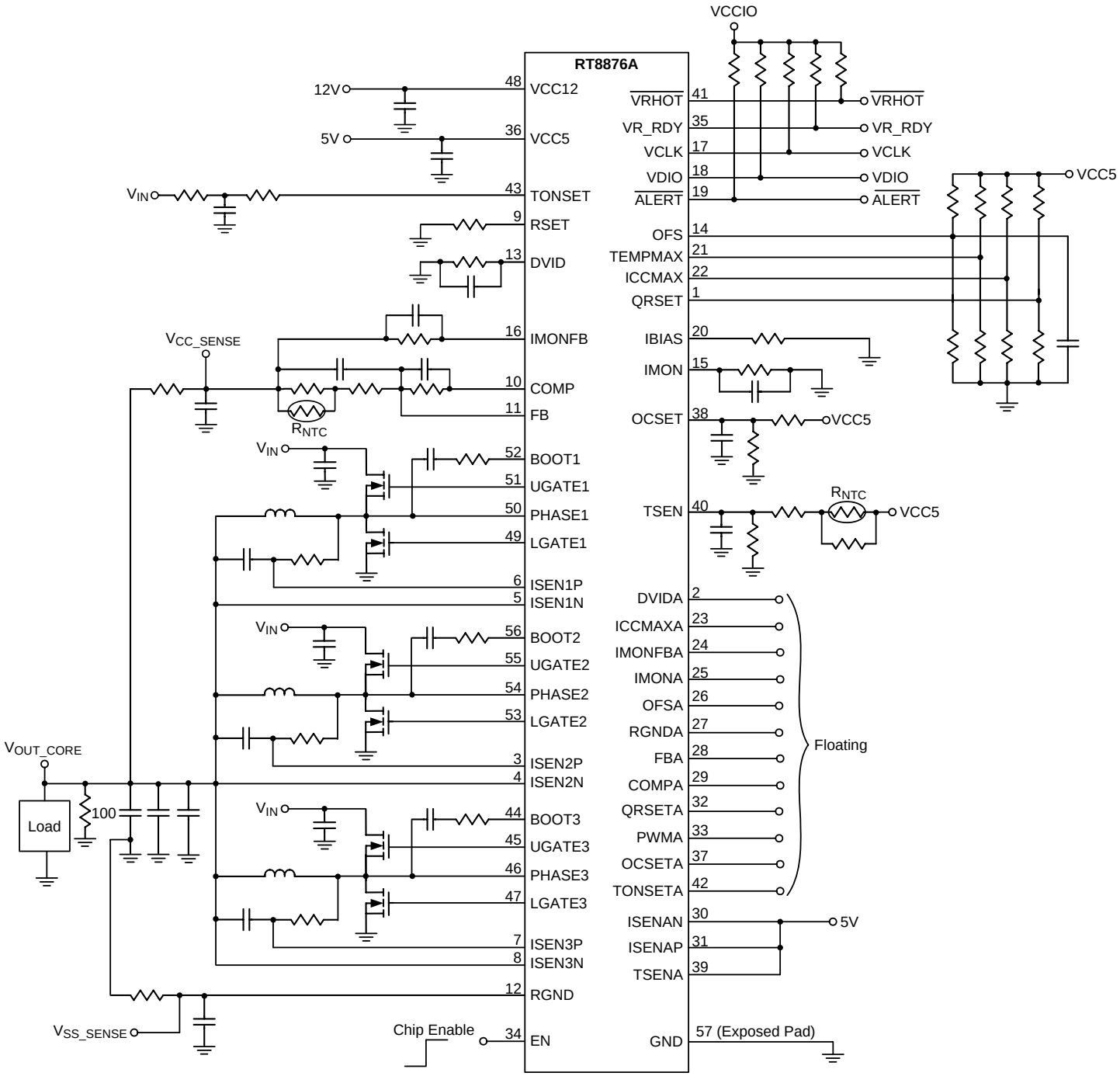
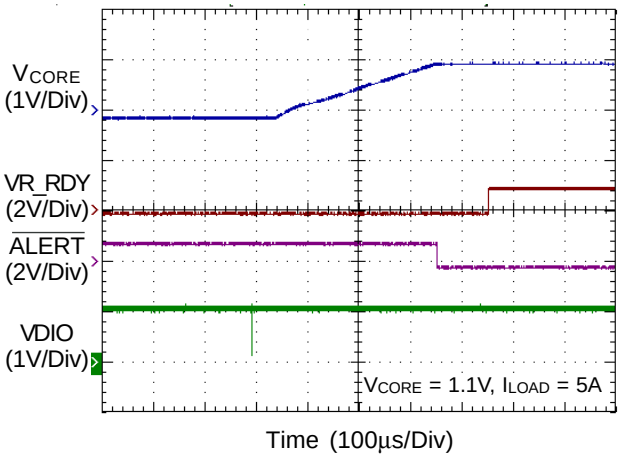


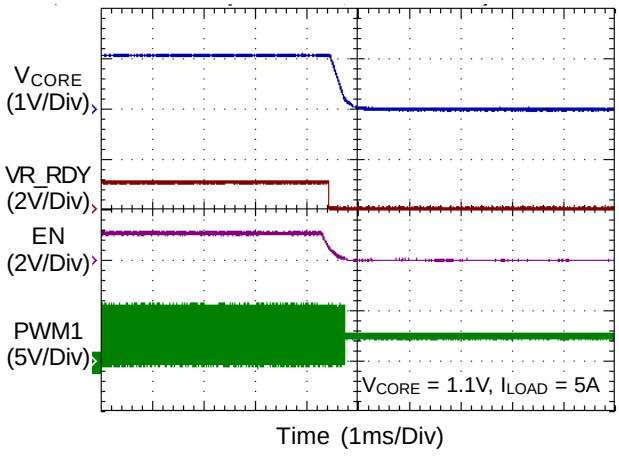
Figure 3. Application Circuit for AXG VR Being Disabled

Typical Operating Characteristics

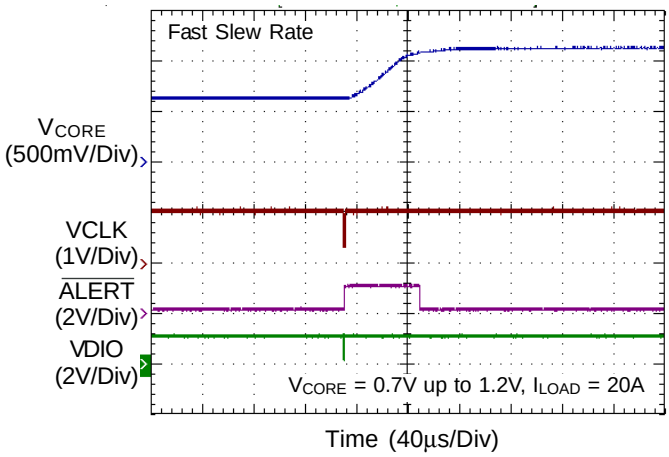
CORE VR Power On



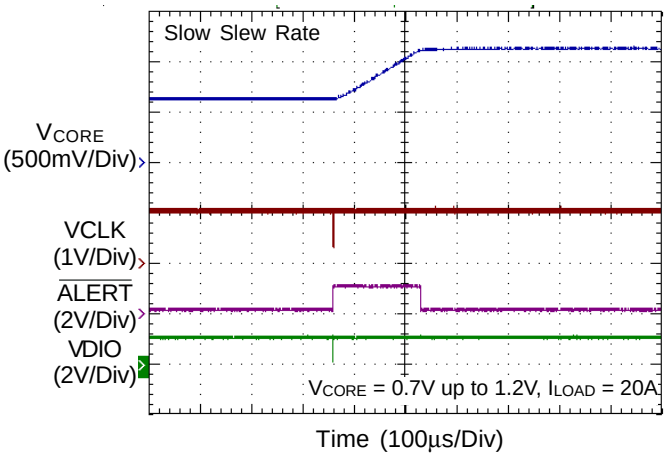
CORE VR Power Off from EN



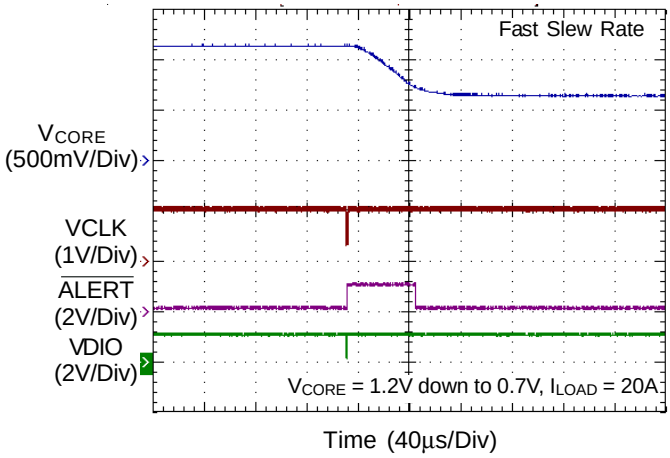
CORE VR Dynamic VID Up



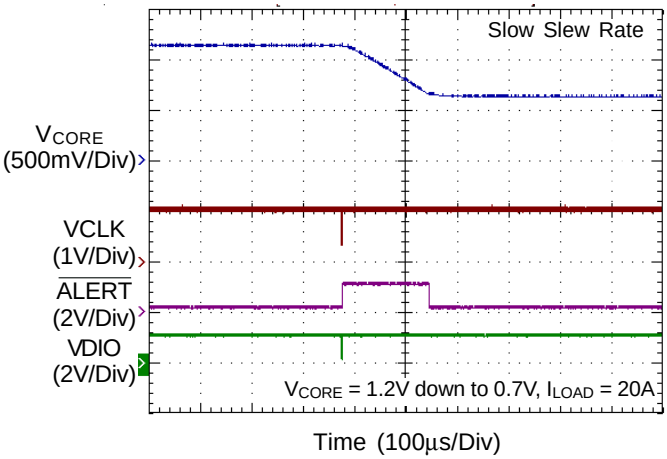
CORE VR Dynamic VID Up



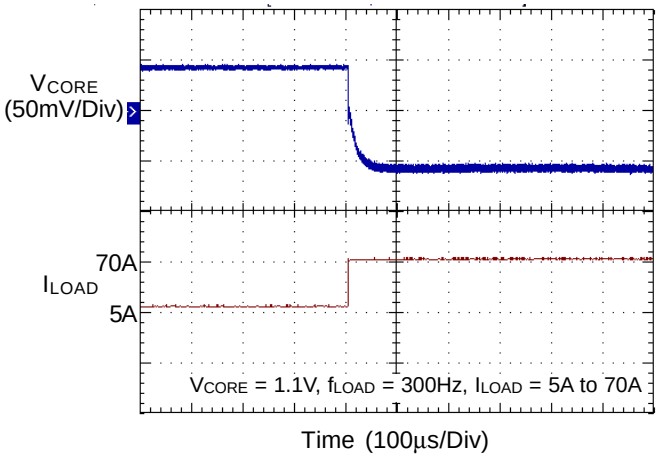
CORE VR Dynamic VID Down



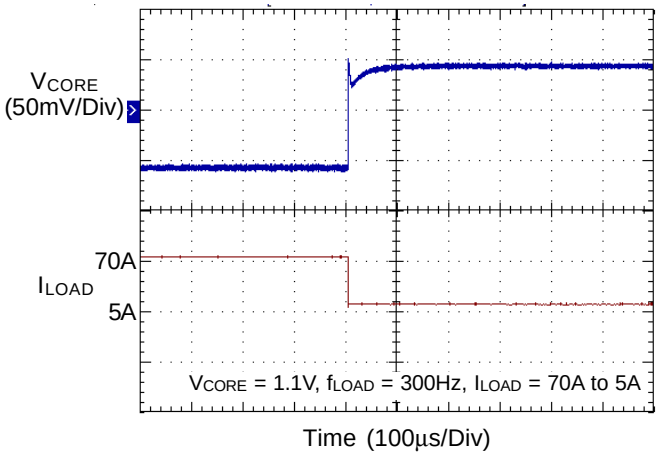
CORE VR Dynamic VID Down



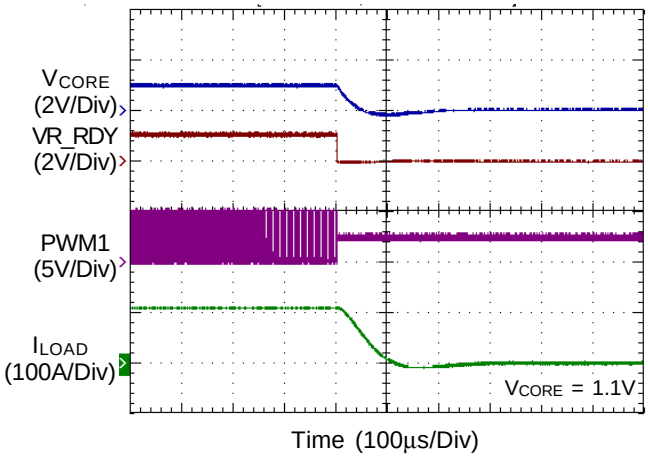
CORE VR Load Transient Response



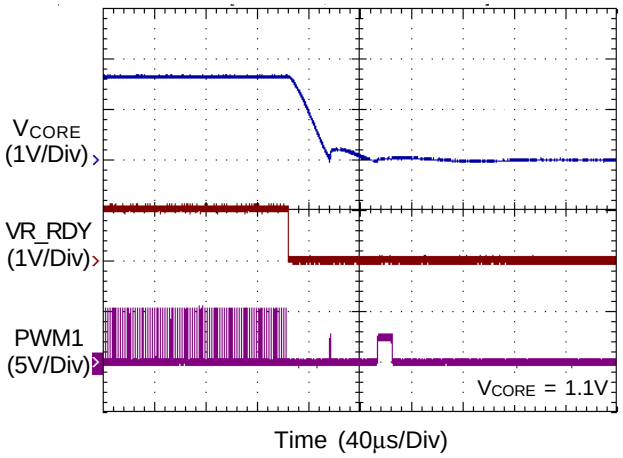
CORE VR Load Transient Response



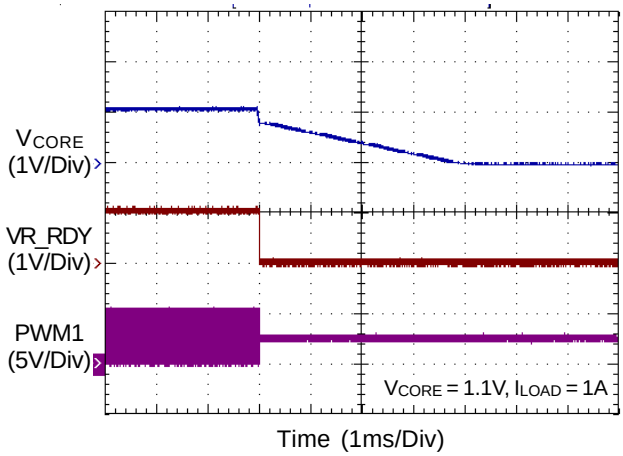
CORE VR OCP



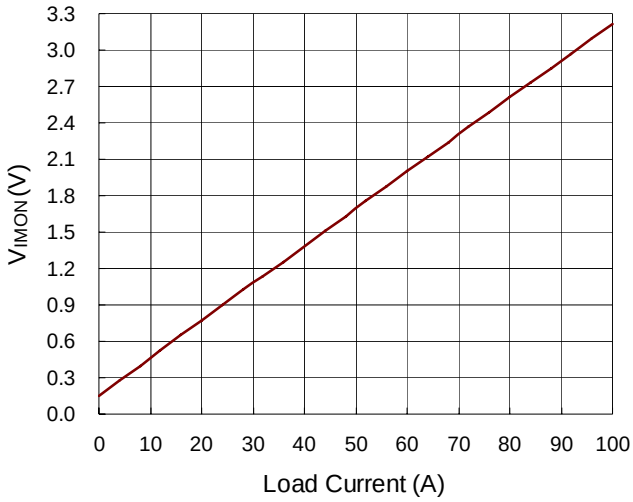
CORE VR OVP & NVP



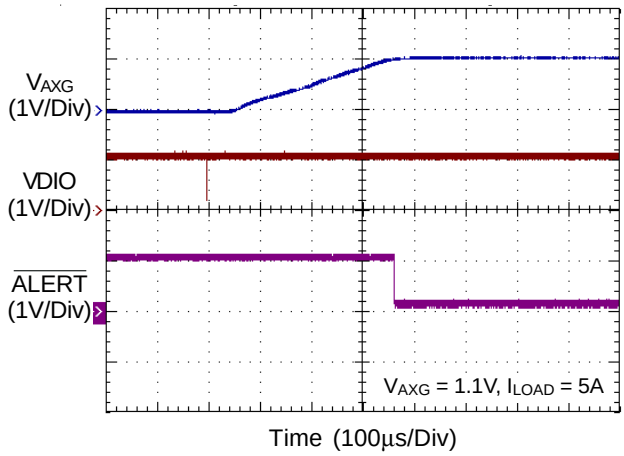
CORE VR UVP



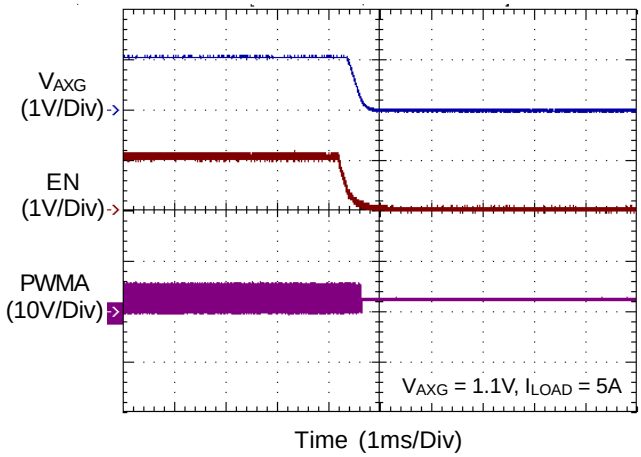
V_{IMON} vs. Load Current



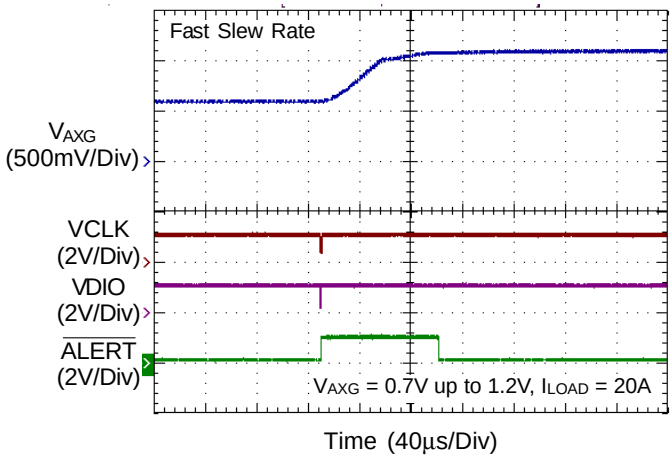
AXG VR Power On



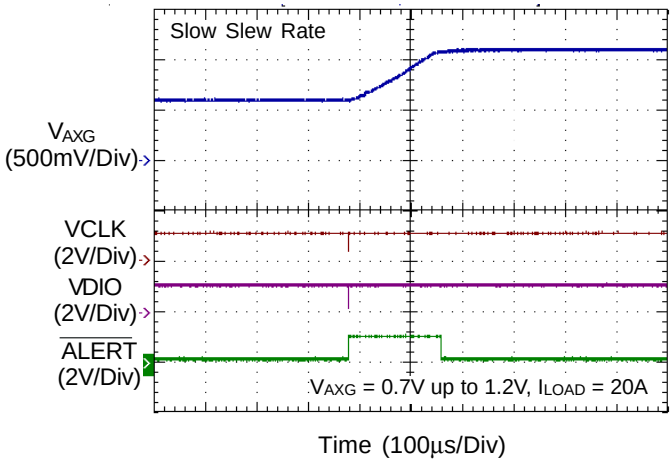
AXG VR Power Off from EN



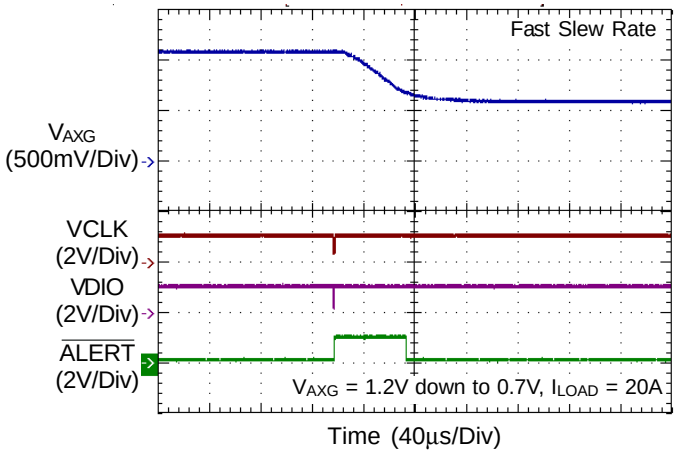
AXG VR Dynamic VID Up



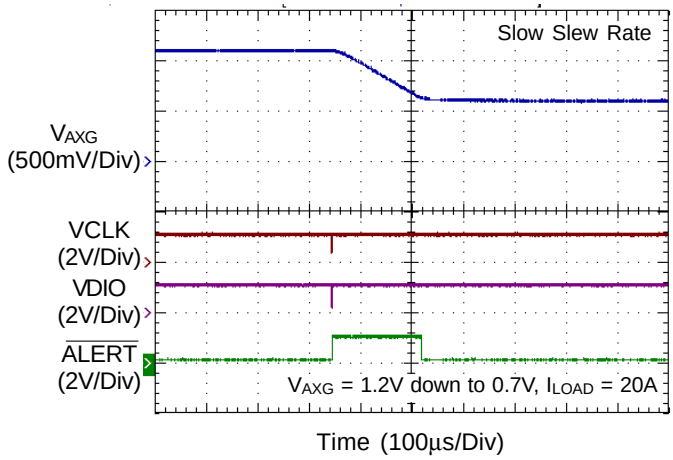
AXG VR Dynamic VID Up



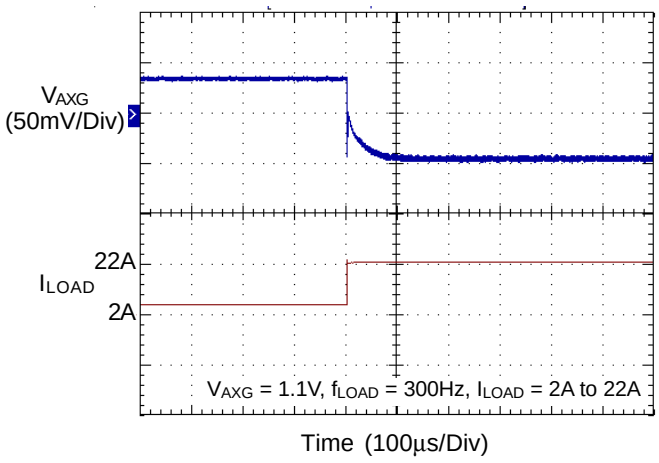
AXG VR Dynamic VID Down



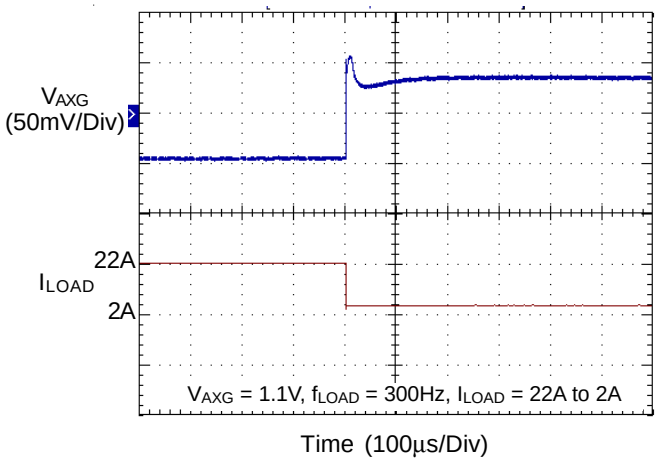
AXG VR Dynamic VID Down



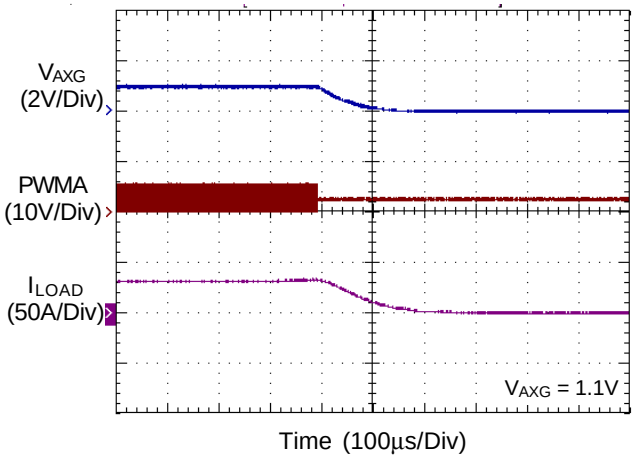
AXG VR Load Transient Response



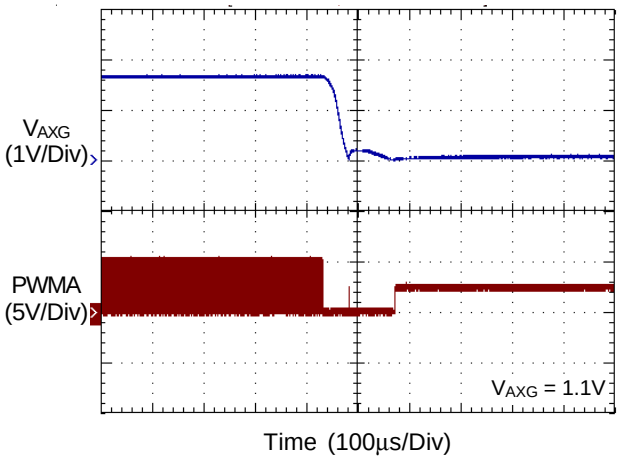
AXG VR Load Transient Response



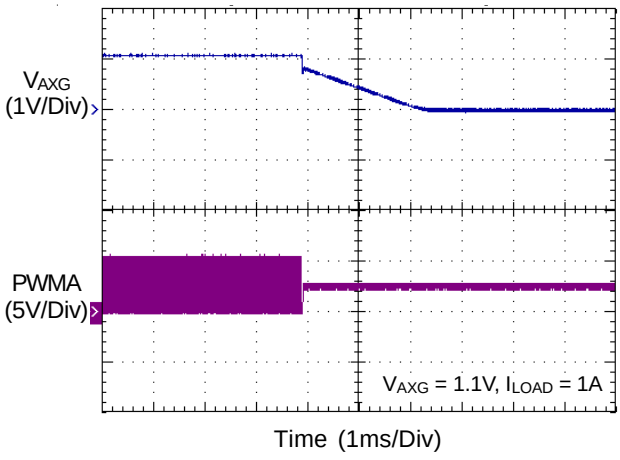
AXG VR OCP



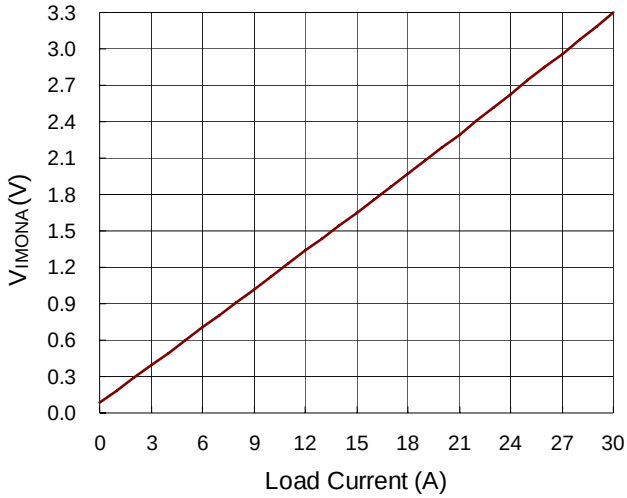
AXG VR OVP & NVP



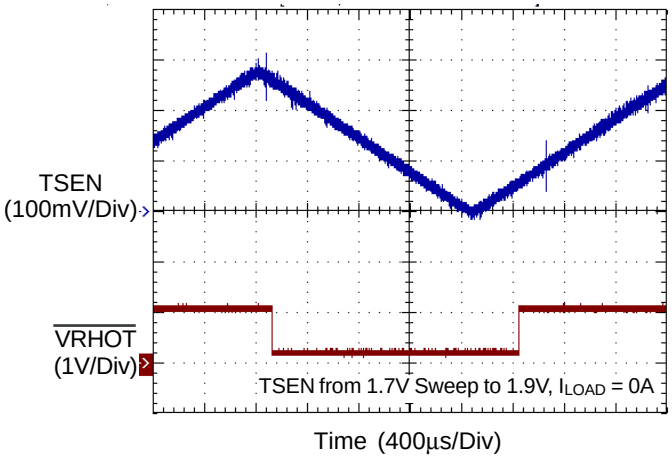
AXG VR UVP



VIMONA vs. Load Current



Thermal Monitoring



Application Information

The RT8876A is a CPU power controller which includes two channels : a 3/2/1 phase synchronous Buck controller with three integrated drivers for CORE VR, and a single phase Buck controller for AXG VR. The RT8876A is compliant with Intel VR12/IMVP7 voltage regulator specification to fulfill Intel's CPU power supply requirements of both CORE and AXG voltage regulators. A Serial VID (SVID) interface is built-in in the RT8876A to communicate with Intel VR12/IMVP7 compliant CPU. The RT8876A adopts G-NAVP™ (Green Native Adaptive Voltage Positioning), which is Richtek's proprietary topology derived from finite DC gain EA amplifier with current mode control, making it an easy setting PWM controller, meeting all Intel CPU requirements of AVP. The load line can be easily programmed by setting the DC gain of the error amplifier. The RT8876A has fast transient response because of the G-NAVP™ commanding variable switching frequency. Based on the G-NAVP™ topology, the RT8876A also features a quick response mechanism so that fully phases can respond for optimized AVP performance during load transient. The G-NAVP™ topology also represents a high efficiency system with green power concept. With the G-NAVP™ topology, the RT8876A is also a green power controller with high efficiency under heavy load, light load, and very light load conditions. The RT8876A supports mode transition function with various operating states, including multi-phase, single phase and DEM (Diode Emulation Modes). These different operating states allow the overall power control system to have the lowest power loss. By utilizing the G-NAVP™ topology, the operating frequency of the RT8876A varies with VID, load, and input voltage to further enhance the efficiency even in CCM. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT8876A supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. The RT8876A also builds in a high accuracy ADC for some platform setting functions, such as no-load offset or over current level. The controller supports both DCR and sense resistor current sensing. The RT8876A provides power VR ready signals for both CORE VR and AXG VR. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8876A is available in a WQFN-56L 7x7 small footprint package.

General Loop Functions :

Power Ready (POR) Detection

During start-up, the RT8876A will detect the voltage at the voltage input pins : VCC5, VCC12 and EN. When VCC5 > 4.24V and VCC12 > 4V, the RT8876A will recognize the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT8876A will enter start-up sequence for both CORE rail and AXG rail. If the voltage at any voltage pin drops below low threshold (POR = low), the RT8876A will enter power down sequence and all the functions will be disabled. Normally, connecting system V_{TT} (1.05V) to the EN pin and power stage V_{IN} (12V) to the VCC12 pin is recommended. 2ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only after POR = low. The condition of V_{EN} = low will not clear these latches.

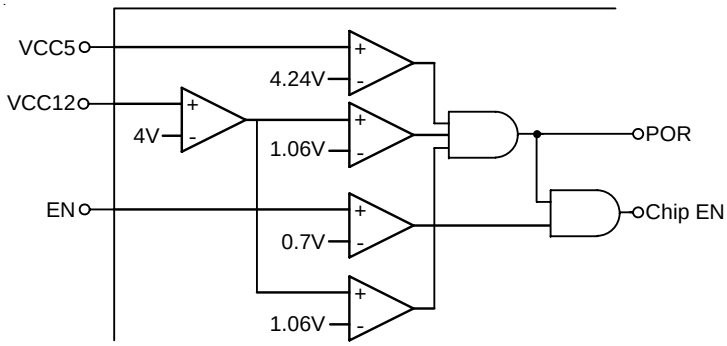


Figure 4. Power Ready (POR) Detection

Precise Reference Current Generation

The RT8876A includes complicated analog circuits inside the controller. These analog circuits need very precise reference voltage/current to drive these analog devices. The RT8876A will auto generate a 2.14V voltage source at the IBIAS pin, and a 53.6kΩ resistor is required to be connected between IBIAS and analog ground. Through this connection, the RT8876A will generate a 40μA current from the IBIAS pin to analog ground, and this 40μA current

will be mirrored inside the RT8876A for internal use. Note that other types of connection or other values of resistance applied at the IBIAS pin may cause failure of the RT8876A's functions, such as slew rate control, OFS accuracy, etc. In other words, the IBIAS pin can only be connected with a 53.6kΩ resistor to GND. The resistance accuracy of this resistor is recommended to be 1% or higher.

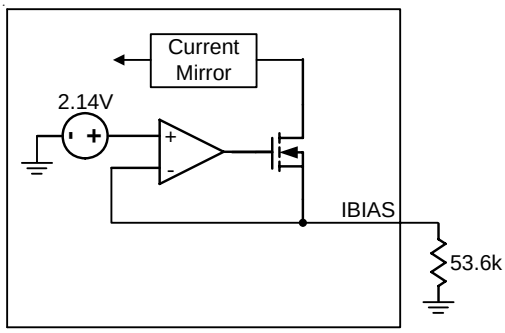


Figure 5. IBIAS Setting

ICCMAX, ICCMAXA and TEMPMAX

The RT8876A provides ICCMAX, ICCMAXA and TEMPMAX pins for platform users to set the maximum level of output current or VR temperature : ICCMAX for CORE VR max current, ICCMAXA for AXG VR max current, and TEMPMAX for CORE VR max temperature. To set ICCMAX, ICCMAXA and TEMPMAX platform designers should use resistive voltage divider on these three pins. The current of the divider should be several milliamps to avoid noise effect. The 3 items share the same algorithms : the ADC divides 5V into 255 levels. Therefore, the LSB = 5 / 255 = 19.6mV, which means 19.6mV applied to ICCMAX pin equals to 1A setting. For example, if the maximum level of temperature is desired to be 120°C, the voltage applied to TEMPMAX should be 120 x 19.6mV = 2.352V. The ADC circuit inside these three pins will decode the voltage applied and store the maximum current/temperature setting into ICC_Max and Temp_Max registers. The ADC monitors and decodes the voltage at these three pins only ONCE after power up. After ADC decoding (only once), a 128μA current will be generated at the ICCMAXA pin for internal use. Make sure the voltage at the ICCMAXA pin is greater than 1.55V to guarantee proper functionality The RT8876A will NOT take any action even when the VR output current or temperature exceeds its maximum setting at these ADC pins. The maximum level settings at these ADC pins are different from over current protection or over temperature protection. In other words, these maximum level setting pins are only for platform users to define their system operating conditions and these messages will only be utilized by the CPU.

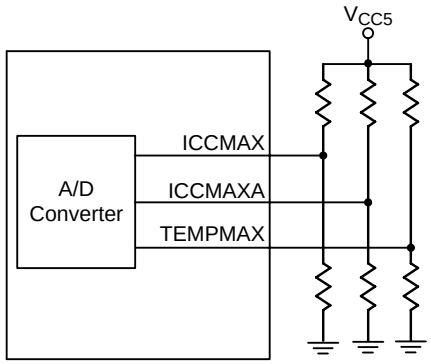


Figure 6. ADC Pins Setting

$V_{INITIAL}$ Setting

The VR's $V_{INITIAL}$ can be selected as 0V or 1.1V by QRSET pin. The connection of the QRSET pin is usually a voltage divider circuit which is described later in the Quick Response section in CORE rail part. Before POR, the RT8876A will source an 80μA current from the QRSET pin to the external voltage divider to determine the voltage level while the RT8876A is still not powered on. Before POR, if the voltage at the QRSET pin is higher than V_{CC5} – 0.5V, the $V_{INITIAL}$ will be 1.1V. If the voltage is lower than V_{CC5} – 1.8V, the $V_{INITIAL}$ will be 0V. For example, a 5V voltage divided by two 1kΩ resistors connected to the QRSET pin generates 2.54V (5V / 2 + 80μA x 1kΩ / 2) before POR and 2.5V (5V/2) after POR. So the $V_{INITIAL}$ will be 0V under this condition. Please note that the both Core rail and AXG rail are simultaneously set as $V_{INITIAL}$ = 1.1V or 0V.

VR Rail Addressing

The VR's address can be flipped by setting QRSETA pin. The connection of the QRSETA pin is usually a voltage divider circuit which is described later in the Quick Response section in AXG rail part. Before POR, the RT8876A will source an 80μA current from the QRSETA pin to the external voltage divider to determine the voltage level while the RT8876A is still not powered on. Before

POR, if the voltage at the QRSETA pin is lower than V_{CC5} – 1.8V, the address will be flipped, that is, VR0 (CORE) address is flipped from 0000 to 0001 and VR1 (AXG) address is flipped from 0001 to 0000. For example, a 5V voltage divided by two 1kΩ resistors connected to the QRSETA pin generates 2.54V (5V / 2 + 80μA x 1kΩ / 2) before POR and 2.5V (5V/2) after POR. So the address will be flipped under this condition.

Start-Up Sequence

The RT8876A utilizes an internal soft-start sequence which strictly follows Intel VR12/IMVP7 start-up sequence specifications. After POR = high and EN = high, the controller considers all the power inputs ready and enters start-up sequence. If $V_{INITIAL}$ = 0V, V_{OUT} is programmed to stay at 0V for 2ms waiting for SVID command. If $V_{INITIAL}$ = 1.1V, VOUT will ramp up to $V_{INITIAL}$ voltage (which is not zero) immediately after both POR = high and EN = high. After V_{OUT} reaches target $V_{INITIAL}$, V_{OUT} will stay at $V_{INITIAL}$ waiting for SVID command. After the RT8876A receives valid VID code (typically SetVID_Slow command), V_{OUT} will ramp up to the target voltage with specified slew rate (see section "Data and Configuration Register"). After V_{OUT} reaches target voltage (VID voltage for $V_{INITIAL}$ = 0V or $V_{INITIAL}$ for $V_{INITIAL}$ = 1.1V), the RT8876A will send out VR_RDY signal to indicate that the power state of the RT8876A is ready. The VR ready circuit is an open-drain structure, so a pull-up resistor connected to a voltage source is recommended.

Power Down Sequence

Similar to the start-up sequence, the RT8876A also utilizes a soft shutdown mechanism during turn-off. After EN = low, the internal reference voltage (positive terminal of compensation EA) starts ramping down with 3.125mV/μs slew rate, and V_{OUT} will follow the reference voltage to 0V. After V_{OUT} drops below 0.2V, the RT8876A shuts down and all functions (drivers) are disabled. The VR_RDY will be pulled down immediately after POR = low or EN = low.

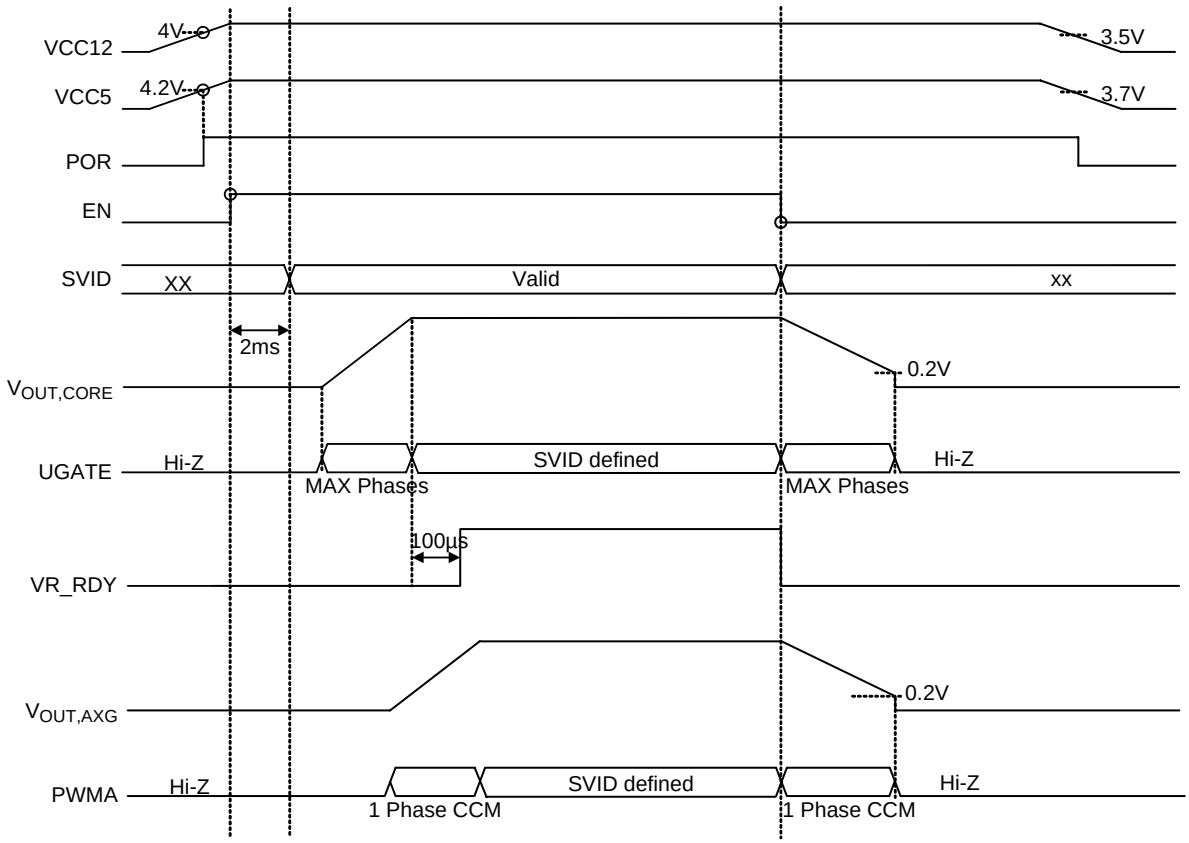


Figure 7 (a). Power Sequence for $V_{INITIAL}$ = 0V

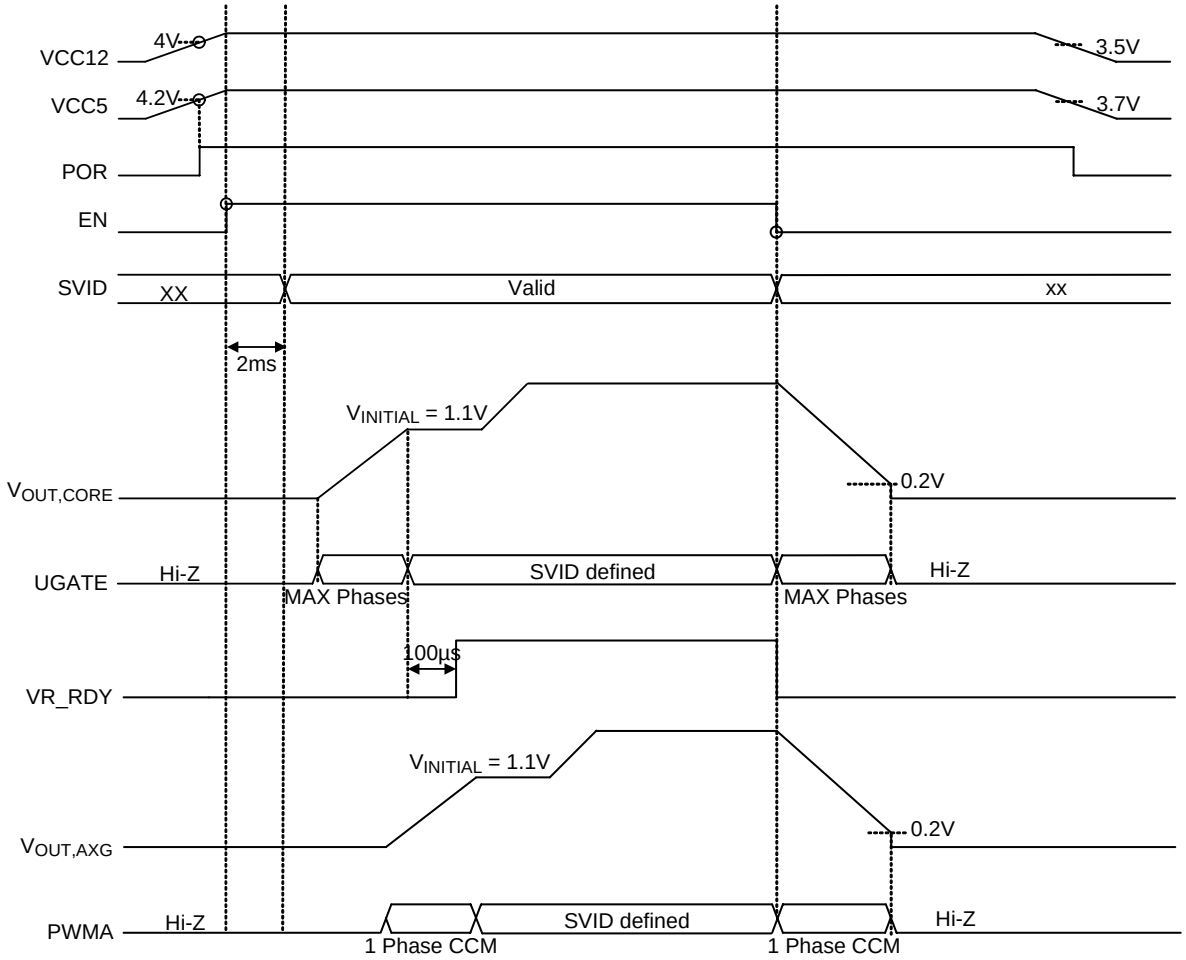


Figure 7 (b). Power Sequence for $V_{INITIAL}$ = 1.1V

CORE VR

Active Phase Determination : Before POR

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during start-up. Normally, the CORE VR operates as a 3-phase PWM controller. Pulling ISEN3N to VCC5 programs a 2-phase operation, pulling ISEN3N and ISEN2N to VCC5 programs a 1-phase operation. Before POR, CORE VR detects whether the voltages of ISEN2N and ISEN3N are higher than "VCC5 – 1V" respectively to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC5.

Loop Control Introduction

The CORE VR adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 8. Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and induces $V_{OUT,CORE}$ to decrease, thus achieving AVP to meet Intel's load line specification. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

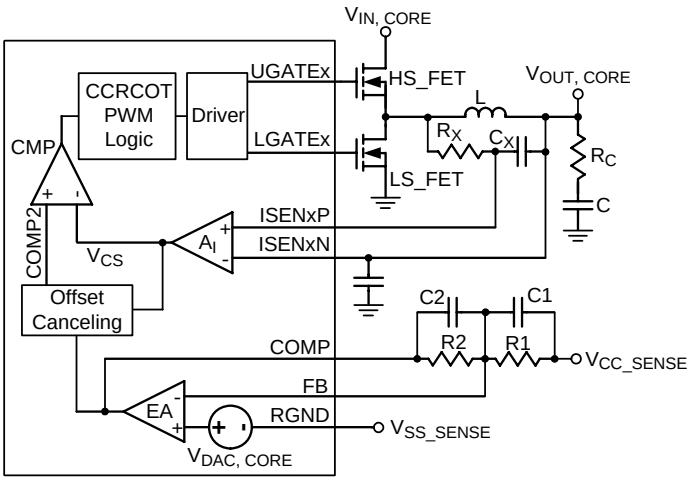


Figure 8. CORE VR : Simplified Schematic for Droop and Remote Sense in CCM

Droop Setting (with Temperature Compensation)

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. The target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} \quad (1)$$

Then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 8 yields the desired error amplifier gain A_V as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (2)$$

where A_I is the internal current sense amplifier gain 10V/V. R_{SENSE} is the current sense resistor. Figure 9 shows the error amplifier gain (A_V) influence on V_{OUT} accuracy according to equation (2). In general, the DCR of the inductor is adopted as R_{SENSE} to achieve lossless current sensing method. R_{DROOP} is the equivalent load line resistance as well as the desired static output impedance.

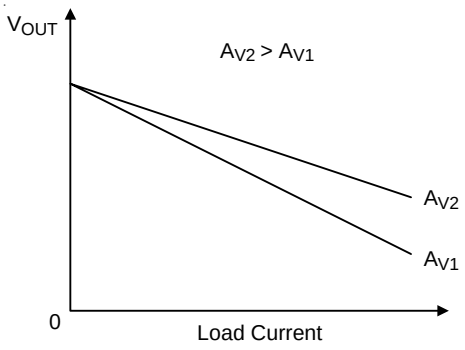


Figure 9. Error Amplifier gain (A_V) Influence on Load Line

Since the DCR of the inductor is temperature dependent, it affects the output accuracy at hot conditions. Temperature compensation is recommended for the lossless inductor DCR current sense method. Figure 10 shows a simple but effective way of compensating the temperature variations of the sense resistor using an NTC thermistor placed in the feedback path.

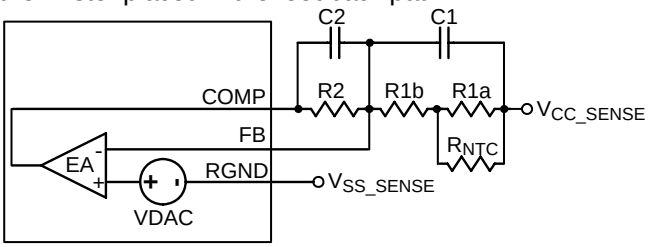


Figure 10. Loop Setting with Temperature Compensation

Usually, R1a is set to equal R_{NTC} (25°C). R1b is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R1b and R2 and then C1 and C2. According to equation (2), to compensate the temperature variations of the sense resistor, the error amplifier gain (A_V) should have the same temperature coefficient with R_{SENSE}. Hence

$$\frac{A_{V,\,HOT}}{A_{V,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (3)$$

From equation (2), A_V can be obtained at any temperature (T°C) as shown below :

$$A_{V,\,T°C} = \frac{R2}{R1a\,//\,R_{NTC,\,T°C} + R1b} \quad (4)$$

The standard formula for the resistance of NTC thermistor as a function of temperature is given by :

$$R_{NTC,\,T°C} = R_{25°C}\, e^{\left\{\beta\left[\left(\frac{1}{T+273}\right) - \left(\frac{1}{298}\right)\right]\right\}} \quad (5)$$

where $R_{25°C}$ is the thermistor's nominal resistance at room temperature, β is the thermistor's material constant in Kelvins, and T is the thermistor's actual temperature in Celsius.

The DCR value at different temperature can be calculated by the following equation :

$$DCR_{T°C} = DCR_{25°C} \times [1 + 0.00393 \times (T - 25)] \quad (6)$$

where 0.00393 is the temperature coefficient of copper. For a given NTC thermistor, solving equation (4) at room temperature (25°C) yields :

$$R2 = A_{V,\ 25°C} \times (R1b + R1a\ //\ R_{NTC,\ 25°C}) \quad (7)$$

where $A_{V,\ 25°C}$ is the error amplifier gain at room temperature and can be obtained from equation (2). R_{1b} can be obtained by substituting (7) for (3),

$$R1b = \frac{\frac{R_{SENSE,\ HOT}}{R_{SENSE,\ COLD}} \times (R1a\ //\ R_{NTC,\ HOT}) - (R1a\ //\ R_{NTC,\ COLD})}{\left(1 - \frac{R_{SENSE,\ HOT}}{R_{SENSE,\ COLD}}\right)} \quad (8)$$

Loop Compensation

Optimized compensation of the CORE VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 10 shows the compensation circuit. Previous design procedure shows how to select resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range. The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (9)$$

where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (10)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{(R1b + R1a\ //\ R_{NTC,\ 25°C}) \times \pi \times f_{SW}} \quad (11)$$

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching related losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Constant on time control is adopted in RT8876A, a constant on time can be set by connecting a resistor from VIN to TONSET pin first, and then the switching frequency of the regulator can be decided to apply in different applications. Figure 11 shows the On-Time setting Circuit. Connect a resistor (R_{TON}) between $V_{IN,CORE}$ and TONSET to set the on-time of UGATE :

$$t_{ON}\ (V_{DAC} < 1.2V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC}} \quad (12)$$

where t_{ON} is the UGATE turn on period, V_{IN} is Input voltage of the CORE VR, and V_{DAC} is the DAC voltage. When VDAC is larger than 1.2V, the equivalent switching frequency may be over 500kHz, and this too fast switching frequency is unacceptable. Therefore, the CORE VR implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When V_{DAC} is larger than 1.2V, the on-time equation will be modified to :

$$t_{ON}\ (V_{DAC} \geq 1.2V) = \frac{20.33 \times 10^{-12} \times R_{TON} \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (13)$$

During PS2/PS3 operation, the CORE VR shrinks its on-time for the purpose of reducing output voltage ripple caused by DCM operation. The shrink percentage is 15% compared with original on-time setting by equation (12) or (13). That is, after setting the PS0 operation on-time, the PS2/PS3 operation on-time is 0.85 times the original on-time. On-time translates only roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in external HS-FET. Also, the dead-time effect increases the effective on-time, which in turn reduces the switching frequency. It occurs only in CCM and during dynamic output voltage transitions, when the inductor current reverses at light or negative load currents. With reversed inductor current, the phase goes high earlier than normal, extending the on-time by a period equal to the HS-FET rising dead time. For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{S(MAX)}(kHz) = \frac{1}{T_{ON} - T_{HS-Delay}} \times \frac{V_{DAC(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS-FET} + DCR - R_{DROOP}\right]}{V_{IN(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS-FET} - R_{ON\_HS-FET}\right]} \quad (14)$$

Where $f_{S(MAX)}$ is the maximum switching frequency, $t_{HS-DELAY}$ is the turn-on delay of HS-FET, $V_{DAC(MAX)}$ is the Maximum VDAC of application, $V_{IN(MAX)}$ is the Maximum application Input voltage, $I_{LOAD(MAX)}$ is the maximum load of application, R_{ON_LS-FET} is the Low side FET $R_{DS(ON)}$, R_{ON_HS-FET} is the High side FET $R_{DS(ON)}$,DCR is the inductor DCR, and R_{DROOP} is the load line setting.

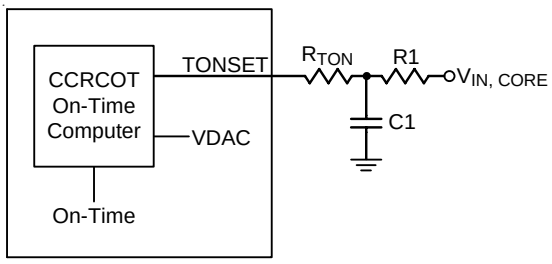


Figure 11. CORE VR : On-Time Setting with R_C Filter

Differential Remote Sense Setting

The CORE VR includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE}. Connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

Current Sense Setting

The current sense topology of the CORE VR is continuous inductor current sensing. Therefore, the controller can be less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The internal current sense amplifier gain (Ai) is fixed to be 10. The ISENxP and ISENxN denote the positive and negative input of the current sense amplifier of any phase. Users can either use a current sense resistor or the inductor's DCR for current sensing. Using the inductor's DCR allows higher efficiency because of lossless characteristic as shown in Figure 12. Refer to below equation for optimum transient performance :

$$\frac{L}{DCR} = R_X \times C_X \quad (15)$$

$$R_X = \frac{0.36\mu H}{1m\Omega \times 100nF} = 3.6k\Omega \quad (16)$$

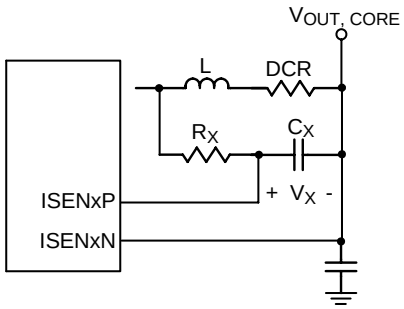


Figure 12. CORE VR : Lossless Inductor Sensing

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage.

If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is chosen too small. Vice versa, with a resistance too large the output voltage transient has only a small initial dip and the recovery is too fast causing a ring back. Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor DCR sensing method.

Current Balance

The CORE VR implements internal current balance mechanism in the current loop. The CORE VR senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase will be adjusted to be shorter, vice versa.

No Load Offset (SVID & Platform)

The CORE VR features no load offset function which provides the possibility of wide range positive offset of output voltage. The no-load offset function can be implemented through the SVID interface or OFS pin. Users can disable pin offset function by simply connecting OFS pin to GND. The RT8876A will latch the OFS status after POR.

If pin offset function is enabled, that the OFS pin voltage is more than 0.6V before POR.

If then the output voltage is :

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{PIN-OFS} + V_{SVID-OFS} \quad (17)$$

The pin offset voltage is set by supplying a voltage into OFS pin. The linear range of offset pin voltage is from 0.9V to 1.83V. The pin offset voltage can be calculated as below :

$$V_{PIN-OFS} = V_{OFS} - 1.2V \quad (18)$$

For example, supplying 1.3V at OFS pin will achieve 100mV offset at the output. Connecting a filter capacitor between the OFS pin and GND is necessary.

Operation Mode Transition

RT8876A supports operation mode transition function at the CORE VR for the SetPS command of Intel's VR12/ IMVP7 CPU. The default operation mode of the CORE VR is PS0, which is full phase CCM operation. Other operation modes include PS1 (single phase CCM operation) and PS2 (single phase DEM operation). After receiving SetPS command, the CORE VR will immediately change to the new operation state. When the CORE VR receives SetPS command of PS1 operation mode, the CORE VR operates as a single phase CCM controller, and only channel 1 is active. The CORE VR will disable phase 2 and phase 3 by disabling Internal PWM logic drivers (PWM = high impedance state). Therefore, 2 internal drivers which support tri-state shutdown are also required for compatibility with PS1 operation mode. Similarly, when the CORE VR receives SetPS command of PS2 operation mode, the CORE VR operates as a single phase DCM controller, and only channel 1 is active with diode emulation operation. The CORE VR will disable phase 2 and phase 3 by disabling internal PWM logic drivers (PWM = high impedance state). Therefore, all internal drivers which support tri-state shutdown are required for compatibility with PS2 operation state. If the CORE VR receives dynamic VID change command (SetVID), the CORE VR will automatically enter PS0 operation mode and all phases will be activated. After $V_{OUT,CORE}$ reaches target voltage, the CORE VR will stay at PS0 state and ignore former SetPS command. Only re-sending SetPS command after SetVID command will the CORE VR be forced into PS1 or PS2 operation states again.

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The DVID pin can be used to compensate the load-line effect, so that the output voltage can be settled to the target value more quickly. During a dynamic VID up event occurred, the RT8876A sources out a current (I_{DVID}) to DVID pin. The voltage on DVID pin is added to DAC during DVID rising to enhance the dynamic VID performance. Connecting a capacitor in parallel with a resistor to DVID pin is recommended. I_{DVID} is 8μA during a SetVID_Fast event. If it is a SetVID_Slow event, I_{DVID} automatically shrinks to 2μA (if slow slew rate is 0.25 x fast slew rate). This function is null during a dynamic VID down event.

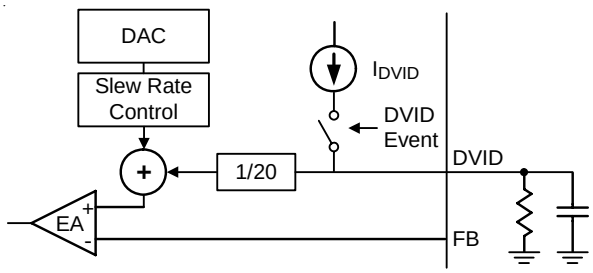


Figure 13. DVID Compensation Circuit

Ramp Amplitude Adjust

When the CORE VR enters PS2 operation mode, the internal ramp of CORE VR will be modified for the reason of stability. In case of smooth transition into PS2, the CCM ramp amplitude should be designed properly. The RT8876A provides RSET pin for platform users to set the ramp amplitude of the CORE VR in CCM. The criteria is to set the ramp amplitude proportional to the on-time (when V_{DAC} <1.2V). The equation will be :

$$57.6 \times 10^{-12} = t_{ON} \times (V_{IN} - V_{DAC}) \times 1 / RSET \quad (19)$$

where 57.6×10^{-12} is an internal coefficient of analog circuit.

According to equation (12), the RSET equation can be simplified to :

$$R_{RSET} = 0.4236 \times R_{TON} \quad (20)$$

Thermal Monitoring and Temperature Reporting

The CORE VR provides thermal monitoring function via sensing TSEN pin voltage. Through the voltage divider resistors, R1 and R_{NTC}, the voltage of TSEN will be proportional to VR temperature. When VR temperature rises, TSEN voltage also rises. The ADC circuit of the CORE VR monitors the voltage variation at the TSEN pin from 1.46V to 1.845V with 55mV resolution. This voltage is then decoded into digital format and stored into Temperature_Zone register.

To meet Intel's VR12/IMVP7 specification, platform users have to set the TSEN voltage to meet the temperature variation of VR from 75% to 100% VR max temperature. For example, if the VR max temperature is 100°C, platform users have to set the TSEN voltage to be 1.515V when VR temperature reaches 82°C and 1.845V when VR temperature reaches 100°C. Detailed voltage setting versus temperature variation is shown in Table 4. The thermometer code is implemented in Temperature_Zone register.

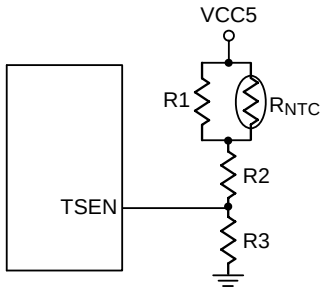


Figure 14. CORE VR : Thermal Monitoring Circuit

Table 4. Temperature_Zone Register

$\overline{\text{VRHOT}}$	SVID Thermal Alert	Comparator Trip Points Temperatures Scaled to maximum = 100% Voltage Represents Assert bit Minimum Level					
b7	b6	b5	b4	b3	b2	b1	b0
100%	97%	94%	91%	88%	85%	82%	75%
1.845V	1.79V	1.735V	1.68V	1.625V	1.57V	1.515V	1.46V

The $\overline{\text{VRHOT}}$ pin is an open-drain structure that sends out active low $\overline{\text{VRHOT}}$ signal. When b6 of Temperature_Zone register asserts to 1 (when TSEN voltage rises above 1.79V), the $\overline{\text{ALERT}}$ signal will be asserted to low, which is so-called SVID thermal alert. In the mean time, the CORE VR will assert bit 1 data to 1 in Status_1 register. The $\overline{\text{ALERT}}$ assertion will be de-asserted when b5 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSEN voltage falls under 1.735V), and bit 1 of Status_1 register will also be cleared to 0. The bit 1 assertion of Status_1 is not latched and cannot be cleared by GetReg command. When b7 of Temperature_Zone register asserts to 1 (when TSEN voltage rises above 1.845V), the $\overline{\text{VRHOT}}$ signal will be asserted to low. The $\overline{\text{VRHOT}}$ assertion will be de-asserted when b6 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSEN voltage falls under 1.79V). It is typically recommended to connect a pull-up resistor from the $\overline{\text{VRHOT}}$ pin to a voltage source.

Current Monitoring and Current Reporting

The CORE VR provides current monitoring function via sensing the voltage difference of IMONFB pin and output voltage. In G-NAVP™ technology, the output voltage is dependent on output current, and the current monitoring function is achieved by this characteristic of output voltage. Figure 15 shows the current monitoring setting principle. The equivalent output current will be sensed from IMONFB pin and mirrored to IMON pin. The resistor connected to IMON pin determines voltage gain of the IMON output. The current monitor indicator equation is shown as :

$$V_{IMON} = \frac{I_{LOAD} \times R_{DROOP} \times R_{IMON}}{R_{IMONFB}} \quad (21)$$

where I_{LOAD} is the output load current, R_{DROOP} is the equivalent load line resistance, and R_{IMON} and R_{IMONFB} are the current monitor current setting resistors. In VR12/IMVP7 specification, the voltage signal of current monitoring will be restricted by a maximum value. Platform designers have to select R_{IMON} to meet the maximum voltage of IMON at full load. To find R_{IMON} and R_{IMONFB} based on :

$$\frac{R_{IMON}}{R_{IMONFB}} = \frac{V_{IMON(MAX)}}{I_{MAX} \times R_{DROOP}} \quad (22)$$

where the $V_{IMON(MAX)}$ is the maximum voltage at full load, and I_{MAX} is the full load current of VR.

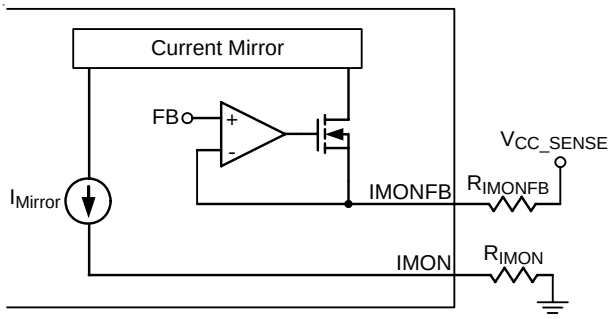


Figure 15. CORE VR : Current Monitoring Circuit

The ADC circuit of the CORE VR monitors the voltage variation at the IMON pin from 0V to 3.3V, and this voltage is decoded into digital format and stored into Output_Current register. The ADC divides 3.3V into 255 levels, so LSB = 3.3V/255 = 12.941mV. Platform designers should design V_{IMON} to be 3.3V at I_{CCMAX}. For example, when load current = 50% x I_{CCMAX}, V_{IMON} = 1.65V and Output_Current register = 7Fh. The IMON pin is an output of the internal operational amplifier and sends out IMON signal. When the data of Output_Current register reaches 255d (when IMON voltage rises above 3.3V), the $\overline{\text{ALERT}}$ signal will be asserted to low, which is so-called SVID ICCMAX alert. In the mean time, the CORE VR will assert the bit 2 data to 1 in Status_1 register. The $\overline{\text{ALERT}}$ assertion will be de-asserted when the data of Output_Current register decreases to 242d (when IMON voltage falls under 3.144V). The bit 2 assertion of Status_1 register is latched and can only be cleared when two criteria are met : the data of Output_Current register decreases to 242d (when IMON voltage falls under 3.144V) and the GetReg command is sent to the Status_1 register of the CORE VR.

Quick Response

The CORE VR utilizes a quick response feature to support heavy load current demand during instantaneous load transient. The CORE VR monitors the current of the IMONFB pin, and this current is mirrored to internal quick response circuit. At steady state, this mirrored current will not trigger a quick response. When the $V_{OUT, CORE}$ voltage drops abruptly due to load apply transient, the mirrored current flowing into quick response circuit will also increase instantaneously. When the mirrored current instantaneously rises above 5μA, quick response will be triggered. When quick response is triggered, the quick response circuit will generate a quick response pulse. The internal quick response pulse generation circuit is similar to the on-time generation circuit. The only difference is the QRSET pin. The voltage at the QRSET pin also influences the pulse width of quick response. A voltage divider circuit is recommended to be applied to the QRSET pin. Therefore, with a little modification of equation (12), the pulse width of quick response pulse can be calculated as :

$$t_{ON,\,QR} = \frac{V_{QRSET}}{1.2} \times t_{ON}$$

$$= \frac{20.33 \times 10^{-12} \times R_{TON} \times V_{QRSET}}{V_{IN} - V_{DAC}} \quad (23)$$

After generating a quick response pulse, the pulse is then applied to the on-time generation circuit, and all the active phases on-times will be overridden by the quick response pulse.

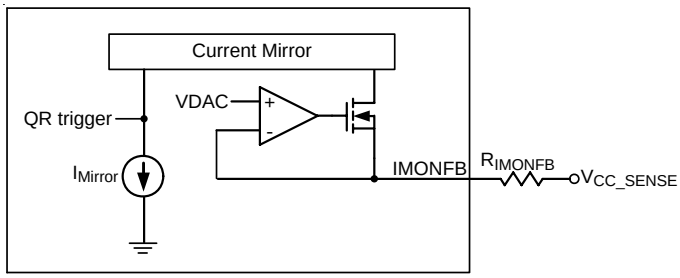


Figure 16. CORE VR : Quick Response Triggering Circuit

Over Current Protection

The CORE VR compares a programmable current limit set point to the voltage from the current sense amplifier output of each phase for Over Current Protection (OCP). Therefore, the OCP mechanism of the RT8876A implements per-phase current protections. The voltage applied to the OCSET pin defines the desired current limit threshold, I_{LIMIT_CORE} :

$$V_{OCSET} = 48 \times I_{LIMIT\_CORE} \times R_{SENSE} \quad (24)$$

Connect a resistive voltage divider from VCC5 to GND, and the joint of the resistive voltage divider is connected to the OCSET pin as shown in Figure 17. For a given R_{OC2},

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC5}}{V_{OCSET}} - 1 \right) \quad (25)$$

The current limit is triggered when per-phase inductor current exceeds the current limit threshold, I_{LIMIT_CORE}, as defined by V_{OCSET}. The driver will then be forced to turn off UGATE until the condition is cleared. If the over current condition of any phase remains valid for 15 cycles, the CORE VR will trigger OCP latch. Latched OCP forces PWM into high impedance, which disables internal PWM logic drivers. If the over current condition is not valid for 15 continuous cycles, the OCP latch counter will be reset. When OCP is triggered by the CORE VR, the AXG VR will also enter soft shut down sequence.

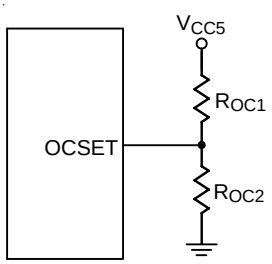


Figure 17. OCP Setting without Temperature Compensation

If inductor DCR is used as the current sense component, temperature compensation is recommended for proper protection under all conditions. Figure 18 shows a typical OCP setting with temperature compensation. Usually, R_{OC1a} is selected to be equal to the thermistor's nominal resistance at room temperature. Ideally, assume V_{OCSET} has the same temperature coefficient as R_{SENSE} (Inductor DCR) :

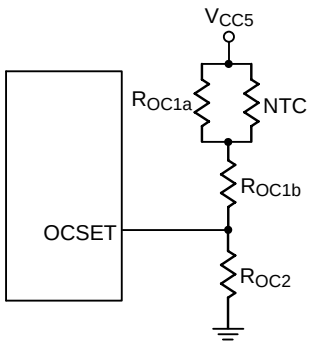


Figure 18. OCP Setting without Temperature Compensation

$$\frac{V_{OCSET,\,HOT}}{V_{OCSET,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (26)$$

According to the basic circuit calculation, we can get V_{OCSET} at any temperature :

$$V_{OCSET,\,T°C} = V_{CC5} \times \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,T°C} + R_{OC1b} + R_{OC2}} \quad (27)$$

Re-write (27) from (26) to get V_{OCSET} at room temperature

$$\frac{R_{OC1a} // R_{NTC,\,COLD} + R_{OC1b} + R_{OC2}}{R_{OC1a} // R_{NTC,\,HOT} + R_{OC1b} + R_{OC2}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (28)$$

$$V_{OCSET,\,25°C} = V_{CC5} \times \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,25°C} + R_{OC1b} + R_{OC2}} \quad (29)$$

Solving (28) and (29) yields R_{OC1b} and R_{OC2}

$$R_{OC2} = \frac{\alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD} + (1-\alpha) \times R_{EQU,\,25°C}}{\frac{V_{CC5}}{V_{OCSET,\,25°C}} \times (1-\alpha)} \quad (30)$$

$$R_{OC1b} = \frac{(\alpha - 1) \times ROC2 + \alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD}}{(1-\alpha)} \quad (31)$$

where

$$\alpha = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} = \frac{DCR_{25°C} \times [1 + 0.00393\ x\ (T_{HOT} - 25)]}{DCR_{25°C} \times [1 + 0.00393\ x\ (T_{COLD} - 25)]} \quad (32)$$

$$R_{EQU,\,T°C} = R_{OC1a} // R_{NTC,\,T°C} \quad (33)$$

Over Voltage Protection (OVP)

The over voltage protection circuit of the CORE VR monitors the output voltage via the ISEN1N pin after POR.

The supported maximum operating VID of the VR ($V_{(MAX)}$) is stored in the VOUT_Max register. Once V_{ISEN1N} exceeds "$V_{(MAX)}$ + 150mV", OVP is triggered and latched. The CORE VR will try to turn on low side MOSFETs and turn off high side MOSFETs of all active phases of the CORE VR to protect the CPU. When OVP is triggered by the CORE VR, the AXG VR will also enter soft shut down sequence. A 1µs delay is used in OVP detection circuit to prevent false trigger. Note that if OFS pin is higher than 0.9V before power up, OVP will trigger at "$V_{(MAX)}$ + 850mV".

Negative Voltage Protection (NVP)

During OVP latch state, the CORE VR also monitors the ISEN1N pin for negative voltage protection. Since the OVP latch will continuously turn on all low side MOSFETs of the CORE VR, the CORE VR may suffer negative output voltage. As a consequence, when the ISEN1N voltage drops below –0.05V after triggering OVP, the CORE VR will trigger NVP to turn off all low side MOSFETs of the CORE VR while the high side MOSFETs remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on all low side MOSFETs. Therefore, the output voltage may travel between 0V and –0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered. A 1µs delay is used in NVP detection circuit to prevent false trigger.

Under Voltage Protection (UVP)

The CORE VR implements under voltage protection of $V_{OUT,CORE}$. If ISEN1N is less than the internal reference by 300mV, the CORE VR will trigger UVP latch. The UVP latch will turn off both high side and low side MOSFETs.

When UVP is triggered by the CORE VR, the AXG VR will also enter soft shut down sequence. A 3µs delay is used in UVP detection circuit to prevent false trigger. If platform OFS function is enabled (OFS pin not connected to GND), the UVP function will be disabled.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC5 or VCC12 pin drops below POR threshold, the CORE VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off by shutting down internal PWM logic drivers. A 3µs delay is used in UVLO detection circuit to prevent false trigger.

AXG VR

AXG VR Disable

The AXG VR can be disabled by connecting ISENAN to a voltage higher than "V_{CC5} – 1V". If not in use, ISENAP and TSENA are recommended to be connected to VCC5, while PWMA is left floating. When AXG VR is disabled, all SVID commands related to AXG VR will be rejected.

Loop Control

The AXG VR adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, $V_{OUT, AXG}$, will decrease with increasing output load current. The control loop consists of a PWM modulator with power stage, a current sense amplifier and an error amplifier as shown in Figure 19. Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, steady state COMPA voltage also increases and induces $V_{OUT, AXG}$ to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to cancel the inherent output offset of finite-gain peak current mode controller.

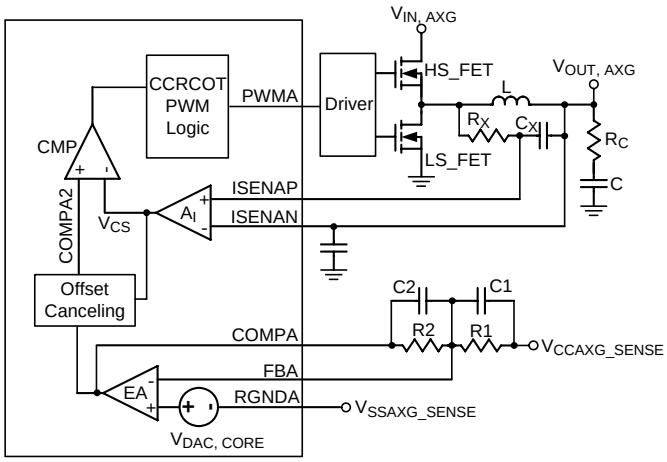


Figure 19. AXG VR : Simplified Schematic for Droop and Remote Sense in CCM

Droop Setting (with Temperature Compensation)

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. The target is to have

$$V_{OUT,AXG} = V_{DAC,AXG} - I_{LOAD} \times R_{DROOP} \quad (34)$$

, then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 19 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (35)$$

where A_I is the internal current sense amplifier gain, R_{SENSE} is the current sense resistance (an external sense resistor

or the DCR of the inductor), and R_{DROOP} is the equivalent load line resistance as well as the desired static output impedance. Since the DCR of the inductor is temperature dependent, the output accuracy may be affected at high temperature conditions. Temperature compensation is recommended for the lossless inductor DCR current sense method. Figure 20 shows a simple but effective way of compensating the temperature variations of the sense resistor by using an NTC thermistor placed in the feedback path.

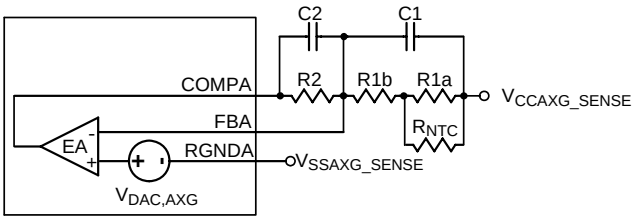


Figure 20. AXG VR : Loop Setting with Temperature Compensation

Usually, R_{1a} is set to equal $R_{NTC\ (25°C)}$ and R_{1b} is selected to linearize the NTC's temperature characteristic. For a given NTC, the design procedure is to get R_{1b} and R2 first, and then C1 and C2 next. According to equation (35), to compensate the temperature variations of the sense resistor, the error amplifier gain (A_V) should have the same temperature coefficient as R_{SENSE}. Hence :

$$\frac{A_{V,\ HOT}}{A_{V,\ COLD}} = \frac{R_{SENSE,\ HOT}}{R_{SENSE,\ COLD}} \quad (36)$$

From (33), Av can be obtained at any temperature (T°C) as :

$$A_{V,\ T°C} = \frac{R2}{R1a\ //\ R_{NTC,\ T°C} + R1b} \quad (37)$$

The standard formula for the resistance of NTC thermistor as a function of temperature is given by :

$$R_{NTC,\ T°C} = R_{25°C}\ e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}} \quad (38)$$

where $R_{25°C}$ is the thermistor's nominal resistance at room temperature, β is the thermistor's material constant in Kelvins, and T is the thermistor actual temperature in Celsius. To calculate DCR value at different temperatures, use the equation below :

$$DCR_{T°C} = DCR_{25°C}\ x\ [1+\ 0.00393\ x\ (T - 25)] \quad (39)$$

where 0.00393 is the temperature coefficient of copper.

For a given NTC thermistor, solving equation (37) at room temperature (25°C) yields

$$R2 = A_{V,\ 25°C}\ x\ (R_{1b} + R_{1a}\ //\ R_{NTC,\ 25°C}) \quad (40)$$

where $A_{V,\ 25°C}$ is the error amplifier gain at room temperature and can be obtained from equation (35). R_{1b} can be obtained by substituting (40) to (36),

$$R1b = \frac{\frac{R_{SENSE,\ HOT}}{R_{SENSE,\ COLD}} \times (R1a\ //\ R_{NTC,\ HOT}) - (R1a\ //\ R_{NTC,\ COLD})}{\left(1 - \frac{R_{SENSE,\ HOT}}{R_{SENSE,\ COLD}}\right)} \quad (41)$$

Loop Compensation

Optimized compensation of the AXG VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for a proper compensation. Figure 20 shows the compensation circuit. Previous design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (42)$$

where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as below :

$$C2 = \frac{C \times R_C}{R2} \quad (43)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{(R1b + R1a\ //\ R_{NTC,\ 25°C}) \times \pi \times f_{SW}} \quad (44)$$

TON Setting

High frequency operation optimizes the application by allowing smaller component size, but with the trade-off of efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents

are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 21 shows the on-time setting circuit. Connect a resistor (R_{TON}) between $V_{IN,AXG}$ and TONSETA pin to set the on-time of UGATE :

$$t_{ON}\ (V_{DAC} < 1.2V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC,AXG}} \quad (45)$$

where t_{ON} is the UGATE turn-on period, V_{IN} is the input voltage of the AXG VR, and $V_{DAC,\,AXG}$ is the DAC voltage. When $V_{DAC,\,AXG}$ is larger than 1.2V, the equivalent switching frequency may be too fast at over 500kHz, which is unacceptable. Therefore, the AXG VR implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When $V_{DAC,\,AXG}$ is larger than 1.2V, the on-time equation will be modified to :

$$t_{ON}\ (V_{DAC} \geq 1.2V) = \frac{20.33 \times 10^{-12} \times R_{TON} \times V_{DAC,\,AXG}}{V_{IN} - V_{DAC,\,AXG}} \quad (46)$$

On-time translates only roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in the external HS-FET. Also, the dead-time effect increases the effective on-time, which in turn reduces the switching frequency. It occurs only in CCM, and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the phase goes high earlier than normal, extending the on-time by a period equal to the HS-FET rising dead time.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{S(MAX)}(kHz) = \frac{1}{t_{ON} - T_{HS-Delay}} \times \frac{V_{DAC(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS-FET} + DCR - R_{DROOP}\right]}{V_{IN(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS-FET} - R_{ON\_HS-FET}\right]} \quad (47)$$

where $f_{S(MAX)}$ is the maximum switching frequency, $t_{HS-DELAY}$ is the turn-on delay of HS-FET, $V_{DAC(MAX)}$ is the maximum $V_{DAC,\,AXG}$ of application, $V_{IN(MAX)}$ is the maximum application input voltage, $I_{LOAD(MAX)}$ is the maximum load of application, R_{ON_LS-FET} is the Low side FET $R_{DS(ON)}$, R_{ON_HS-FET} is the High side FET $R_{DS(ON)}$, DCR is the inductor DCR, and R_{DROOP} is the load line setting.

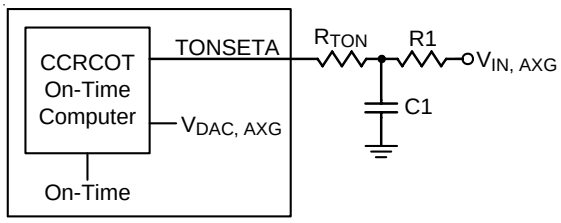


Figure 21. AXG VR : On-Time setting with RC Filter

Differential Remote Sense Setting

The AXG VR includes differential, remote sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins V_{CCAXG_SENSE} and V_{SSAXG_SENSE}. Connect the RGNDA to V_{SSAXG_SENSE}. Connect the FBA to V_{CCAXG_SENSE} with a resistor to build the negative input path of the error amplifier. The $V_{DAC,AXG}$ and the precision voltage reference are referred to RGNDA for accurate remote sensing.

Current Sense Setting

The current sense topology of the AXG VR is continuous inductor current sensing. Therefore, the controller can be less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The internal current sense amplifier gain (A_I) is fixed to be 20. The ISENAP and ISENAN denote the positive and negative input of the current sense amplifier. Users can either use a current sense resistor or the inductor's DCR for current sensing. Using inductor's DCR allows higher efficiency as shown in Figure 22. Refer to below equation for optimum transient performance :

$$\frac{L}{DCR} = R_X \times C_X \quad (48)$$

For example, choosing L = 0.36µH with 1mΩ DCR and C_X = 100nF yields :

$$R_X = \frac{0.36\mu H}{1m\Omega \times 100nF} = 3.6k\Omega \quad (49)$$

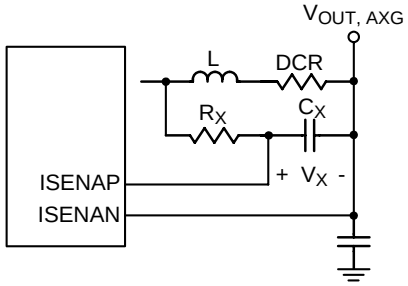


Figure 22. AXG VR : Lossless Inductor Sensing

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is chosen too small. Vice versa, if the resistance is too large the output voltage transient has only a small initial dip and the recovery becomes too fast, causing a ring back to occur. Using current sense resistor in series with the inductor can have better accuracy, but at the expense of efficiency. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor DCR sensing method.

No Load Offset (SVID & Platform)

The AXG VR features no load offset function which provides the possibility of wide range positive offset of output voltage. The no load offset function can be implemented through the SVID interface or OFSA pin. Users can disable pin offset function by simply connecting OFSA pin to GND. The RT8876A will latch the OFSA status after POR. If pin offset function is enabled, the OFSA pin voltage is more than 0.6V before POR.

If then the output voltage is

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{PIN-OFS} + V_{SVID-OFS} \quad (50)$$

The pin offset voltage is set by supplying a voltage into OFSA pin. The linear range of offset pin voltage is from 0.9V to 1.83V. The pin offset voltage can be calculated as below :

$$V_{PIN-OFSA} = V_{OFSA} - 1.2V \quad (51)$$

For example, supplying 1.3V at OFSA pin will achieve 100mV offset at the output. Connecting a filter capacitor between the OFSA pin and GND is necessary.

Operation Mode Transition

The RT8876A supports operation mode transition function at AXG VR for the SetPS command of Intel VR12/IMVP7 CPU. The default operation mode of the AXG VR is PS0, which is CCM operation. Other operation mode includes PS2 (single phase DEM operation). After receiving SetPS command, the AXG VR will immediately change to the new operation state. When the AXG VR receives SetPS command of PS2 operation mode, the AXG VR operates as a single phase DCM controller and diode emulation operation is activated. Therefore, an external driver which supports tri-state shutdown is required for compatibility with PS2 operation state.

If the AXG VR receives dynamic VID change command (SetVID), the AXG VR will automatically enter PS0 operation mode. After $V_{OUT,AXG}$ reach target voltage, AXG VR will stay at PS0 state and ignore former SetPS command. Only by resending SetPS command after SetVID command will the AXG VR be forced into PS2 operation state again.

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The DVIDA pin can be used to compensate the load-line effect, so that the output voltage can be settled to the target value more quickly.

During a dynamic VID up event occurred, the RT8876A sources out a current (I_{DVIDA}) to DVIDA pin. The voltage on DVIDA pin is added to DAC during DVID rising to enhance the dynamic VID performance. Connecting a capacitor in parallel with a resistor to DVIDA pin is recommended. I_{DVIDA} is 8μA during a SetVID_Fast event. If it is a SetVID_Slow event, I_{DVIDA} automatically shrinks to 2μA (if slow slew rate is 0.25x fast slew rate). This function is null during a dynamic VID down event.

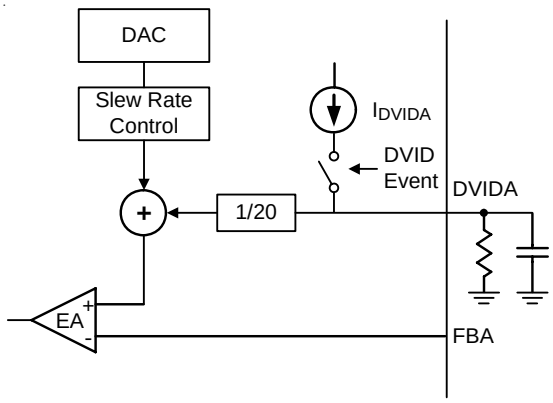


Figure 23. DVID Compensation Circuit

Thermal Monitoring and Temperature Reporting

The AXG VR provides thermal monitoring function via sensing TSENA pin voltage. Through the voltage divider resistors, R1 and R_{NTC}, the voltage of TSENA will be proportional to VR temperature. When VR temperature rises, the TSENA voltage also rises. The ADC circuit of the AXG VR monitors the voltage variation at the TSENA pin from 1.46V to 1.845V with 55mV resolution. This voltage is then decoded into digital format and stored into Temperature_Zone register. To meet Intel's VR12/IMVP7 specification, platform users have to set the TSENA voltage to meet the temperature variation of VR from 75% to 100% VR max temperature.

For example, if the VR max temperature is 100°C, platform users have to set the TSENA voltage to be 1.46V when VR temperature reaches 75°C and 1.845V when VR temperature reaches 100°C. Detailed voltage setting versus temperature variation is shown in Table 5. The thermometer code is implemented in Temperature_Zone register.

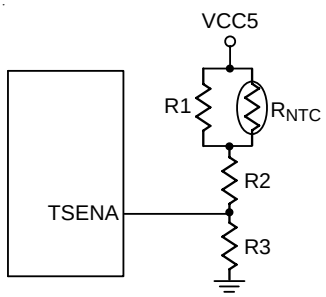


Figure 24. AXG VR : Thermal Monitoring Circuit

Table 5. Temperature_Zone register

$\overline{\text{VRHOT}}$	SVID Thermal Alert
b7	b6
100%	97%
1.845V	1.79V

Comparator Trip Points Temperatures Scaled to maximum = 100% Voltage Represents Assert bit Minimum Level					
b5	b4	b3	b2	b1	b0
94%	91%	88%	85%	82%	75%
1.735V	1.68V	1.625V	1.57V	1.515V	1.46V

The $\overline{\text{VRHOT}}$ pin is an open-drain structure that sends out active-low $\overline{\text{VRHOT}}$ signal. When b6 of Temperature_Zone register asserts to 1 (when TSENA voltage rises above 1.79V), the $\overline{\text{ALERT}}$ signal will be asserted to low, which is so-called SVID thermal alert. In the mean time, the AXG VR will assert the bit 1 data to 1 in Status_1 register. The $\overline{\text{ALERT}}$ assertion will be de-asserted when b5 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSENA voltage falls under 1.735V), and the bit 1 of Status_1 register will also be cleared to 0. The bit 1 assertion of Status_1 is not latched and cannot be cleared by GetReg command.

When b7 of Temperature_Zone register asserts to 1 (when TSENA voltage rises above 1.845V), the $\overline{\text{VRHOT}}$ signal will be asserted to low. The $\overline{\text{VRHOT}}$ assertion will be de-asserted when b6 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSENA voltage falls under 1.79V). The thermal monitoring function of the AXG VR can be disabled by connecting TSENA to VCC5. If TSENA is disabled, all the SVID commands related to Tmperature_Zone register of the AXG VR will be rejected.

Current Monitoring and Current Reporting

The AXG VR provides current monitoring function via sensing the IMONFBA pin. In G-NAVP™ technology, the output voltage is dependent on the output current, and the current monitoring function is achieved by this output voltage characteristic. Figure 25 shows the current monitoring setting principle. The equivalent output current will be sensed from the IMONFBA pin and mirrored to the IMONA pin. The resistor connected to the IMONA pin determines the voltage gain of the IMONA output. The current monitor indicator equation is shown as :

$$V_{IMONA} = \frac{I_{LOAD} \times R_{DROOP} \times R_{IMONA}}{R_{IMONFBA}} \quad (52)$$

Where I_{LOAD} is the output load current, R_{DROOP} is the equivalent load line resistance, and R_{IMONA} and $R_{IMONFBA}$ are the current monitor current setting resistors. In VR12/IMVP7 specification, the voltage signal of current monitoring will be restricted by a maximum value. Platform designers have to select R IMONA to meet the maximum

voltage of IMONA at full load. Find R_{IMONA} and $R_{IMONFBA}$ based on :

$$\frac{R_{IMONA}}{R_{IMONFBA}} = \frac{V_{IMONA(MAX)}}{I_{MAX} \times R_{DROOP}} \quad (53)$$

where $V_{IMONA(MAX)}$ is the maximum voltage at full load, and I_{MAX} is the full load current of VR.

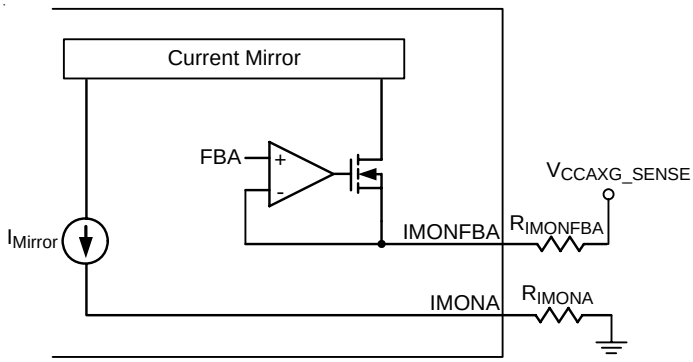


Figure 25. AXG VR : Current Monitoring Circuit

The ADC circuit of the AXG VR monitors the voltage variation at the IMONA pin from 0V to 3.3V, and this voltage is decoded into digital format and stored into the Output_Current register. The ADC divides 3.3V into 255 levels, so LSB = 3.3V/255 = 12.941mV. Platform designers should design V_{IMONA} to be 3.3V at ICCMAXA. For example, when load current = 50% x ICCMAXA, V_{IMONA} = 1.65V and Output_Current register = 7Fh. The IMONA pin is an output of the internal operational amplifier and sends out IMONA signal. When the data of Output_Current register reaches 255d (when IMONA voltage rises above 3.3V), the ALERT signal will be asserted to low, which is so-called SVID ICCMAXA alert. In the mean time, the AXG VR will assert the bit 2 data to 1 in Status_1 register. The ALERT assertion will be de-asserted when the data of Output_Current register decreases to 242d (when IMONA voltage falls under 3.144V). The bit 2 assertion of Status_1 register is latched and can only be cleared when two criteria are met : the data of Output_Current register decreases to 242d (when IMONA voltage falls under 3.144V) and the GetReg command is sent to the Status_1 register of the AXG VR.

Quick Response

The AXG VR utilizes a quick response feature to support heavy load current demand during instantaneous load transient. The AXG VR monitors the current of the IMONFBA pin, and this current is mirrored to internal quick response circuit. At steady state, this mirrored current will not trigger a quick response. When the $V_{OUT,AXG}$ voltage drops abruptly due to load apply transient, the mirrored current into quick response circuit will also increase instantaneously. When the mirrored current instantaneously rises above 5μA, quick response will be triggered.

When quick response is triggered, the quick response circuit will generate a quick response pulse. The internal quick response pulse generation circuit is similar to the on-time generation circuit. The only difference is the QRSETA pin. The voltage at the QRSETA pin also influences the pulse width of quick response. A voltage divider circuit is recommended to be applied to the QRSETA pin. Therefore, with a little modification of equation (45), the pulse width of quick response pulse can be calculated as :

$$t_{ON,QR} = \frac{V_{QRSETA}}{1.2} \times t_{ON}$$
$$= \frac{20.33 \times 10^{-12} \times R_{TON} \times V_{QRSETA}}{V_{IN} - V_{DAC,AXG}} \quad (54)$$

After generating a quick response pulse, the pulse is then applied to the on-time generation circuit and the AXG VR's on-time will be overridden by the quick response pulse.

Over Current Protection

The AXG VR compares a programmable current limit set point to the voltage from the current sense amplifier output for Over Current Protection (OCP). Therefore, the OCP mechanism of the RT8876A implements per-phase current protection. The voltage applied to the OCSETA pin defines the desired current limit threshold I_{LIMIT_AXG} :

$$V_{OCSETA} = 48 \times I_{LIMIT\_AXG} \times R_{SENSE} \quad (55)$$

Connect a resistive voltage divider from VCC5 to GND, and the joint of the resistive voltage divider is connected to the OCSETA pin as shown in Figure 26. For a given R_{OC2},

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC5}}{V_{OCSET}} - 1 \right)$$

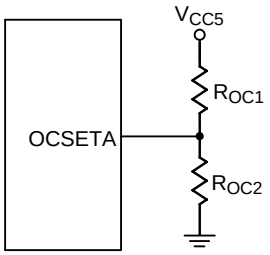


Figure 26. AXG VR : OCP Setting without Temperature Compensation

The current limit is triggered when inductor current exceeds the current limit threshold, I_{LIMIT_AXG}, as defined by V_{OCSETA}. The driver will then be forced to turn off UGATE until the condition is cleared. If the over current condition of any phase remains valid for 15 cycles, the AXG VR will trigger OCP latch. Latched OCP forces PWM into high impedance, which disables internal PWM logic drivers. If the over current condition is not valid for 15 continuous cycles, the OCP latch counter will be reset. When OCP is triggered by the AXG VR, the CORE VR will also enter soft shut down sequence. If inductor DCR is used as the current sense component, temperature compensation is recommended for proper protection under all conditions. Figure 26 shows a typical OCP setting with temperature compensation.

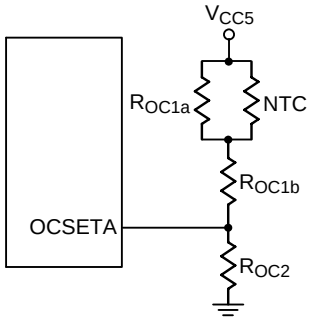


Figure 27. AXG VR : OCP Setting with Temperature Compensation

Usually, R_{OC1a} is selected to be equal to the thermistor's nominal resistance at room temperature. Ideally, assume V_{OCSET} has the same temperature coefficient as R_{SENSE} (Inductor DCR) :

$$\frac{V_{OCSETA,\,HOT}}{V_{OCSETA,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (56)$$

According to the basic circuit calculation, we can get V_{OCSETA} at any temperature :

$$V_{OCSETA,\,T°C} = V_{CC5} \times \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,25°C} + R_{OC1b} + R_{OC2}} \quad (57)$$

Re-write (56) from (57) to get V_{OCSETA} at room temperature:

$$\frac{R_{OC1a} // R_{NTC,\,COLD} + R_{OC1b} + R_{OC2}}{R_{OC1a} // R_{NTC,\,HOT} + R_{OC1b} + R_{OC2}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (58)$$

$$V_{OCSETA,\,25°C} = V_{CC5} \times \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,25°C} + R_{OC1b} + R_{OC2}} \quad (59)$$

Solving (62) and (63) yields R_{OC1b} and R_{OC2}

$$R_{OC2} = \frac{\alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD} + (1-\alpha) \times R_{EQU,\,25°C}}{\frac{V_{CC5}}{V_{OCSETA,\,25°C}} \times (1-\alpha)} \quad (60)$$

$$R_{OC1b} = \frac{(\alpha - 1) \times ROC2 + \alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD}}{(1-\alpha)} \quad (61)$$

where

$$\alpha = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} = \frac{DCR_{25°C} \times [1 + 0.00393 \times (T_{HOT} - 25)]}{DCR_{25°C} \times [1 + 0.00393 \times (T_{COLD} - 25)]} \quad (62)$$

$$R_{EQU,\,T°C} = R_{OC1a} // R_{NTC,\,T°C} \quad (63)$$

Over Voltage Protection (OVP)

The over voltage protection circuit of the AXG VR monitors the output voltage via the ISENAN pin after POR. The supported maximum operating VID of the VR ($V_{(MAX)}$) is stored in the VOUT_Max register. Once V_{ISENAN} exceeds "$V_{(MAX)}$ + 150mV", OVP is triggered and latched. The AXG VR will try to turn on low side MOSFETs and turn off

high side MOSFETs of the AXG VR to protect the CPU. When OVP is triggered by the AXG VR, the CORE VR will also enter shut down sequence. A 1µs delay is used in OVP detection circuit to prevent false trigger. Note that if OFSA pin is higher than 0.9V before power up, OVP would trigger when "$V_{(MAX)}$ + 850mV".

Negative Voltage Protection (NVP)

During OVP latch state, the AXG VR also monitors the ISENAN pin for negative voltage protection. Since the OVP latch continuously turns on all low side MOSFETs of the AXG VR, the AXG VR may suffer negative output voltage. As a consequence, when the ISENAN voltage drops below –0.05V after triggering OVP, the AXG VR will trigger NVP to turn off all low side MOSFETs of the AXG VR while the high side MOSFETs remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on all low side MOSFETs.

Therefore, the output voltage may bounce between 0V and –0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered. A 1µs delay is used in NVP detection circuit to prevent false trigger.

Under Voltage Protection (UVP)

The AXG VR implements under voltage protection of $V_{OUT,AXG}$, if V_{FBA} is less than the internal reference by 300mV, the AXG VR will trigger UVP latch. The UVP latch will turn off both high side and low side MOSFETs. When UVP is triggered by the AXG VR, the CORE VR will also enter soft shut down sequence. A 3µs delay is used in UVP detection circuit to prevent false trigger. If platform OFSA function is enabled (OFSA pin not connected to GND), the UVP function will be disabled.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC5 or VCC12 pin drops below POR threshold, the AXG VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off by shutting down internal PWM logic driver. A 3µs delay is used in UVLO detection circuit to prevent false trigger.

Output LC Filter

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{I_{Ripple(MAX)}} \times T_{ON} \quad (64)$$

where T_{ON} is the UGATE turn-on period. Higher inductance yields in less ripple current and hence higher efficiency. The downside is a slower transient response of the power stage to load transients. This might increase the need for more output capacitors, thus driving up the cost. Select a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors are typically used : bulk capacitors closely located next to the inductors, and ceramic output capacitors in close proximity to the load. Latter ones are for mid-frequency decoupling with especially small ESR and ESL values, while the bulk capacitors have to provide enough stored energy to overcome the low frequency bandwidth gap between the regulator and the CPU.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-56L 7x7 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.226W for WQFN-56L 7x7 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 26 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

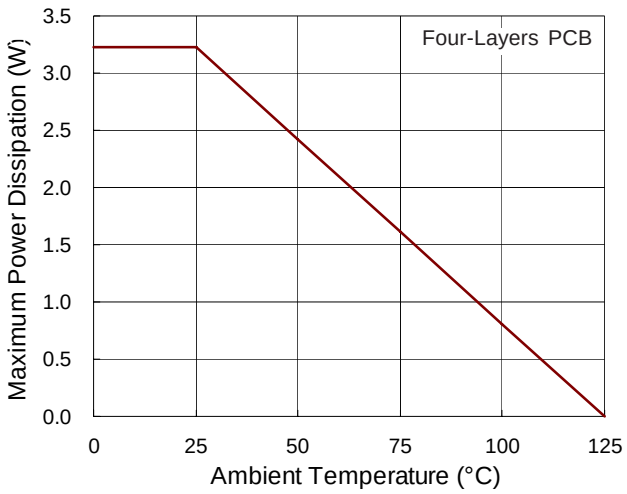


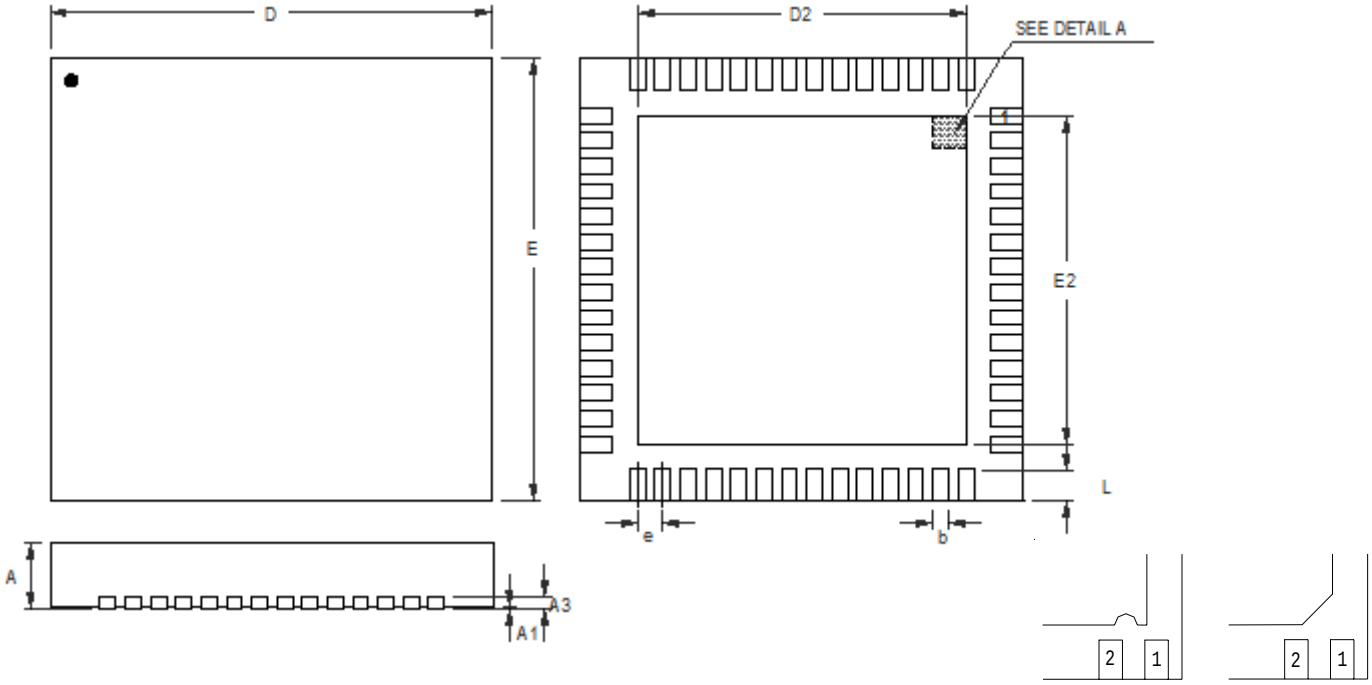
Figure 26. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for PC board layout considerations :

- Input ceramic capacitors must be placed to the drain of high side FET and source of low side FET as close as possible. The loop (The drain of high side FET to phase node to the source of low side FET) is very critical due to it is the main EMI source in Buck converter, so the loop has to be minimized.
- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to let the inductor charging path be longer than the discharging path.
- Place the current sense component close to the controller. ISENxP and ISENxN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee current sense accuracy.
- The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high speed switching nodes away from sensitive analog areas (COMP, FB, ISENxP, ISENxN, etc...)

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.150	5.250	0.203	0.207
E	6.900	7.100	0.272	0.280
E2	5.150	5.250	0.203	0.207
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 56L QFN 7x7 Package

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