Dual Channel Synchronous-Rectified Buck MOSFET Driver

General Description

The RT9607/A is a dual power channel MOSFET driver specifically designed to drive four power N-MOSFETs in a synchronous-rectified buck converter topology. These drivers combined with RichTek' s series of Multi-Phase Buck PWM controllers provide a complete core voltage regulator solution for advanced microprocessors.

The RT9607/A can provide flexible gate driving for both high side and low side drivers. This gives more flexibility of MOSFET selection.

The output drivers of the part are capble to driver a 3nF load in 30/40ns rising/falling time with fast propagation delay from input transition to the gate of the power MOSFET. This device implements bootstrapping on the upper gates with only a single external capacitor required for each power channel. This reduces implementation complexity and allows the use of higher performance, cost effective, N-MOSFETs. Adaptive shoot-through protect-ion is integrated to prevent both MOSFETs from conducting simultaneously.

The RT9607/A can detect high side MOSFET drain-to-source electrical short at power on and pull the 12V power by low side MOS and cause power supply to go into over current shutdown to prevent damage of CPU.

RT9607 has longer UGATE/LGATE dead time which can drive the MOSFETs with large gate RC value, avoiding the shoot-through phenomenon. RT9607A is targeted to drive small gate RC value MOSFETs and performs better efficiency.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

- **Drives Four N-MOSFETs**
- **Adaptive Shoot-Through Protection**
- **Propagation Delay 40ns**
- **Support High Switching Frequency**
- **Fast Output Rise Time**
- **5V to 12V Gate-Drive Voltages for Optimal Efficiency**
- **Tri-State Input for Bridge Shutdown**
- **Supply Under-Voltage Protection**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Core Voltage Supplies for motherboard/desktop PC microprocessor core power
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters

Ordering Information

RT9607/A □ □

- Package Type
  - QV : VQFN-16L 3x3 (V-Type)
  - S : SOP-14
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)
- Short Dead Time
- Long Dead Time

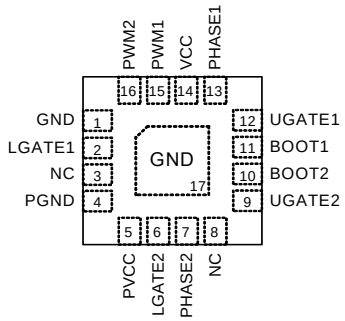
Note :

Richtek products are :

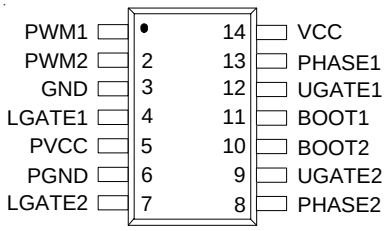
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

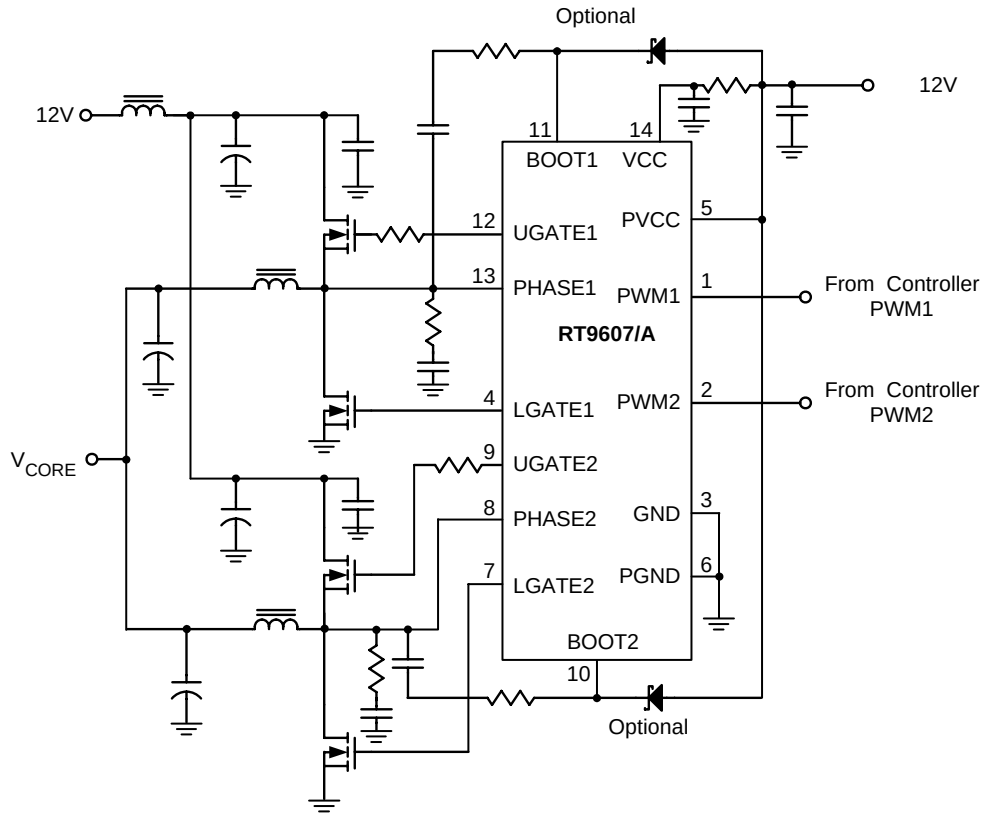


VQFN-16L 3x3

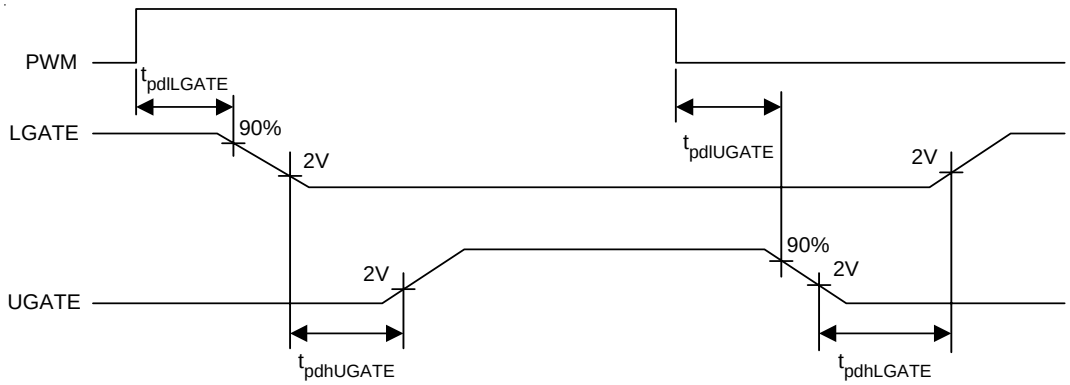


SOP-14

Typical Application Circuit



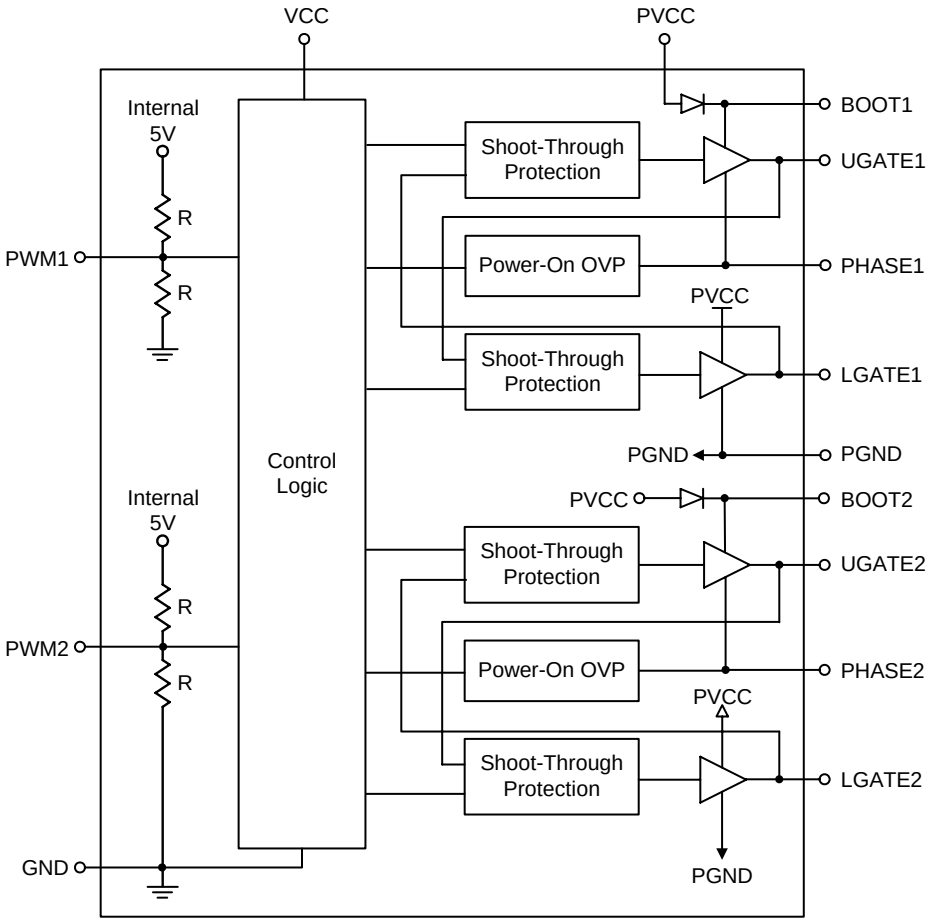
Timing Diagram



Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9607/A□S	RT9607/A□QV		
1	15	PWM1	Channel 1 PWM Input.
2	16	PWM2	Channel 2 PWM Input.
3	1	GND	Ground Pin.
4	2	LGATE1	Lower Gate Drive of Channel 1.
5	5	PVCC	Upper and Lower Gate Driver Power Rail.
6	4	PGND	Lower Gate Driver Ground Pin.
7	6	LGATE2	Lower Gate Drive of Channel 2.
8	7	PHASE2	Connect this pin to phase point of Channel 2. Phase point is the connection point of high side MOSFET source
9	9	UGATE2	Upper Gate Drive of Channel 2.
10	10	BOOT2	Floating Bootstrap Supply Pin of Channel 2.
11	11	BOOT1	Floating Bootstrap Supply Pin of Channel 1.
12	12	UGATE1	Upper Gate Drive of Channel 1.
13	13	PHASE1	Connect this pin to phase point of Channel 1. Phase point is the connection point of high side MOSFET source
14	14	VCC	Control Logic Power Supply.
--	3, 8	NC	No Connection.
--	Exposed Pad (17)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 15V
- Supply Voltage, PV_{CC} ---------- V_{CC} + 0.3V
- BOOT Voltage, V_{BOOT}-V_{PHASE} ---------- 15V
- Input Voltage, V_{PWM} ---------- GND - 0.3V to 7V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC} + 15V
  - < 200ns ---------- –0.3V to 42V
- UGATE ---------- V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
- LGATE ---------- GND - 0.3V to V_{PVCC} + 0.3V
  - < 200ns ---------- –2V to V_{CC} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - VQFN–16L 3x3 ---------- 1.471W
  - SOP-14 ---------- 0.909W
- Package Thermal Resistance (Note 2)
  - VQFN–16L 3x3, θ_{JA} ---------- 68°C/W
  - SOP-14, θ_{JA} ---------- 110°C /W
- Storage Temperature Range ---------- –40°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 12V ±10%
- Junction Temperature Range ---------- 0°C to 125°C
- Ambient Temperature Range ---------- 0°C to 70°C

Electrical Characteristics

(Recommended Operating Conditions, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Current						
Bias Supply Current	I_{VCC}	f_{PWM} = 250kHz, V_{PVCC} = 12V, C_{BOOT} = 0.1μF, R_{PHASE} = 20Ω	--	5.5	8.0	mA
Power Supply Current	I_{PVCC}	f_{PWM} = 250kHz, V_{PVCC} = 12V, C_{BOOT} = 0.1μF, R_{PHASE} = 20Ω	--	5.5	10.0	mA
Power-On Reset						
V_{CC} Rising Threshold			--	8.0	--	V
Hysteresis			--	1.0	--	V

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
PWM Input							
Maximum Input Current			V_{PWM} = 0 or 5V	--	500	--	μA
PWM Floating Voltage			VCC = 12V	--	2.5	--	V
PWM Rising Threshold				3.3	3.7	4.3	V
PWM Falling Threshold				1.0	1.26	1.5	V
Output							
UGATE Rise Time		t_{rUGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
UGATE Fall Time		t_{fUGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	--	40	--	ns
LGATE Rise Time		t_{rLGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
LGATE Fall Time		t_{fLGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
Propagation Delay	RT9607	$t_{pdhUGATE}$	V_{BOOT} = V_{PHASE} = 12V See Timing Diagram	--	75	--	ns
	RT9607A			--	25	--	
	RT9607/A	$t_{pdlUGATE}$		--	40	--	
		$t_{pdhLGATE}$	See Timing Diagram	--	20	--	
		$t_{pdlLGATE}$		--	35	--	
Shutdown Window				1.0	--	4.3	V
UGATE Drive Source		$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V	--	1.8	--	Ω
UGATE Drive Sink		$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 12V	--	1.7	--	Ω
LGATE Drive Source		$R_{LGATEsr}$	V_{CC} = 12V	--	1.5	--	Ω
LGATE Drive Sink		$R_{LGATEsk}$	V_{CC} = 12V	--	1.4	--	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (2S2P,4-layers) of JEDEC 51-7 thermal measurement standard.

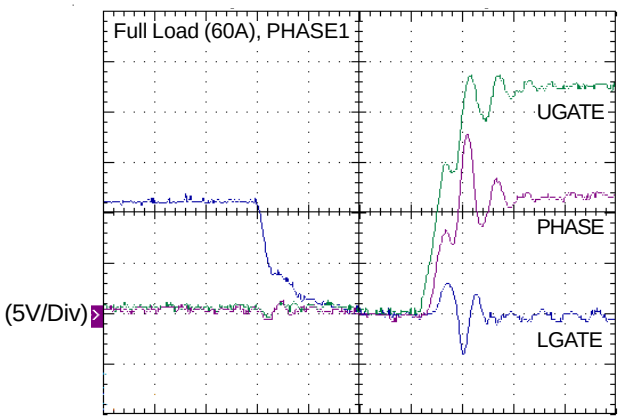
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

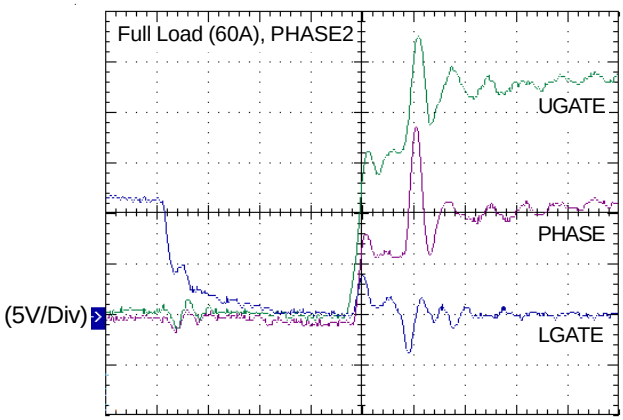
For RT9607

Dead Time at LGATE Falling



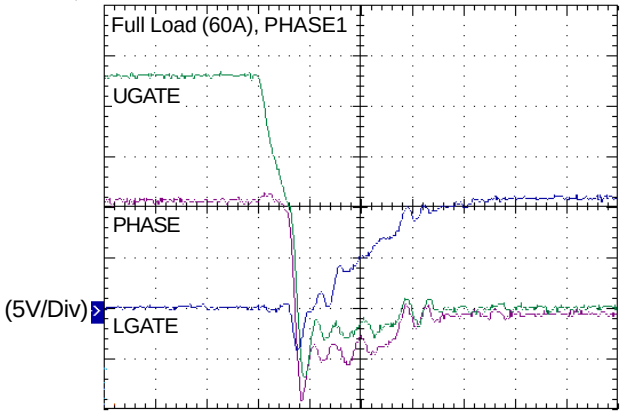
Time (25ns/Div)

Dead Time at LGATE Falling



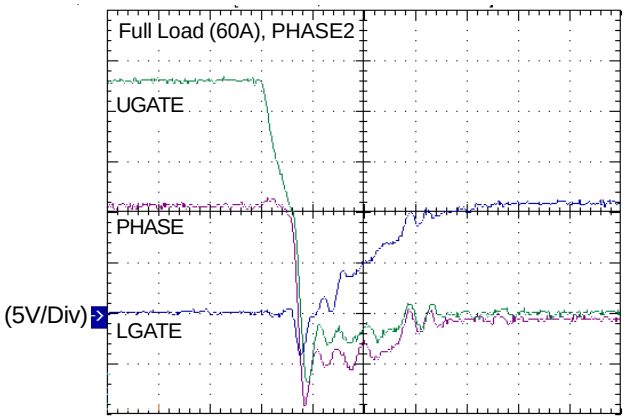
Time (25ns/Div)

Dead Time at LGATE Rising



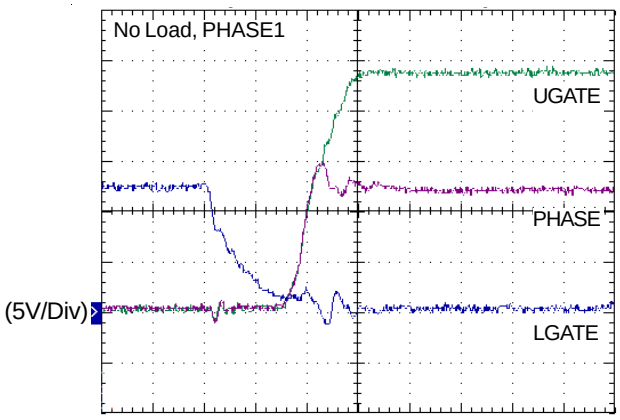
Time (25ns/Div)

Dead Time at LGATE Rising



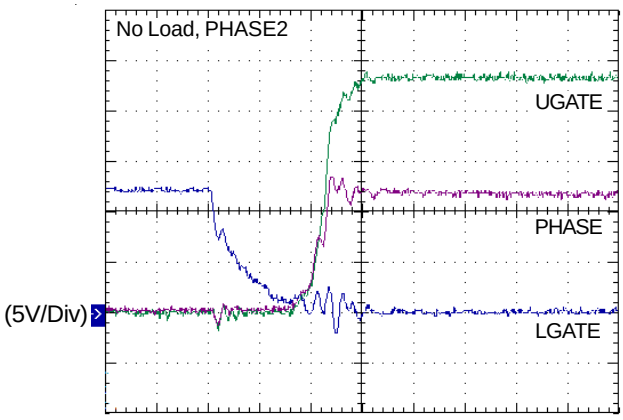
Time (25ns/Div)

Dead Time at LGATE Falling



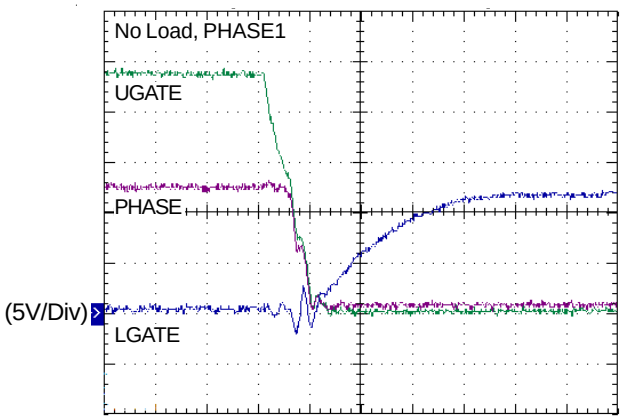
Time (50ns/Div)

Dead Time at LGATE Falling

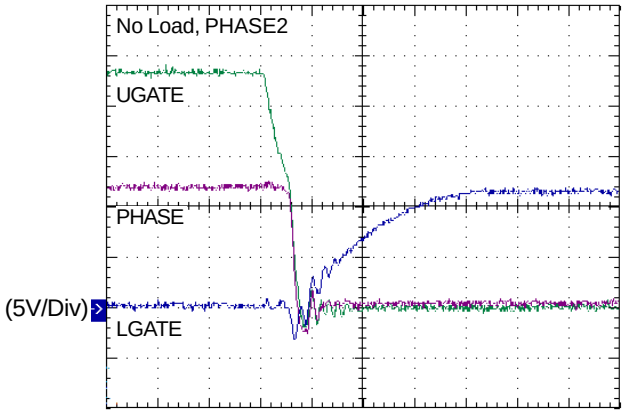


Time (50ns/Div)

Dead Time at LGATE Rising

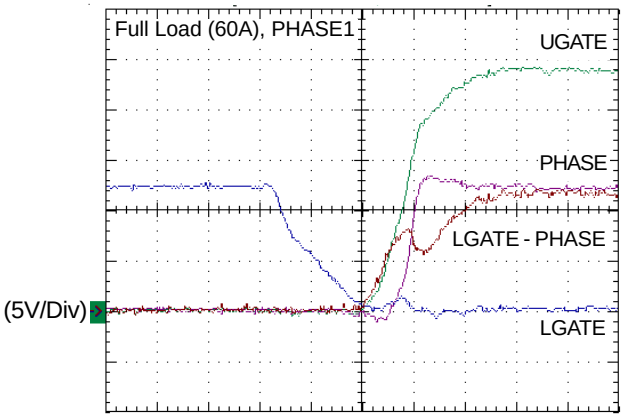


Dead Time at LGATE Rising



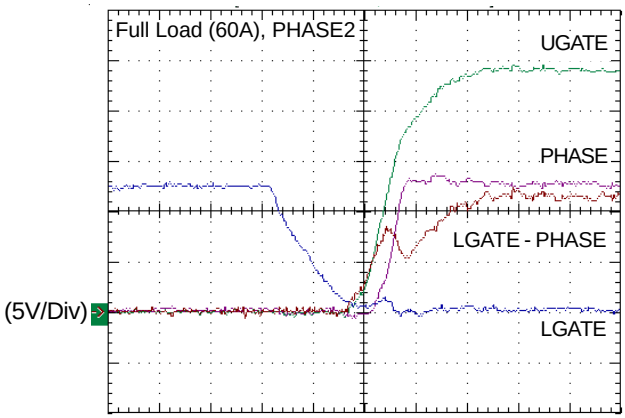
For RT9607A

Dead Time at LGATE Falling



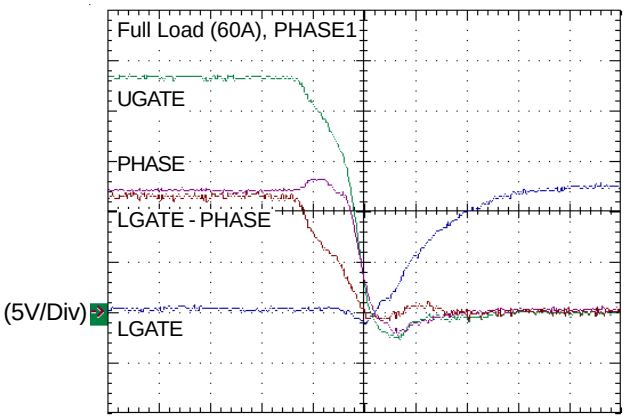
Time (25ns/Div)

Dead Time at LGATE Falling



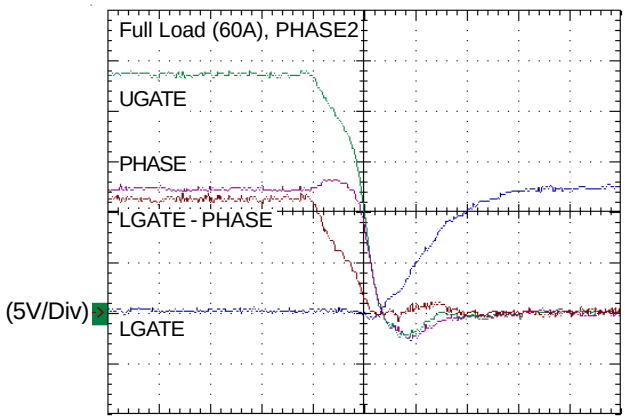
Time (25ns/Div)

Dead Time at LGATE Rising



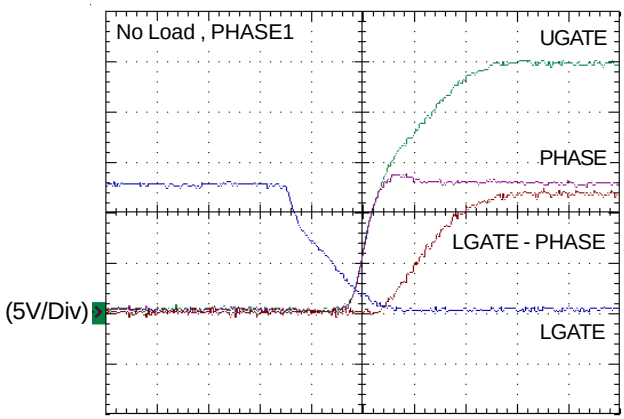
Time (25ns/Div)

Dead Time at LGATE Rising



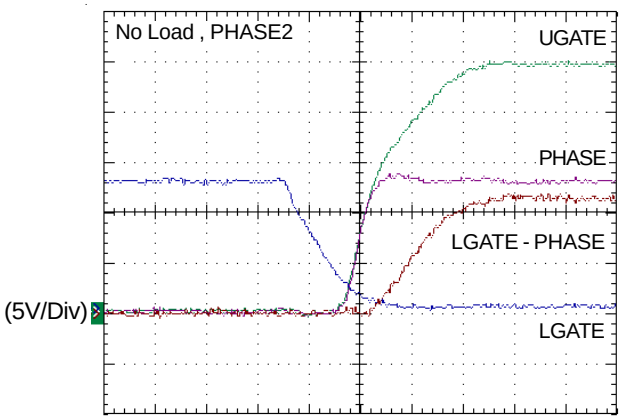
Time (25ns/Div)

Dead Time at LGATE Falling



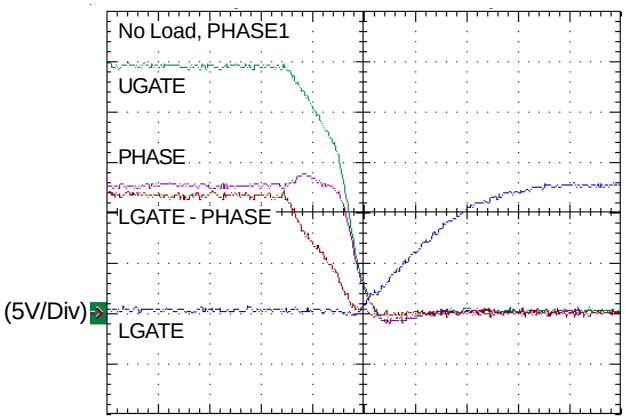
Time (25ns/Div)

Dead Time at LGATE Falling

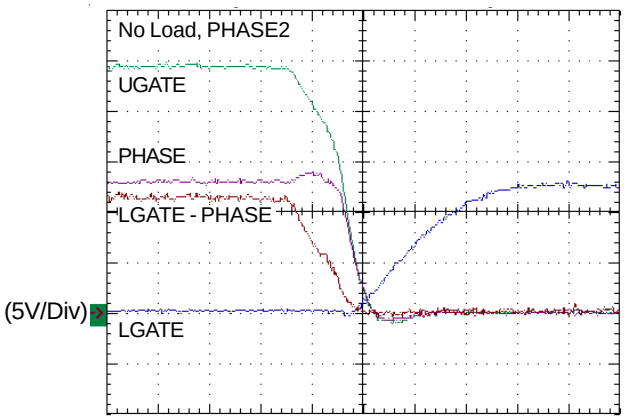


Time (25ns/Div)

Dead Time at LGATE Rising



Dead Time at LGATE Rising



Application Information

The RT9607/A has power on protection function which held UGATE and LGATE low before VCC up cross the rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal turns low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot-through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high. The non-overlapping function is also presented between UGATE and LGATE signal transient.

The PWM signal is recognized as high if above rising threshold and as low if below falling threshold. Any signal level in this window is considered as tri-state, which causes turn-off of both high side and low-side MOSFET. When PWM input is floating (not connected), internal divider will pull the PWM to 1.9V to give the controller a recognizable level. The maximum sink/source capability of internal PWM reference is 60μA.

The PVCC pin provides flexibility of both high side and low side MOSFET gate drive voltages. If 8V, for example, is applied to PVCC, then high side MOSFET gate drive is 8V to 1.5V (approximately, internal diode plus series resistance voltage drop). The low side gate drive voltage is exactly 8V.

The RT9607/A implements a power on over-voltage protection function. If the PHASE voltage exceeds 1.5V at power on, the LGATE would be turn on to pull the PHASE low until the PHASE voltage goes below 1.5V. Such function can protect the CPU from damage by some short condition happened before power on, which is sometimes encountered in the M/B manufacturing line.

Non-overlap Control

To prevent the overlap of the gate drives during the UGATE turn low and the LGATE turn high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to turn low (after propagation delay). Before LGATE can turn high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.2V. Once the monitored voltages fall below 1.2V, LGATE begins to turn high. For short pulse condtion, if the PHASE pin had not gone high after LGATE turns low, the LGATE has to wait for 200ns before turn high only under short pulse (t_{ON}<60ns) condition. By waiting for the voltages of the PHASE pin and high side gate drive to fall below 1.2V, the non-overlap protection circuit ensures that UGATE is low before LGATE turns high. Also to prevent the overlap of the gate drives during LGATE turn low and UGATE turn high, the non-overlap circuit monitors the LGATE voltage. When LGATE go below 1.2V, UGATE is allowed to go high.

Driving power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs} at 12V (or 5V), the gate draws the current only few nanoamperes. Thus once the gate has been driven up to "ON"ON level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

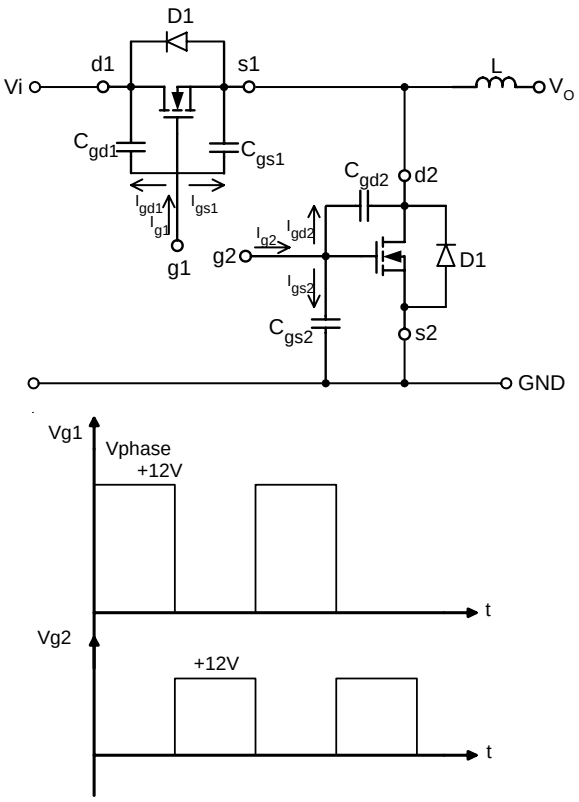


Figure1. The gate driver must supply I_{gs} to C_{gs} and I_{gd} to C_{gd}

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V.The operation consists of charging C_{gd} and C_{gs}. C_{gs1} and C_{gs2} are the capacitances from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs} is referred as "C_{iss}" which is the input capacitance. C_{gd1} and C_{gd2} are the capacitances from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}," the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and $I_{gs2,}$ are showed below

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2}\frac{dV_{g2}}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

According to the design of RT9607/A, before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on

$$I_{gd1} = C_{g1}\frac{dV}{dt} = C_{gd1}\frac{12V}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to Vi. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{V_i + 12V}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified BUCK converter, input voltage V_i = 12V, V_{g1} = V_{g2} = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF,and t_r = 14nS. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF, and t_r = 30nS, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428A \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88A \quad (6)$$

from equation. (3) and (4)

$$I_{gs1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326A \quad (7)$$

$$I_{gs2} = \frac{500 \times 10^{-12} \times (12 + 12)}{30 \times 10^{-9}} = 0.4A \quad (8)$$

the total current required from the gate driving source is

$$Ig1 = Igs + Igd1 = (1.428 + 0.326) = 1.745A \quad (9)$$

$$Ig2 = Igs2 + Igd2 = (0.88 + 0.4) = 1.28A \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Layout Consider

Figure 2. shows the schematic circuit of a two-phase synchronous-buck converter to implement the RT9607/A. The converter operates for the input rang from 5V to 12V.

When layout the PC board, it should be very careful. The power-circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 and Q3, Q4, L4 should be very close. The connection from Q1, and Q3 drain to positive sides of C1, C2, C3, and C4; the connection from Q2, and Q4 source to the negative sides of C1, C2, C3, and C4 should be as short as possible.

Next, the trace from Ugate1, Ugate2, Lgate1, and Lgate2 should also be short to decrease the noise of the driver output signals. Phase1 and phase2 signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C7 should be connected to PGND directly. Furthermore, the bootstrap capacitors (C_{b1}, C_{b2}) should always be placed as close to the pins of the IC as possible.

Select the Bootstrap Capacitor

Figure 3. shows part of the bootstrap circuit of RT9607/A. The V_{CB} (the voltage difference between BOOT1 and PHASE1 on RT9607/A) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is

determined by following constraints.

In practice, a low value capacitor C_B will lead the overcharging that could damage the IC. Therefore to minimize the risk of overcharging and reducing the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1µF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. Here, to adopt either a ceramic or tantalum capacitor is suitable.

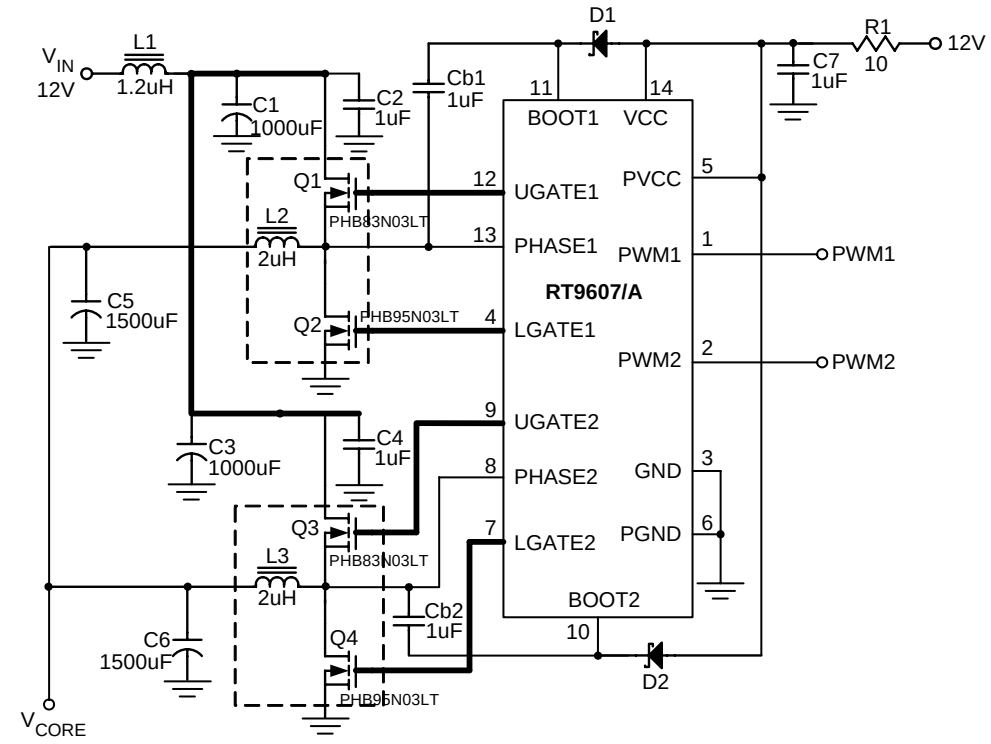


Figure 2. Two- Phase Synchronous-Buck Converter Circuit

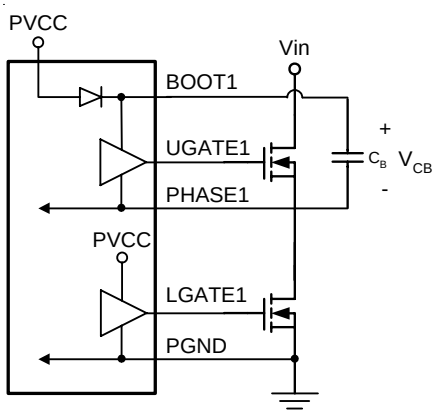
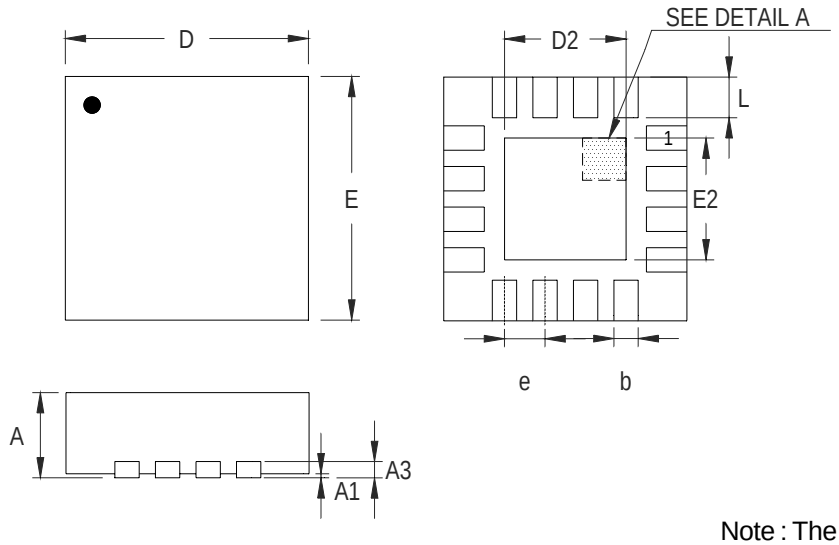
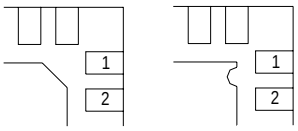


Figure 3. Part of Bootstrap Circuit of RT9607/A

Outline Dimension





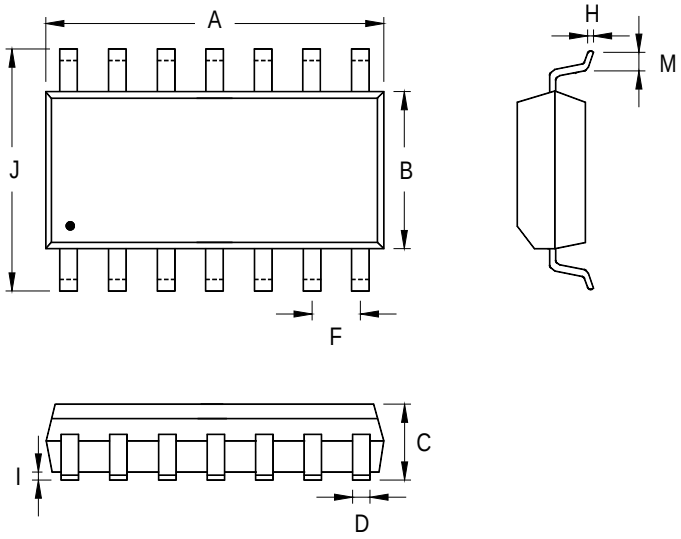
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

14-Lead SOP Plastic Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com