



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFR130 series

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFR130 J

Screening ^{2/}

— = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

Package ^{3/}

J = TO-257
 S.5 = SMD.5
 G = Cerpack

RADIATION TOLERANT 30 AMP, 100 Volts, 25 mΩ Avalanche Rated N-MOSFET

- Features:**
- Rugged Trench Technology
 - Lowest ON-resistance in the industry: 20mΩ typ
 - Radiation tolerant: less than 0.5V typical gate threshold shift @ TID= 100kRAD
 - SEU and SEGR resistant to LET 38
 - Avalanche rated
 - Hermetically Sealed Power Packaging
 - Low Total Gate Charge, Fast Switching
 - Replacement for IRF130 types
 - TX, TXV, S-Level screening available

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V _{DSS}	100	V
Gate – Source Voltage, continuous		V _{GS}	±20	V
Gate – Source Voltage, transient			±30	V
Max. Continuous Drain Current (package limited)	@ T _C = 25°C	I _{D1}	30	A
	@ T _C = 100°C	I _{D2}	30	A
Max. Avalanche Current	@ L= 5.0mH	I _{AR}	10	A
Max. Continuous Drain Current (Tj limited)	@ Tj= 150°C	I _{DM}	140	A
Single Pulse Avalanche Energy	@ L= 5.0mH	E _{AS}	500	mJ
Total Power Dissipation @ T _C = 25°C	TO-257	P _D	120	W
	SMD.5, Cerpack		150	
Operating & Storage Temperature		T _{OP} & T _{STG}	-55 to +175	°C
Maximum Thermal Resistance (Junction to Case)	TO-257	R _{θJC}	1.25	°C/W
	SMD.5, Cerpack		1.00	

NOTES:

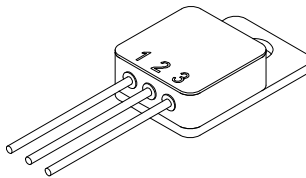
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.

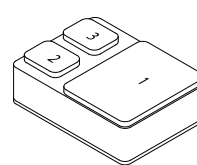
2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ Unless otherwise specified, all electrical characteristics @25°C.

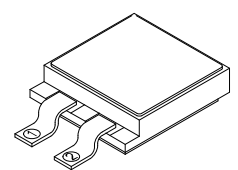
TO-257 (J)



SMD.5 (S.5)



Cerpack (G)





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Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 0.25 \text{ mA}$	BV_{DSS}	100	- 110	-	V
Drain to Source On State Resistance, SFR130J	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$	$R_{DS(on)}$	-	24	30	mΩ
	$V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$		-	40	-	
Drain to Source On State Resistance, SFR130G, SFR130S.5	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$	$R_{DS(on)}$	-	20	25	mΩ
	$V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$		-	35	-	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\mu A, T_j = 25^\circ C$	$V_{GS(th)}$	2.5	3.5	4.5	V
	$V_{DS} = V_{GS}, I_D = 50\mu A, T_j = 125^\circ C$		1.5	2.5	-	
	$V_{DS} = V_{GS}, I_D = 50\mu A, T_j = -55^\circ C$		-	4.0	5.0	
Gate to Source Leakage	$V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	-	5 10	± 100 ± 200	nA
Zero Gate Voltage Drain Current	$V_{DS} = -100V, V_{GS} = 0V, T_j = 25^\circ C$	I_{DSS}	-	0.05	1	μA
	$V_{DS} = 100V, V_{GS} = 0V, T_j = 125^\circ C$		-	3	100	μA
Forward Transconductance	$V_{DS} = 10V, I_D = 30A, T_j = 25^\circ C$	g_{fs}	15	20	-	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	-	52	80	nC
Gate to Source Charge	$V_{DS} = 50V$	Q_{gs}	-	25	-	
Gate to Drain Charge	$I_D = 10A$	Q_{gd}	-	12	-	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	-	30	45	nsec
Rise Time	$V_{DS} = 50V$	t_r	-	40	60	
Turn off Delay Time	$I_D = 10A$	$t_{d(off)}$	-	45	100	
Fall Time	$R_G = 15\Omega$	t_f	-	40	75	
Diode Forward Voltage	$I_F = 10A, V_{GS} = 0V$	V_{SD}	-	0.85	2.0	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr}	-	85	-	nsec
Peak Reverse Recovery Current		Q_{rr}	-	350	-	nC
Reverse Recovery Charge						
Input Capacitance	$V_{GS} = 0V$	C_{iss}	-	2400	3500	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	-	350	400	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	-	80	120	

NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0055A

DOC



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PACKAGE OUTLINE:

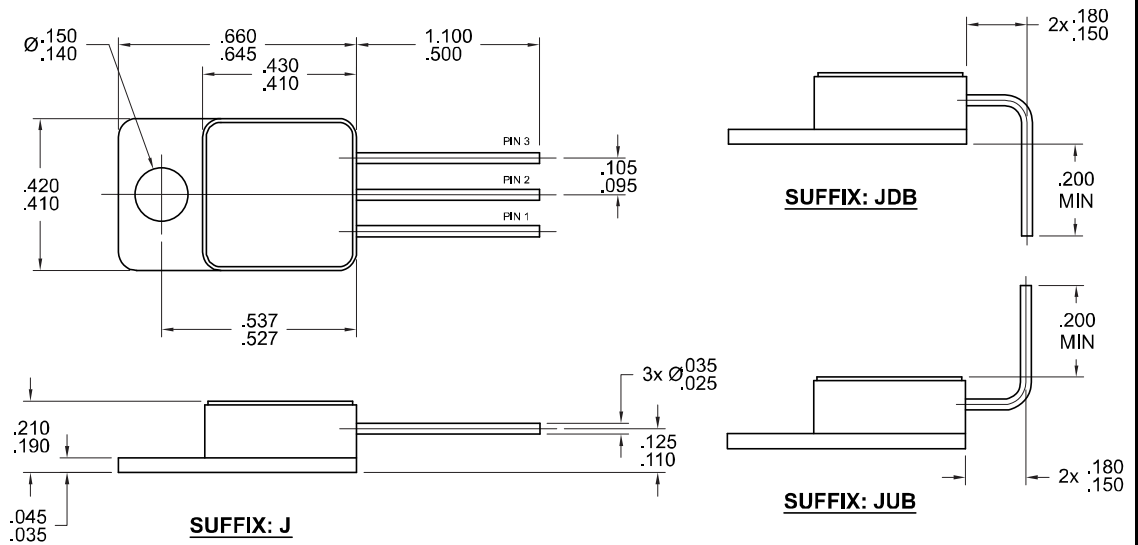
TO-257 (J)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

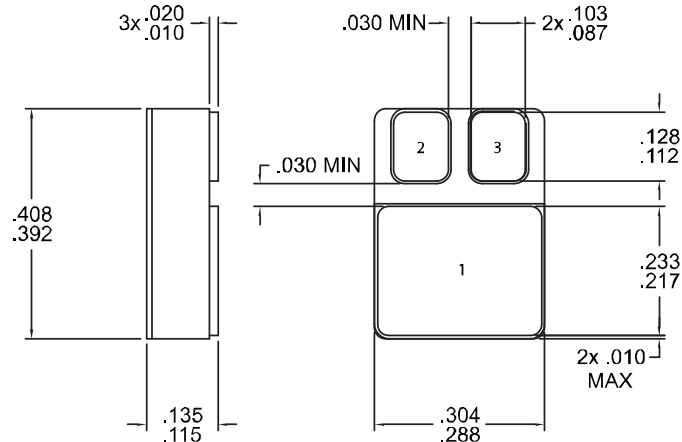
SMD.5 (S.5)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

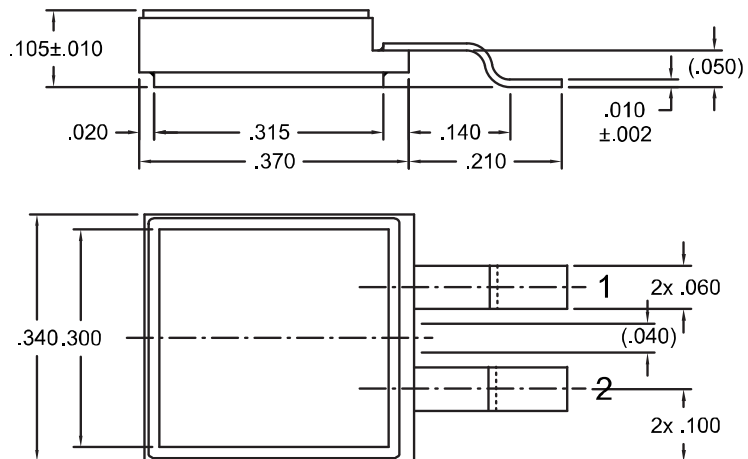
Cerpack (G)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

BOTTOM PAD: GATE



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