

## **CFH2162-P3**

1.8 to 2.0 GHz  
+36 dBm Power GaAs FET

Advanced Product Information  
May 1996 (1 of 2)

## 1.8 to 2.0 GHz +36 dBm Power GaAs FET

### Features

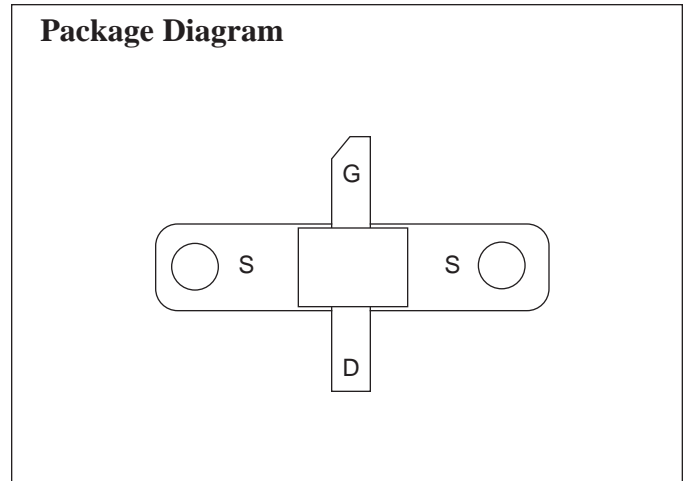
- ❑ High Gain
- ❑ +36 dBm Power Output
- ❑ Proprietary Power FET Process
- ❑ >45% Linear Power Added Efficiency
- ❑ +33 dBm with 30 dBc Third Order Products

### Applications

- ❑ PCS/PCN Base Stations
- ❑ Wireless Local Loop

### Description

The CFH2162-P3 is a high-gain, linear FET intended for driver amplifier applications in high-power systems, and output stage usage in medium power applications at power levels up to +36 dBm. The device is easily matched and pro-



vides excellent linearity at 4 Watts. Manufactured in Celeritek's proprietary power FET process, this device is assembled in a power flange package.

**Specifications** (TA = 25°C) The following specifications are guaranteed at room temperature in Celeritek test fixture at 1.95 GHz.

Parameters	Conditions	Min	Typ	Max	Units
<b>V<sub>d</sub> = 10V, I<sub>d</sub> = 1100 mA (Quiescent)</b>					
P <sub>-1dB</sub>		36.0	37.0	—	dBm
G <sub>-1 dB</sub>		13.0	14.0	—	dB
3rd Order Products <sup>(1)</sup>		30	35	—	dBc
Efficiency	@ P1dB	—	45	—	%
<b>V<sub>d</sub> = 8V, I<sub>d</sub> = 1300 mA (Quiescent)</b>					
P <sub>-1dB</sub>		—	36.0	—	dBm
G <sub>-1 dB</sub>		—	13.0	—	dB

Parameters	Conditions	Min	Typ	Max	Units
g <sub>m</sub>	V <sub>ds</sub> = 2.0V, V <sub>gs</sub> = 0V	—	1700	—	mS
I <sub>dss</sub>	V <sub>ds</sub> = 2.0V, V <sub>gs</sub> = 0V	—	2.8	—	A
V <sub>p</sub>	V <sub>ds</sub> = 3.0V, I <sub>ds</sub> = 65 mA	—	-1.8	—	Volts
BV <sub>GD</sub>	I <sub>gd</sub> = 6.5 mA	20	24	—	Volts
Θ <sub>JL</sub> (2)	@ 150°C TCH	—	8	—	°C/W

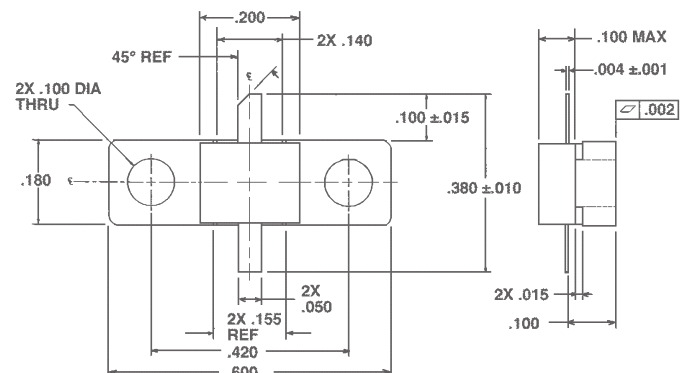
### Absolute Maximum Ratings

Parameter	Symbol	Rating
Drain-Source Voltage	V <sub>DS</sub>	15V <sup>(3)</sup>
Gate-Source Voltage	V <sub>GS</sub>	-5V
Drain Current	I <sub>DS</sub>	I <sub>dss</sub>
Continuous Dissipation	P <sub>T</sub>	10W
Channel Temperature	T <sub>CH</sub>	175°C
Storage Temperature	T <sub>STG</sub>	-65°C to +175°C

#### Notes:

1. Sum to two tones with 1 MHz spacing = 33 dBm.
2. See thermal considerations information.
3. Maximum potential difference across the device (V<sub>d</sub> + V<sub>g</sub>) cannot exceed 18V.

### Power Flange Package Physical Dimensions



## Ordering Information

The CFH2162-P3 power stage is available in a SOIC-8 surface mount package. Devices are available in tape and reel. Ordering part numbers are listed.

<u>Part Number for Ordering</u>	<u>Function</u>	<u>Package</u>
CFH2162-P3	1.8 - 2.0 GMHz Power Stage	Power flange package

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