



SANYO Semiconductors

DATA SHEET

LA7796T

Monolithic Linear IC
**For Digital CATV/Cable Modem Receiver
 AGC Amplifier**

Overview

LA7796T is an AGC amplifier. It is ideally suited for use with Digital CATV, Cable modem receiver and IP Telephony receiver.

Functions

- IF AGC control
- IF AGC amplifier
- IF Step Gain Controlled Amplifier
- Driver amplifier

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	V _{CC} max	Pin 1	7.0	V
Circuit Voltages	V max	Pin 4 , Pin 5	V _{CC} op	V
Circuit Current	I ₆	Pin 6 sink current	2	mA
	I ₇	Pin 7 sink current	2	mA
Allowable Power Dissipation	P _d max	T _a ≤ 85°C	220	mW
Operating Temperature Range	T _{opr}		-20 to 85	°C
Storage Temperature Range	T _{stg}		-55 to 150	°C

Specified board: 20.0mm × 10.0mm × 0.8mm, glass epoxy board.

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Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended Supply Voltage	V_{CC}	Pin 1	5.0	V
Operating Supply Voltage Range	$V_{CC \text{ op}}$	Pin 1	4.5 to 5.5	V

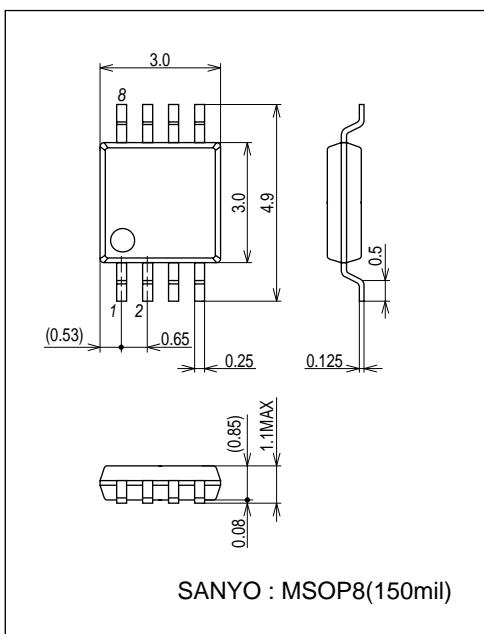
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

Parameter	Symbol	Pin No.	Conditions	Test circuit	Ratings			Unit	
					min	typ	max		
Circuit Current	I_{total}	1	No Signal	1	25	30	35	mA	
IF Input Frequency Range	$f_{(\text{in})}$	2,3	$f_c : -3\text{dB}$	1	30		100	MHz	
Noise Figure	NF	6,7	$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: V_{CC}	2		3	dB	
			$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: GND	2		4	dB	
			$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: OPEN	2		5	dB	
Intermodulation	IM3	6/2,3 7/2,3	$V_4 = 3.0\text{V}$, $f_1 = 44\text{MHz}$, $f_2 = 45\text{MHz}$, Output = $104\text{dB}\mu$ each	1	50			dB	
Total Amplifier Gain	$G_{(\text{AGC1})}$	6/2,3 7/2,3	$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: V_{CC}	1	45.5	48	50.5	dB
	$G_{(\text{AGC2})}$	6/2,3 7/2,3	$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: GND	1	40.5	43	45.5	dB
	$G_{(\text{AGC3})}$	6/2,3 7/2,3	$V_4 = 3.0\text{V}$, $f = 45\text{MHz}$	Pin5: OPEN	1	37.5	40	42.5	dB
AGC Range	GR	6/2,3 7/2,3	IF Output Level $< \pm 1\text{dB}$ $f = 45\text{MHz}$	1	40			dB	
IF Output Level	$V_O(\text{IF})1$	6,7	Output Level, $f = 45\text{MHz}$	1			1.0	V _{p-p}	
AGC Control Max. Voltage	V_{4H}	4	Gain Max.	1	2.5		3	V	
AGC Control Min. Voltage	V_{4L}	4	Gain Min.	1	0		0.5	V	
Input Impedance	Z _{in}	2,3	$V_4 = 0\text{V}$, $f = 45\text{MHz}$	3		1//6.5		kΩ/pF	

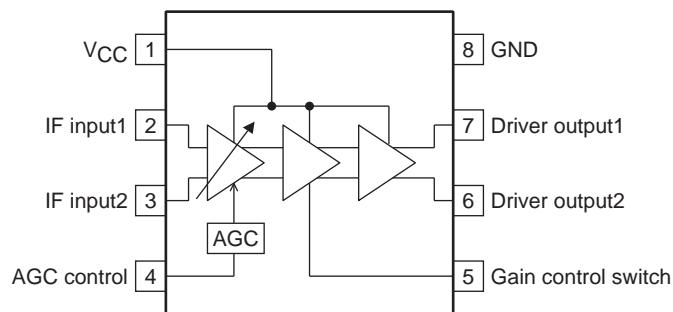
Package Dimensions

unit : mm (typ)

3245B

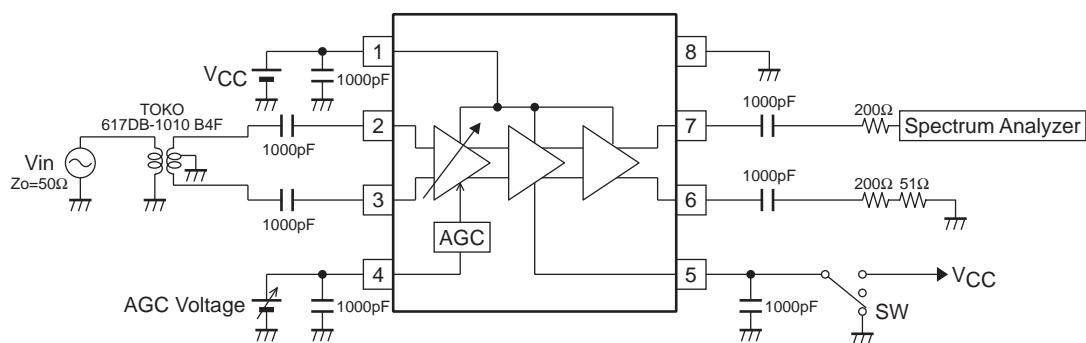


Block Diagram



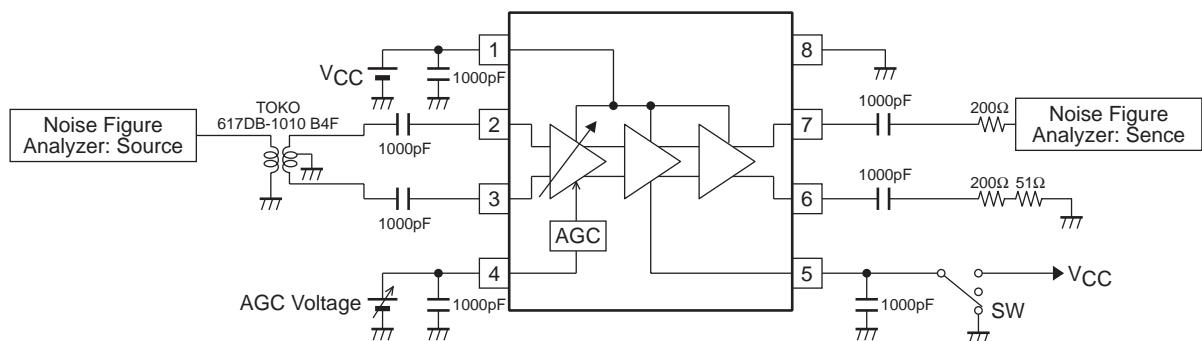
(Caution) Be sure to connect pin 5 to either V_{CC} or GND or keep it open.

Test Circuit1

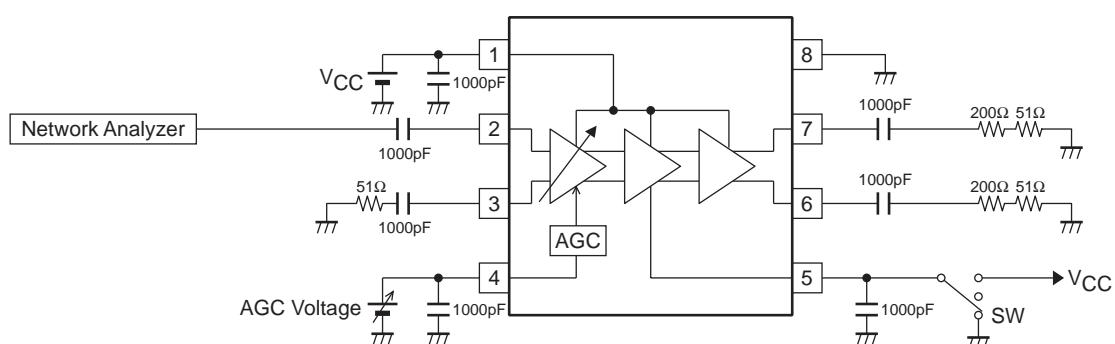


Output Voltage is divided by $50\Omega / (200+50)\Omega$

Test Circuit2



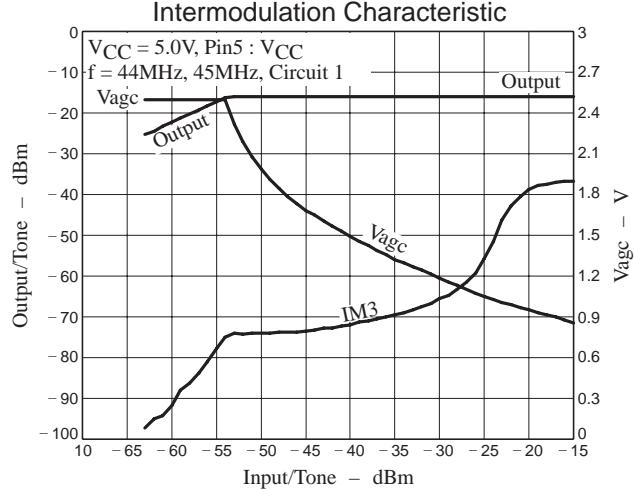
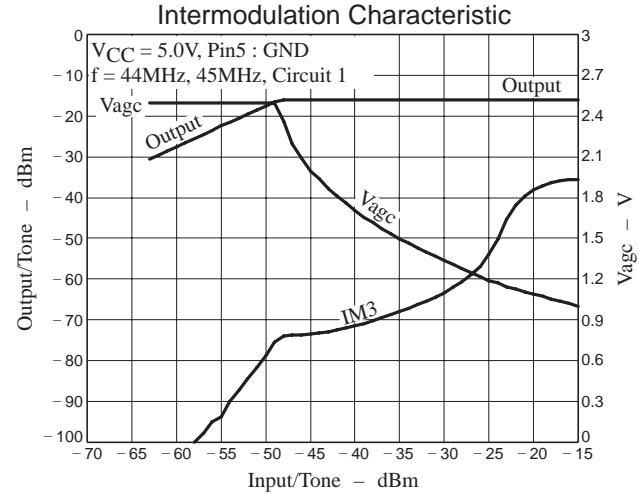
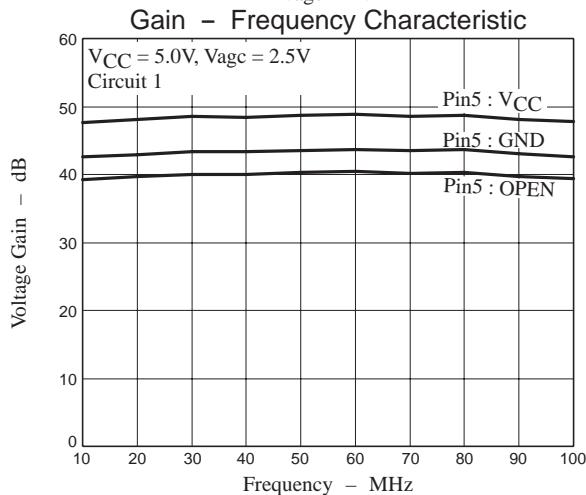
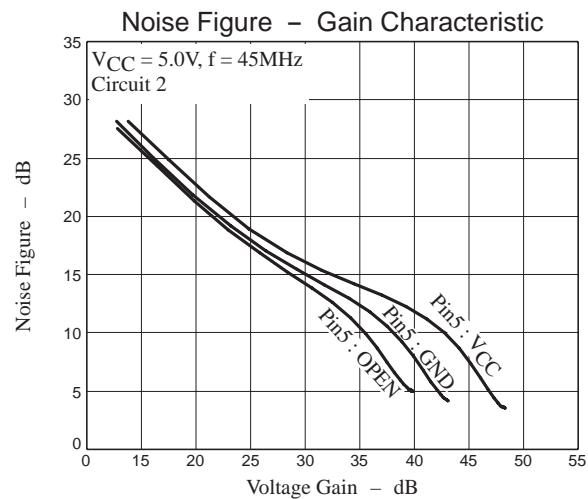
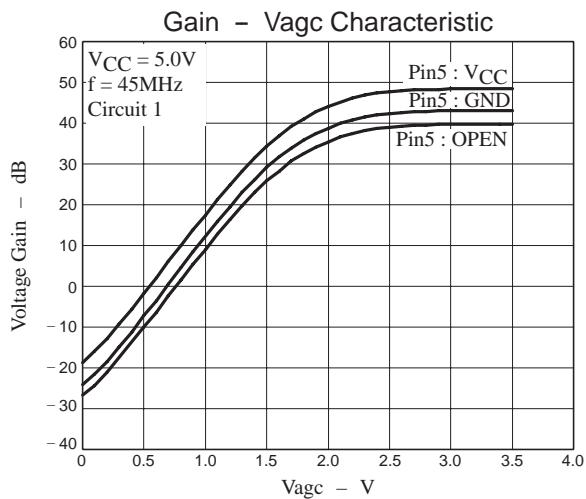
Test Circuit3



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Pin Function

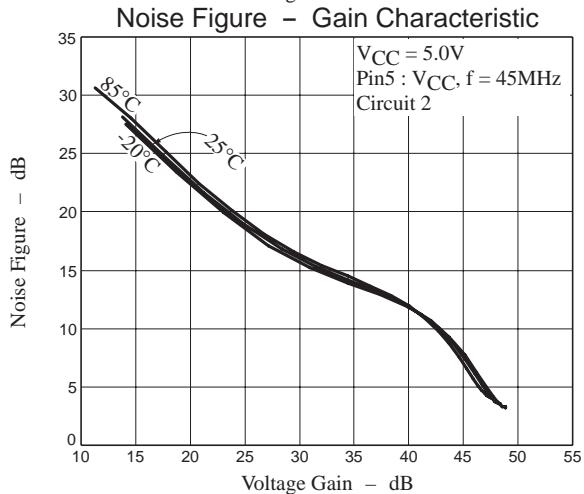
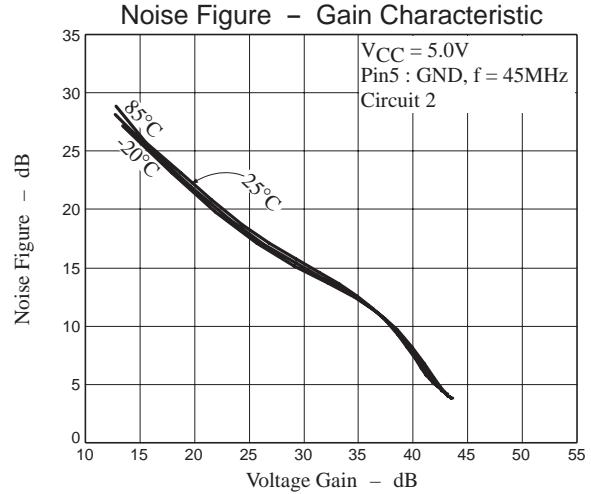
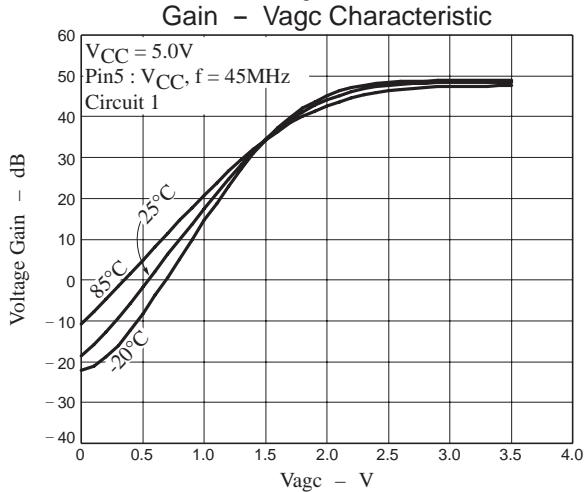
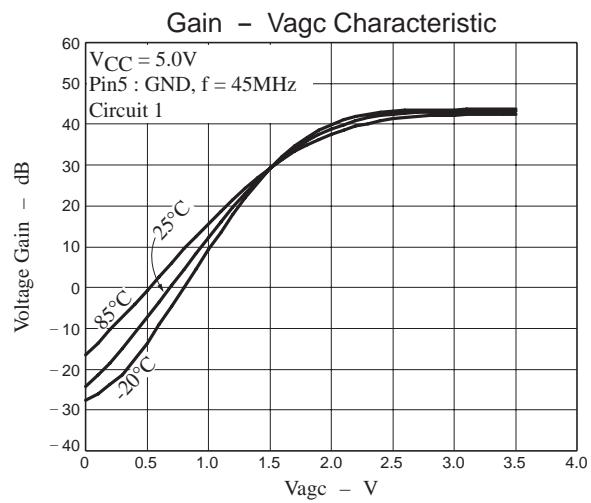
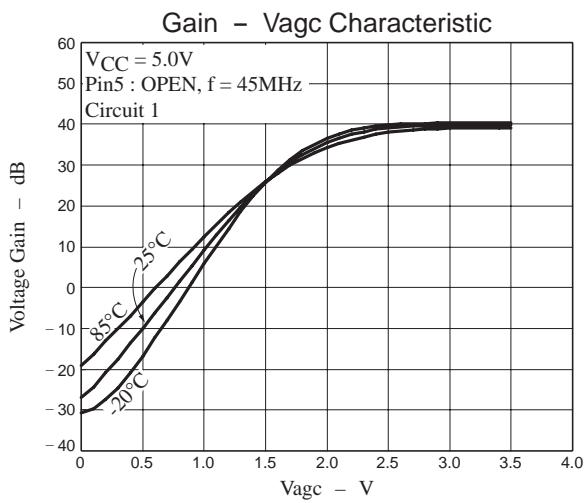
Pin No.	Function	Equivalent circuit
1	V _{CC}	
2 3	IF input.	<p>The diagram shows the IF input stage. It starts with a V_{CC} connection. A diode bridge (two diodes in series) is connected between V_{CC} and ground. The output of the bridge is connected to pin 2 (IF input). A biasing network consisting of resistors and capacitors is connected between the IF input and ground. The output of this stage is connected to pin 3. A common-emitter amplifier stage follows, with its collector connected to V_{CC} and its emitter connected to ground. The base of this stage is connected to the output of the previous stage.</p>
4	AGC control.	<p>The diagram shows the AGC control stage. It starts with a V_{CC} connection. A diode bridge (two diodes in series) is connected between V_{CC} and ground. The output of the bridge is connected to pin 4 (AGC control). A 10kΩ resistor is connected between pin 4 and ground. The other end of this resistor is connected to the base of a common-emitter amplifier stage. The collector of this stage is connected to V_{CC} and the emitter is connected to ground.</p>
5	Gain control Switch.	<p>The diagram shows the Gain control Switch stage. It starts with a V_{CC} connection. A diode bridge (two diodes in series) is connected between V_{CC} and ground. The output of the bridge is connected to pin 5 (Gain control Switch). Three 35kΩ resistors are connected between pin 5 and ground. The bases of three common-emitter amplifier stages are connected to the outputs of these resistors. The collectors of these stages are connected to V_{CC} and the emitters are connected to ground.</p>
6 7	Driver output.	<p>The diagram shows the Driver output stage. It starts with a V_{CC} connection. A diode bridge (two diodes in series) is connected between V_{CC} and ground. The output of the bridge is connected to pin 6 (Driver output). Two 20Ω resistors are connected between pin 6 and ground. The bases of two common-emitter amplifier stages are connected to the outputs of these resistors. The collectors of these stages are connected to V_{CC}. The emitters of these stages are connected to ground through 8.0mA current sources.</p>
8	GND	

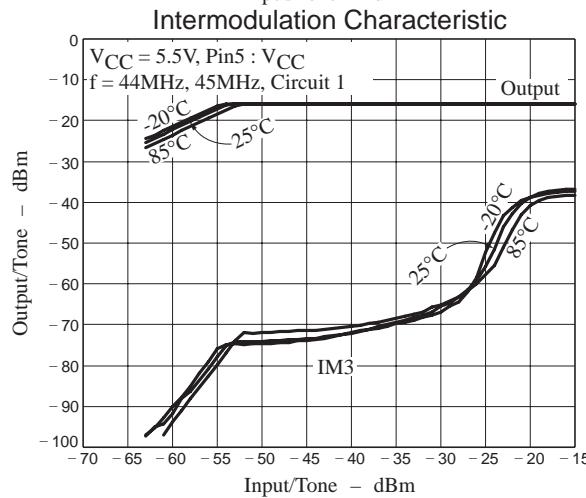
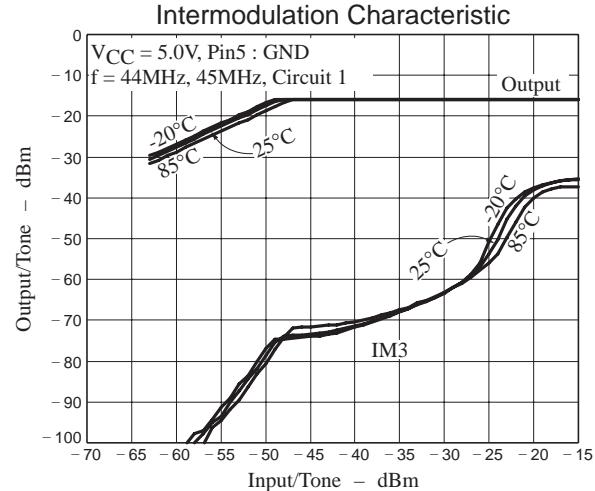
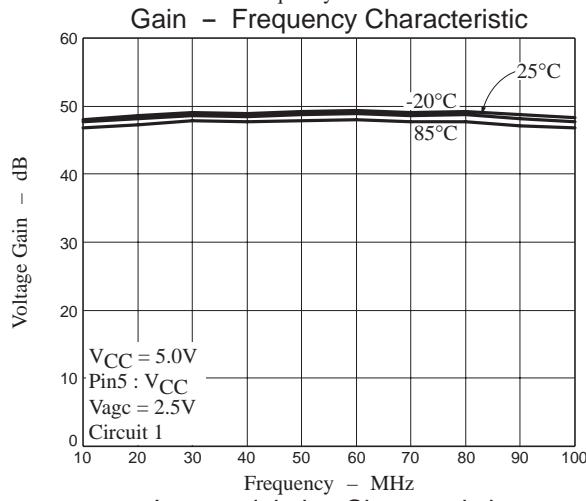
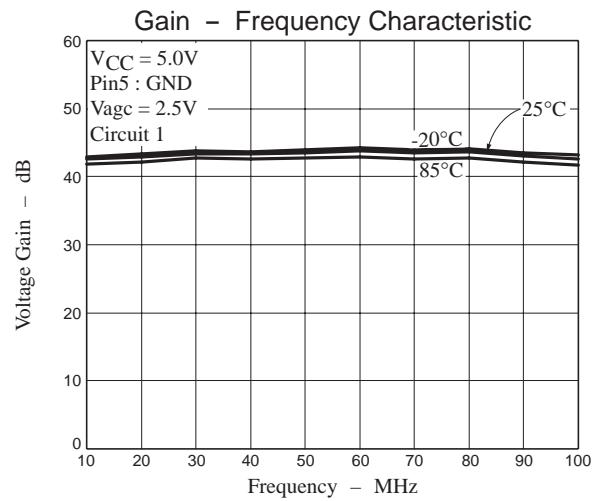
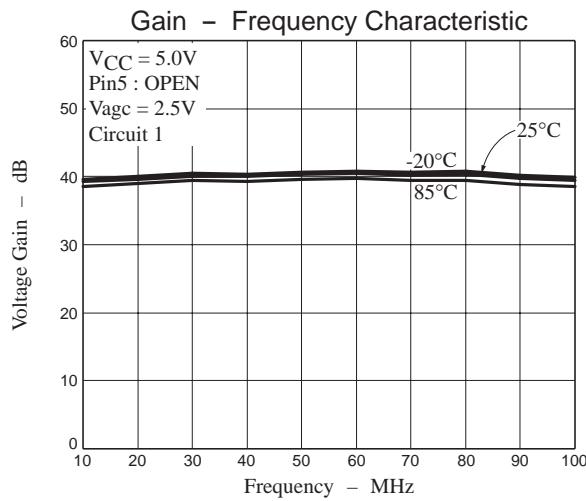


The vertical axis (Output/Tone) on this graph shows the values displayed by the spectrum analyzer for circuit 1.

The actual output power for the corresponding pins is given by the following formula.

$$\{\text{output power [dBm]}\} = \{\text{displayed value [dBm]}\} + 10 \cdot \log(250\Omega/50\Omega)$$





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