



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 6.3 watt RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 2170 MHz.

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 450$ mA, $P_{out} = 6.3$ Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	18.6	20.0	9.4	-43.0	-13
2140 MHz	18.8	20.0	9.2	-42.5	-14
2170 MHz	18.9	20.0	9.1	-42.5	-14

1800 MHz

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 450$ mA, $P_{out} = 6.3$ Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

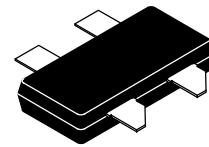
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.8	23.0	9.5	-43.0	-10
1840 MHz	19.1	23.8	9.4	-42.9	-15
1880 MHz	18.7	24.5	9.1	-42.9	-10

Features

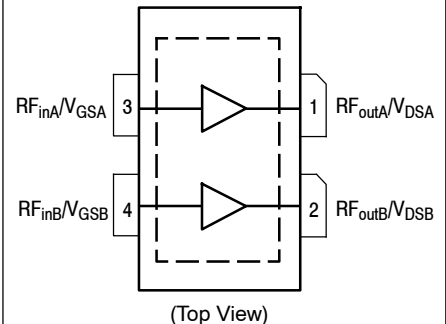
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel.

AFT20P060-4NR3

1805–2170 MHz, 6.3 W AVG., 28 V



**OM-780-4
PLASTIC**



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 6.3 W CW, 28 Vdc, $I_{DQ} = 450$ mA, 2140 MHz Case Temperature 80°C, 60 W CW, 28 Vdc, $I_{DQ} = 450$ mA, 2140 MHz	$R_{\theta JC}$	0.56 0.53	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics (4)

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 36$ μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage ($V_{DS} = 28$ Vdc, $I_D = 450$ mAdc)	$V_{GS(Q)}$	—	2.9	—	Vdc
Fixture Gate Quiescent Voltage (5) ($V_{DD} = 28$ Vdc, $I_D = 450$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.3	5.8	6.3	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 0.36$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.
5. $V_{GG} = 2 \times V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistor divider network on the board. Refer to Test Fixture Layout.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 450\text{ mA}$, $P_{out} = 6.3\text{ W Avg.}$, $f = 2170\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	17.5	18.9	20.5	dB
Drain Efficiency	η_D	18.7	20.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	8.7	9.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-42.5	-40.5	dBc
Input Return Loss	IRL	—	-14	-7	dB

Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 450\text{ mA}$, $f = 2140\text{ MHz}$

VSWR 10:1 at 32 Vdc, 83 W CW Output Power (3 dB Input Overdrive from 60 W CW Rated Power)	No Device Degradation
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Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 450\text{ mA}$, 2110–2170 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	60	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz frequency range. Measurement made on a single path of the device under Class AB conditions, $P_{out} = 47\text{ W}$, $I_{DQ} = 177\text{ mA}$.)	Φ	—	-20	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	70	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 6.3\text{ W Avg.}$	G_F	—	0.33	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.0002	—	dB/°C

1. Part internally matched both on input and output.

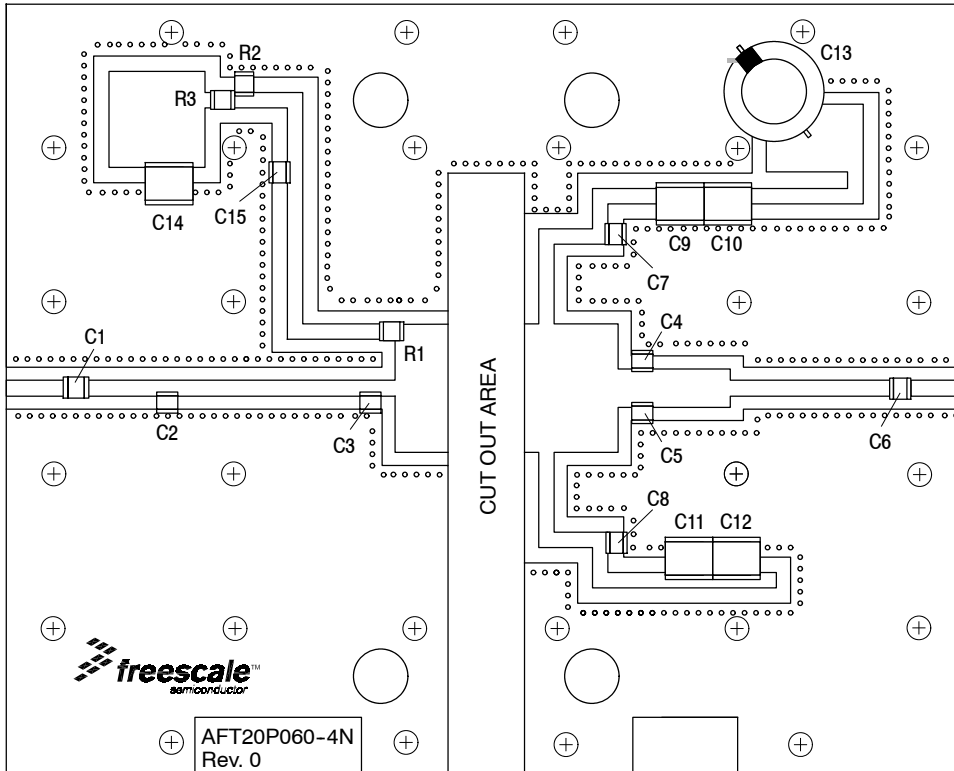


Figure 2. AFT20P060-4NR3 Test Circuit Component Layout — 2110-2170 MHz

Table 6. AFT20P060-4NR3 Test Circuit Component Designations and Values — 2110-2170 MHz

Part	Description	Part Number	Manufacturer
C1, C7, C8, C15	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C2	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C3	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C4, C5	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C6	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C9, C10, C11, C12, C14	10 μ F Chip Capacitors	C5750X7S2A106M	Kemet
C13	470 μ F, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	5.9 Ω , 1/4 W Chip Resistor	CRCW12065R90FKEA	Vishay
R2, R3	2 K Ω , 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
PCB	0.030", $\epsilon_r = 2.55$	AD255A	Arlon

TYPICAL CHARACTERISTICS

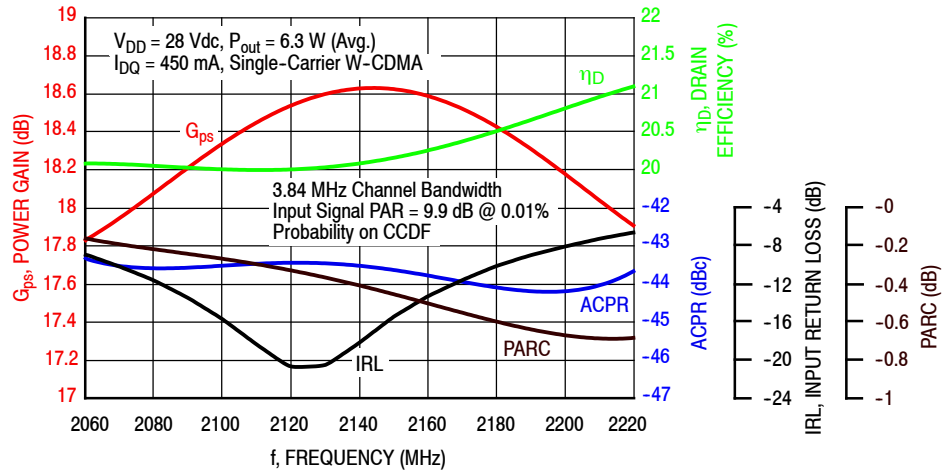


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 6.3$ Watts Avg.

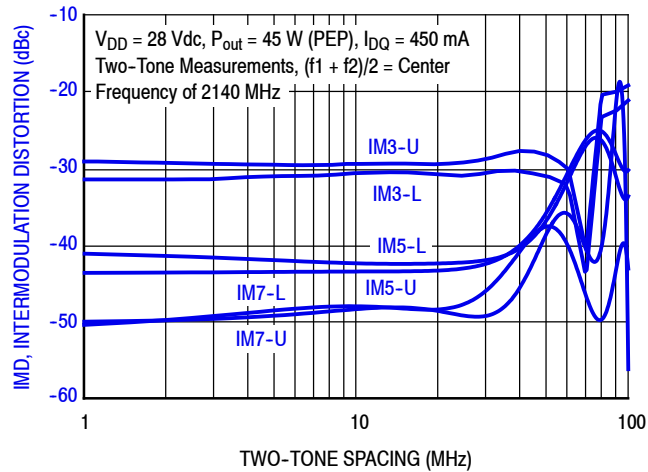


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

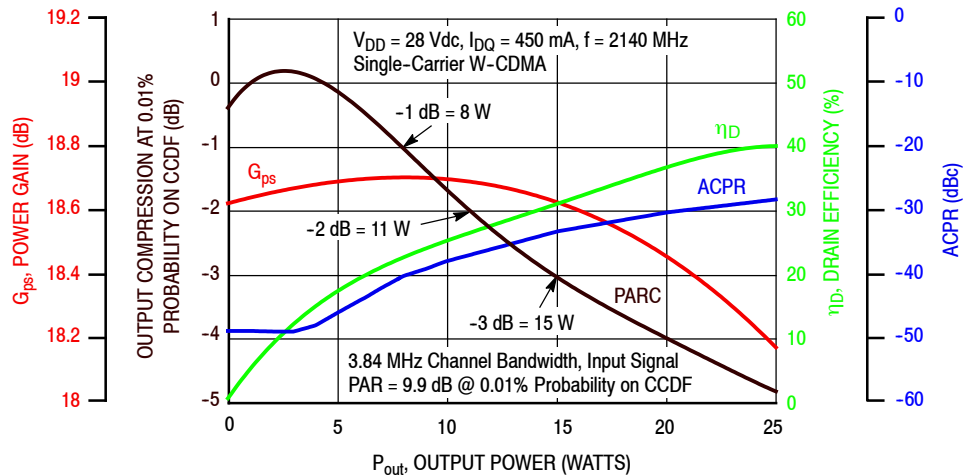


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

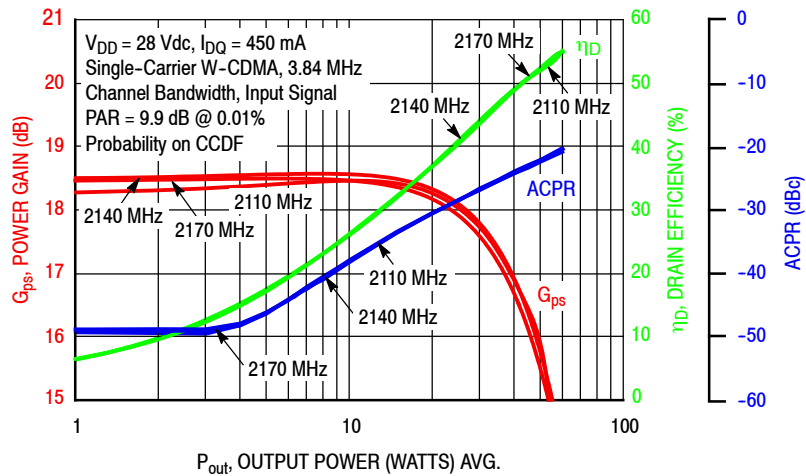


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

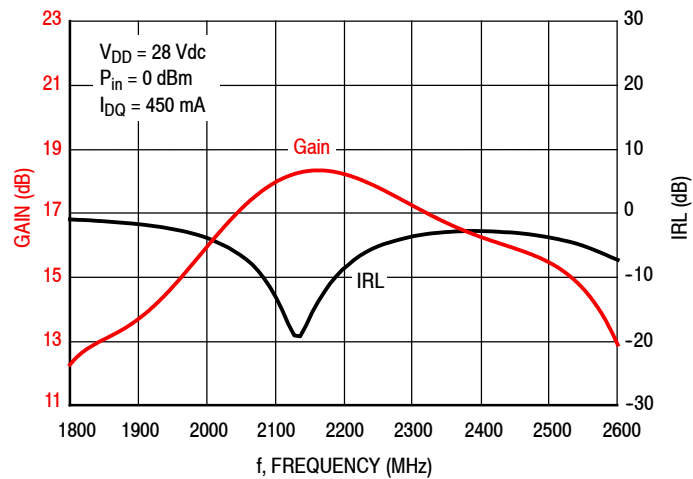


Figure 7. Broadband Frequency Response

ALTERNATE CHARACTERIZATION — 1805-1880 MHz

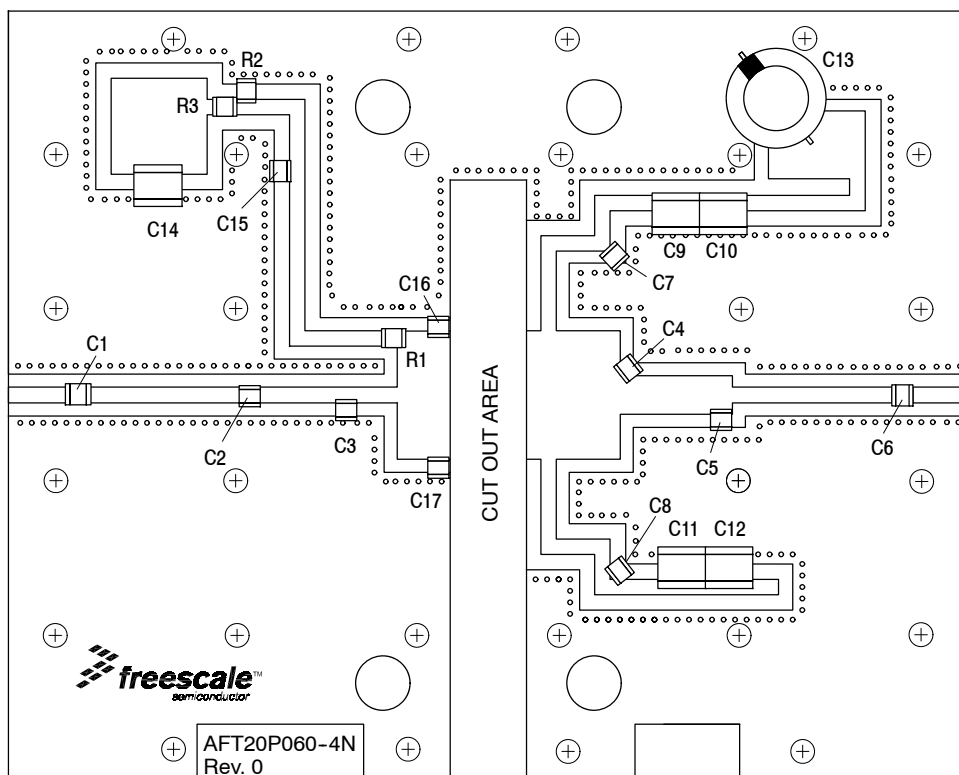


Figure 8. AFT20P060-4NR3 Test Circuit Component Layout — 1805-1880 MHz

Table 7. AFT20P060-4NR3 Test Circuit Component Designations and Values — 1805-1880 MHz

Part	Description	Part Number	Manufacturer
C1	11 pF Chip Capacitor	ATC100B110JT500XT	ATC
C2, C5	1.1 pF Chip Capacitors	ATC100B1R1BT500XT	ATC
C3	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C4	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C6	15 pF Chip Capacitor	ATC100B150JT500XT	ATC
C7, C8, C15	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C9, C10, C11, C12, C14	10 μ F Chip Capacitors	C5750X7S2A106M	Kemet
C13	470 μ F, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C16	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C17	3 pF Chip Capacitor	ATC100B3R0BT500XT	ATC
R1	5.9 Ω , 1/4 W Chip Resistor	CRCW12065R90FKEA	Vishay
R2, R3	2 K Ω , 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
PCB	0.030", $\epsilon_r = 2.55$	AD255A	Arlon

TYPICAL CHARACTERISTICS — 1805-1880 MHz

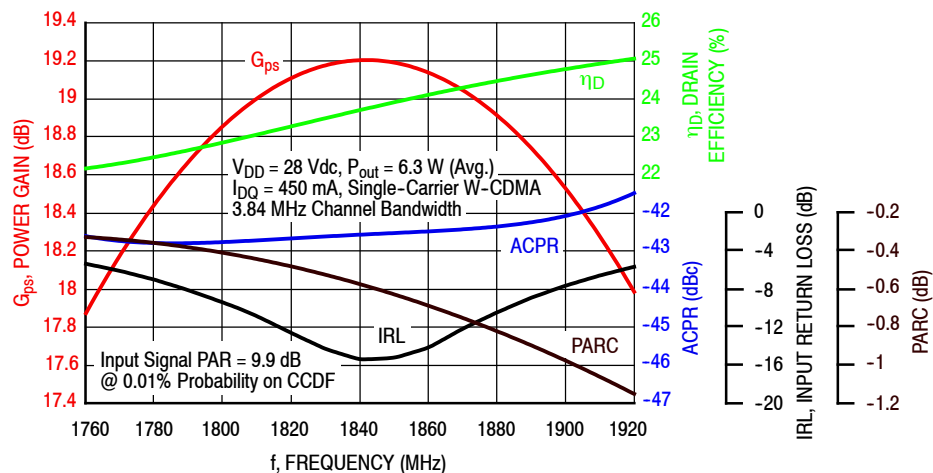


Figure 9. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 6.3$ Watts Avg.

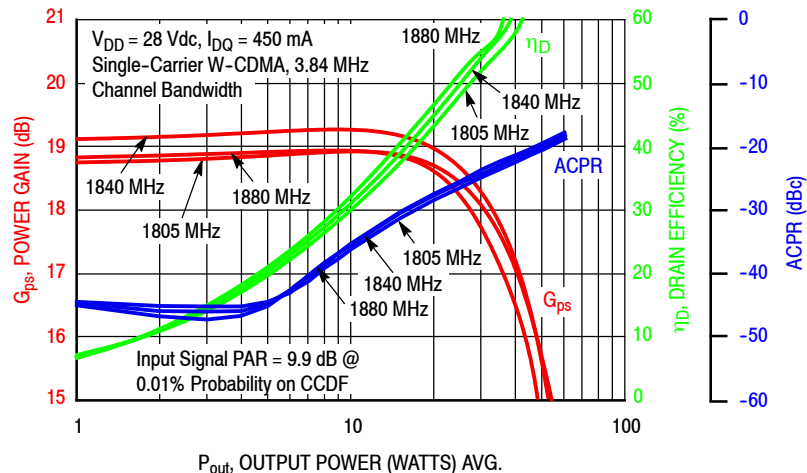


Figure 10. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

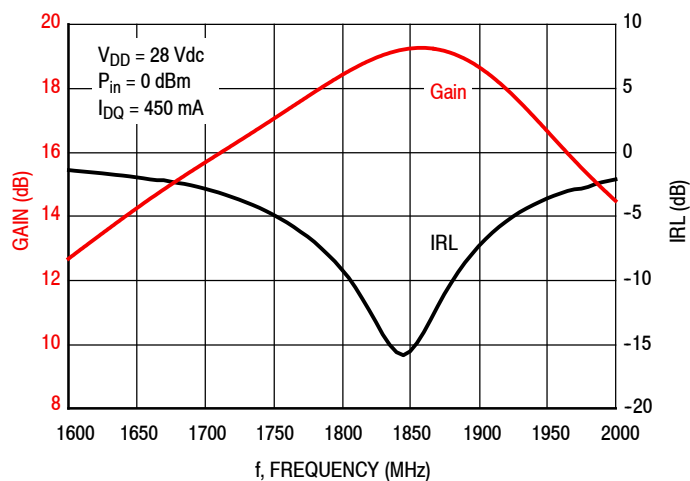
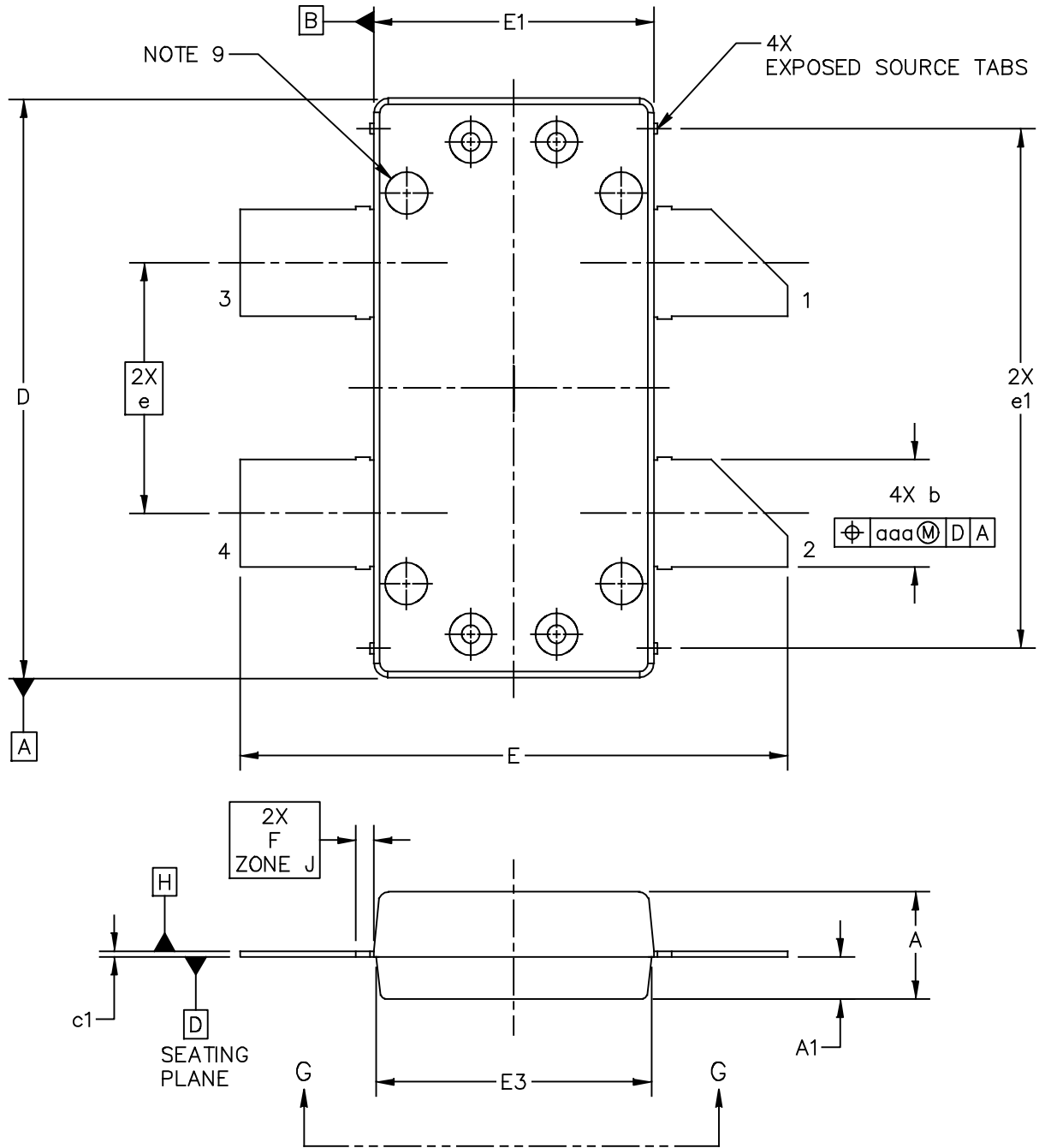


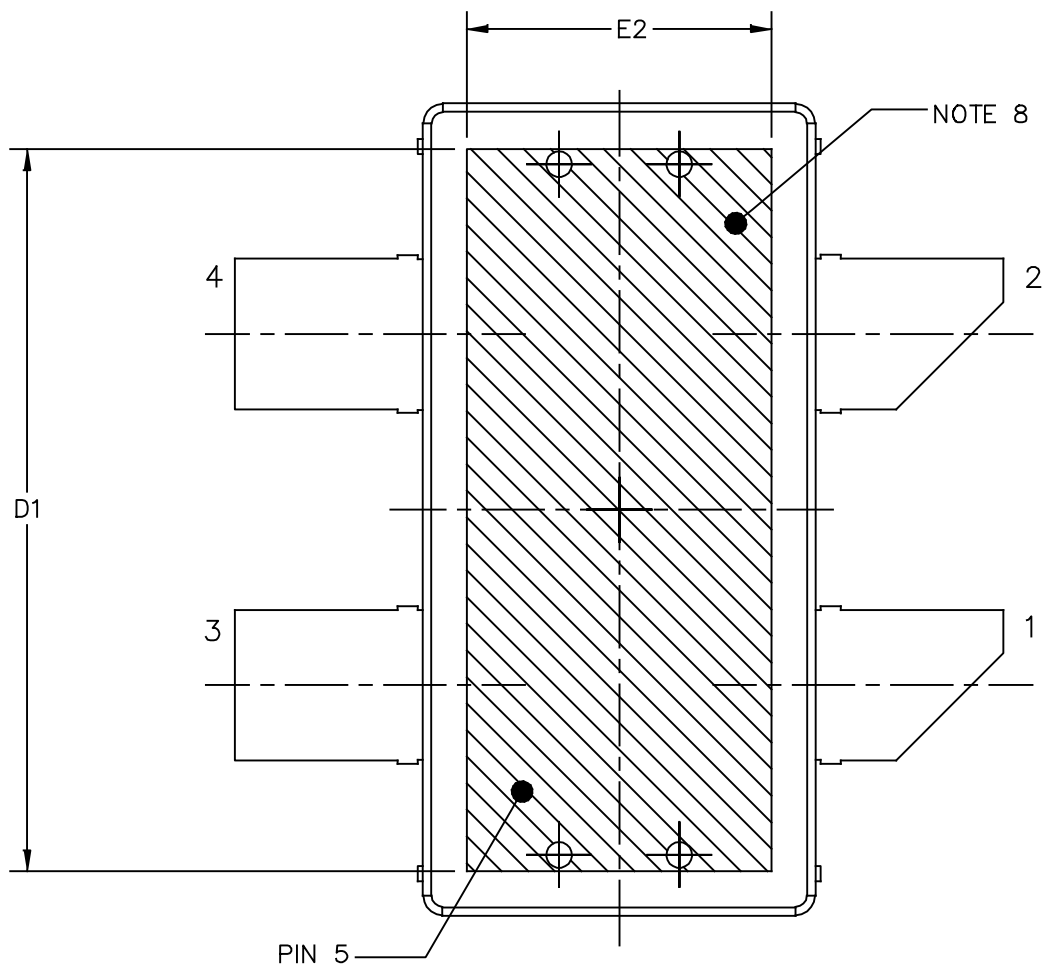
Figure 11. Broadband Frequency Response

PACKAGE DIMENSIONS



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		STANDARD: NON-JEDEC	

AFT20P060-4NR3



BOTTOM VIEW
VIEW G-G

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	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

INCH		MILLIMETER		INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX
A	0.148	.152	3.76	3.86	b	.147	.153
A1	.059	.065	1.50	1.65	c1	.007	.011
D	.808	.812	20.52	20.62	e	.350 BSC	
D1	.720	----	18.29	----	e1	.721	.729
E	.762	.770	19.36	19.56	aaa	.004	0.10
E1	.390	.394	9.91	10.01			
E2	.306	----	7.77	----			
E3	.383	.387	9.72	9.83			
F	.025 BSC		0.635 BSC				
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					CASE NUMBER: 2023—02		10 FEB 2010
					STANDARD: NON—JEDEC		

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2013	• Initial Release of Data Sheet

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