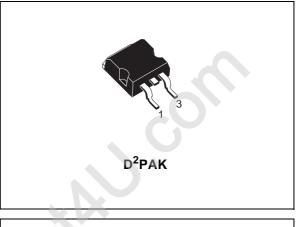
STB90NF03L N-CHANNEL 30V - 0.0056Ω - 90A D<sup>2</sup>PAK LOW GATE CHARGE STripFET™ POWER MOSFET

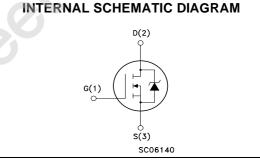
S	ТҮРЕ	V <sub>DSS</sub>	R <sub>DS(on)</sub>	Ι <sub>D</sub>
N	STB90NF03L	30 V	< 0.0065 Ω	90 A

- TYPICAL  $R_{DS}(on) = 0.0056 \Omega$
- TYPICAL Q<sub>g</sub> = 35 nC @ 5V
- OPTIMAL R<sub>DS</sub>(on) x Q<sub>g</sub> TRADE-OFF
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

#### DESCRIPTION

This application specific Power Mosfet is the third generation of STMicroelectronics unique "Single Feature Size<sup>TM</sup>" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.





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#### **APPLICATIONS**

 SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	± 18	V
I <sub>D</sub>	Drain Current (continuos) at T <sub>C</sub> = 25°C	90	А
I <sub>D</sub>	Drain Current (continuos) at T <sub>C</sub> = 100°C	65	A
$I_{DM}(ullet)$	Drain Current (pulsed)	360	А
Ртот	Total Dissipation at $T_C = 25^{\circ}C$	150	W
	Derating Factor	0.73	W/°C
T <sub>stg</sub>	Storage Temperature	55 to 175	°C
Tj	Max. Operating Junction Temperature	- 55 to 175	
ulse width	limited by safe operating area		·

## **ABSOLUTE MAXIMUM RATINGS**

October 2001

## THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
TI	Maximum Lead Temperature For Soldering Purpose	300	°C

# **ELECTRICAL CHARACTERISTICS** (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating $V_{DS}$ = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 18 V			±100	nA

## ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
R <sub>DS(on)</sub>	Static Drain-source On	V <sub>GS</sub> = 10V, I <sub>D</sub> = 45 A		0.0056	0.0065	Ω
	Resistance	$V_{GS} = 5V, I_D = 45 A$		0.007	0.012	Ω

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max,}$ $I_{D} = 45 \text{ A}$		40		S
Ciss	Input Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		2700		pF
Coss	Output Capacitance			860		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			170		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 15V, I <sub>D</sub> = 45 A		30		ns
t <sub>r</sub>	Rise Time	$R_G = 4.7\Omega V_{GS} = 4.5 V$ (see test circuit, Figure 3)		200		ns
Qg	Total Gate Charge	$V_{DD} = 24V, I_D = 90A, V_{GS} = 5V$		35	47	nC
Qgs	Gate-Source Charge			10		nC
Q <sub>gd</sub>	Gate-Drain Charge			18		nC

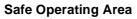
#### SWITCHING OFF

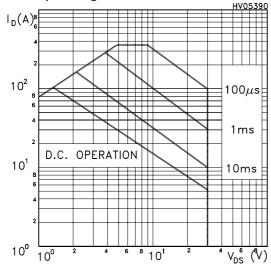
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub>	Turn-off-Delay Time	$V_{DD} = 15V, I_D = 45 \text{ A},$ $R_G = 4.7\Omega, V_{GS} = 4.5 \text{ V}$ (see test circuit, Figure 3)		50		ns
t <sub>f</sub>	Fall Time			105		ns

## SOURCE DRAIN DIODE

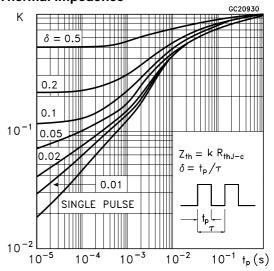
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain Current				90	А
I <sub>SDM</sub> (1)	Source-drain Current (pulsed)				360	А
V <sub>SD</sub> (2)	Forward On Voltage	I <sub>SD</sub> = 90 A, V <sub>GS</sub> = 0			1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD} = 90 \text{ A}, \text{ di/dt} = 100 \text{A/} \mu \text{s},$ $V_{DD} = 15 \text{V}, \text{ T}_{\text{j}} = 150 ^{\circ}\text{C}$ (see test circuit, Figure 5)		80		ns
Qrr	Reverse Recovery Charge			90		nC
I <sub>RRM</sub>	Reverse Recovery Current			2.5		А

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

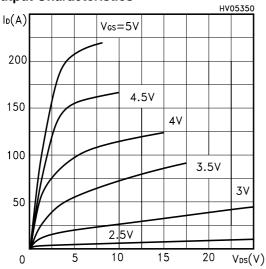




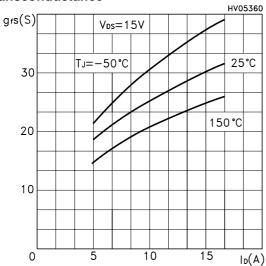
## **Thermal Impedence**



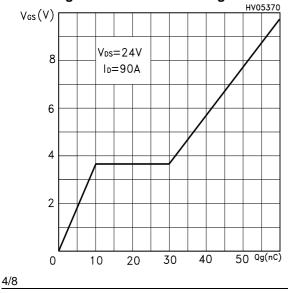
## **Output Characteristics**



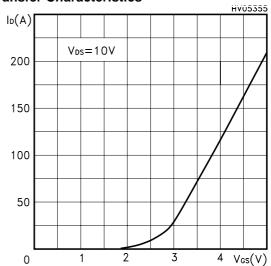
#### Transconductance



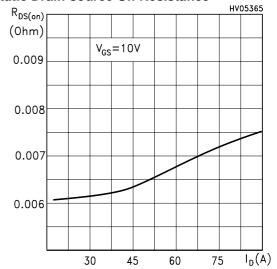
Gate Charge vs Gate-source Voltage

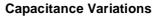


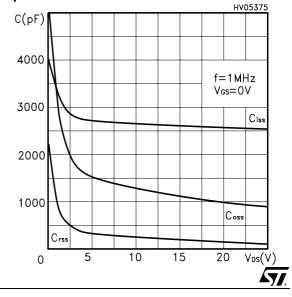


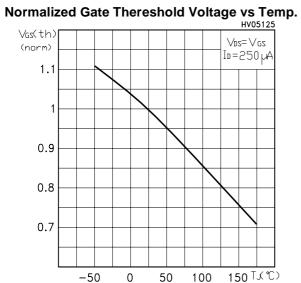


Static Drain-source On Resistance

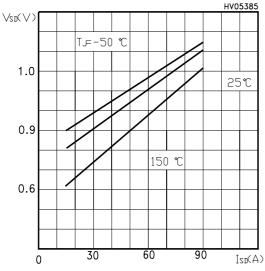








**Source-drain Diode Forward Characteristics** 



Normalized On Resistance vs Temperature Ros(on) (norm) Vcs=10V l₀=45A

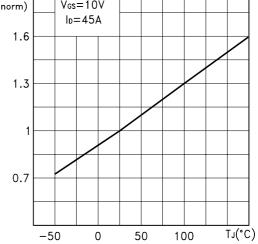
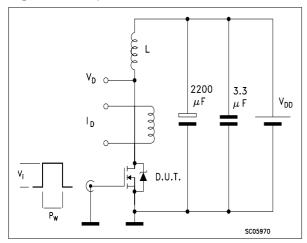
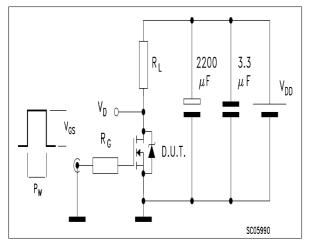


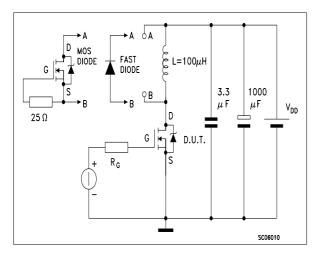
Fig. 1: Unclamped Inductive Load Test Circuit



**Fig. 3:** Switching Times Test Circuit For Resistive Load



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



#### Fig. 2: Unclamped Inductive Waveform

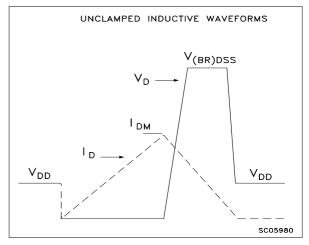
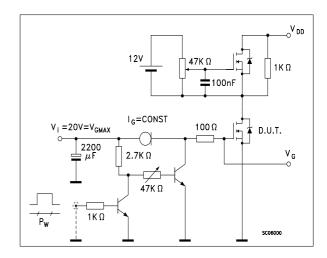


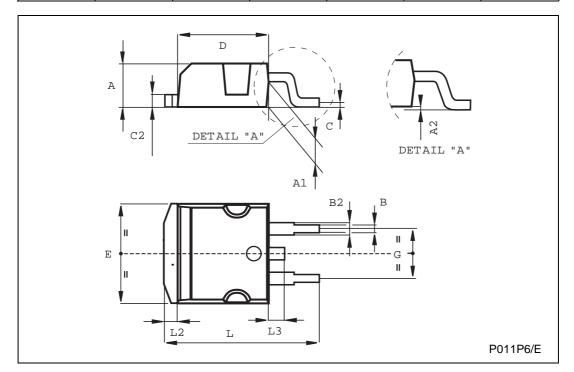
Fig. 4: Gate Charge test Circuit



57.

DIM.		mm			inch		
Dini.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А	4.4		4.6	0.173		0.181	
A1	2.49		2.69	0.098		0.106	
В	0.7		0.93	0.027		0.036	
B2	1.14		1.7	0.044		0.067	
С	0.45		0.6	0.017		0.023	
C2	1.21		1.36	0.047		0.053	
D	8.95		9.35	0.352		0.368	
E	10		10.4	0.393		0.409	
G	4.88		5.28	0.192		0.208	
L	15		15.85	0.590		0.624	
L2	1.27		1.4	0.050		0.055	
L3	1.4		1.75	0.055		0.068	

## TO-263 (D<sup>2</sup>PAK) MECHANICAL DATA



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