# Programmable Peripheral
## PSD7XX Family
### Field-Programmable Microcontroller Peripherals with Supervisory Functions

**Preliminary**

## Introduction

The PSD7XX series is the first family of PSD Field Programmable Microcontroller Peripherals that includes Supervisory Control Functions. PSD7XX devices are used to rapidly implement a highly integrated embedded control system. PSD7XX devices integrate many of the peripheral functions inherent in microcontroller based applications including: EPROM, SRAM, programmable logic, reconfigurable I/O ports, programmable power management, voltage monitor, and WatchDog timer. The PSD7XX family provides a complete solution for microcontroller support and protection.

The PSD7XX family is developed around an innovative "microcontroller-macrocell" logic architecture called the Micro⇔cell. The Micro⇔cell was specifically created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus and the PSD registers which greatly simplifies communication between the MCU and supporting devices.

In addition to the Micro⇔cell based PLD, the PSD7XX offers all of the Supervisory functions needed to monitor embedded system performance. These functions include programmable voltage monitor, WatchDog timer, reset pulse generator and an automatic battery backup of the on-board SRAM. Since the Supervisory functions are fully programmable, the PSD7XX offers the flexibility of using a standard, off the shelf product in a variety of designs under different voltage, reset and clock frequency requirements.

## Key Features

❏ A simple, programmable interface to 8 or 16 bit microcontrollers using either multiplexed or non-multiplexed busses. The bus interface logic directly decodes microcontroller control signals. Microcontroller families supported include the Intel 8031, 80196, 80186, 80C251 and 80386EX; Motorola 68HC11, 68HC16, 68HC12 and 683XX; Philips 8031 and 8051XA; National 16000; Zilog Z80 and Z8; and Neuron 3150.

❏ Three PLDs with 12 Output Micro⇔Cells and 24 Input Micro⇔Cells, 66 inputs and 132 product terms. The PSD7XX PLDs may be used to efficiently implement a variety of logic functions including state machines and address decoders for internal and external control. The PLD also provides seven external chip select outputs and generates control for the WatchDog timer.

❏ Embedded Input and Output Micro⇔Cells enable efficient implementation of user defined system logic functions that require both microcontroller software and hardware interaction.

## Key Features
*(cont.)*

❏ The PSD7XX provides all the supervisory functions required for a microcontroller based system. The supervisory features include:
  – System power supply monitoring with configurable trip points.
  – User programmable WatchDog Timer, controlled by PPLD product terms.
  – Reset generation based on input from:
    1. Voltage comparator with programmable internal or external trip point.
    2. Push button or system reset input.
    3. WatchDog Timer time out.
  – Automatic battery-backup of internal SRAM
  – Write protect of internal SRAM and external battery back up device.
  – Reset input debounce filter.
  – Programmable reset pulse width generator.

❏ Power Management Unit reduces the device standby current to 25 μA typical.

❏ Twenty seven individually configurable I/O Port pins. The Ports may be used as MCU I/Os, PLD I/Os, latched MCU address outputs or special function I/Os. Sixteen I/O port pins can be configured as open drain outputs.

❏ Internal EPROM in densities of 256 Kbit, 512 Kbit and 1 Mbit, configurable in eight or sixteen-bit widths. The EPROM is divided into eight equal-size blocks, accessible by user-specified addresses. The access time includes address latching and PLD decoding. The EPROM includes a low power option.

❏ Internal 4 Kbit SRAM can be configured in eight or sixteen-bit data widths. The SRAM retains data if power is lost by automatically switching to standby power.

❏ A page register expands the microcontroller address space by a factor of sixteen.

❏ A security bit prevents copying the PSD7XX configuration and PLD logic as well as the EPROM contents on device programmers.

❏ The programmable Power Management Unit (PMU) supports two separate, low-power modes allowing operations with as little as 25 μA (at 5V $V_{CC}$). The device can automatically detect a lack of microcontroller activity and put the PSD into power down mode.

❏ The devices are available in EPROM versions. The ceramic package is ideal for prototyping and low-volume production, and in OTP versions for high-volume, low-cost applications.

❏ Package choices include 52 pin plastic (J) and ceramic (L) chip carriers.

❏ PSD7XX family development is supported by the WSI PC based PSDsoft™ design system. The software is MS-Windows® and Windows 95 compatible. The suite includes PSDabel™ (ABEL®), to specify  the PLD logic, and an efficient fitter. The tool also includes the PSDsilosIII simulator from SIMUCAD™. The MagicPro® III programmer is an engineering development tool and can program any PSD device.

Please refer to the revision block at the end of this document for updated information.

# PSD7XX Architectural Overview (cont.)

## Figure 1.  PSD7XX Block Diagram
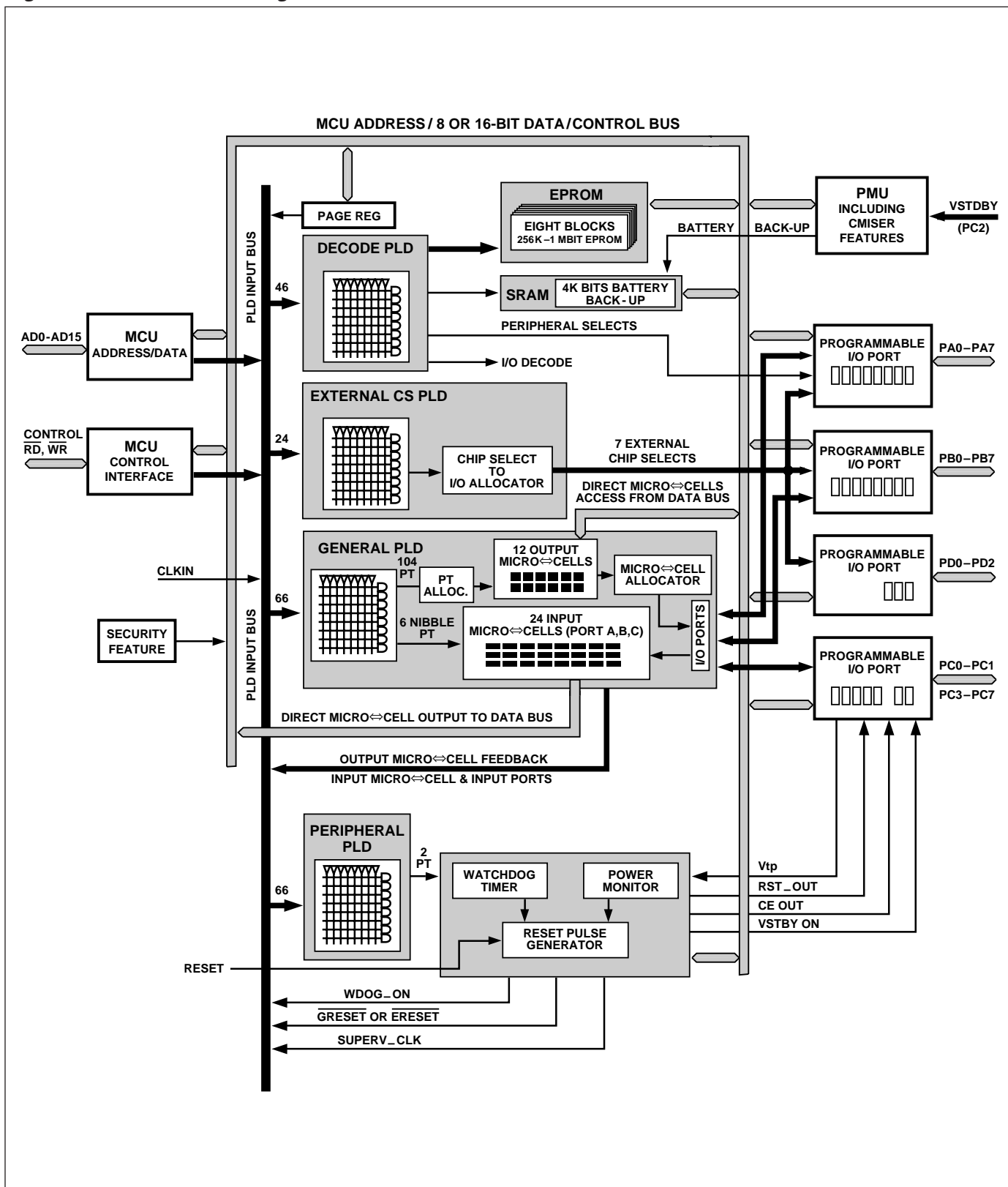
## *General Information*

The PSD7XX family of Field Programmable Microcontroller Peripherals combines supervisory control functions, memory, PLD and innovative system architecture to provide a user-programmable, feature rich, low-power solution to microcontroller system design. The user programmable supervisory functions integrated inside the PSD7XX protect embedded systems from failure due to sudden loss of power, power supply glitches, signal corruption, and memory loss. The high level of integration of the PSD7XX device dramatically reduces the number of discrete components greatly simplifying embedded system development.

## *Development System*

The PSD7XX family is supported by the Windows-based PSDsoft Development System. The PSDsoft design flow is shown in Figure 2. The PLD design entry is done using PSDabel, which creates a minimized logic implementation, and provides logic simulation of the PLDs. The PSD7XX Bus Interface, I/O Port configuration, and Supervisory Function settings are entered in PSDconfiguration.

The PSDcompiler, comprised of a fitter and an address translator, generates an object file from the PSDabel, PSDconfiguration and MCU code files. The object file is then downloaded to a programmer (MagicPro III, Data I/O, or other third party programmer for device programming) or to the PSDsimulator (PSDsilos III Logic simulator) for device-level simulation.

### *Figure 2.  PSDsoft Development Tools*
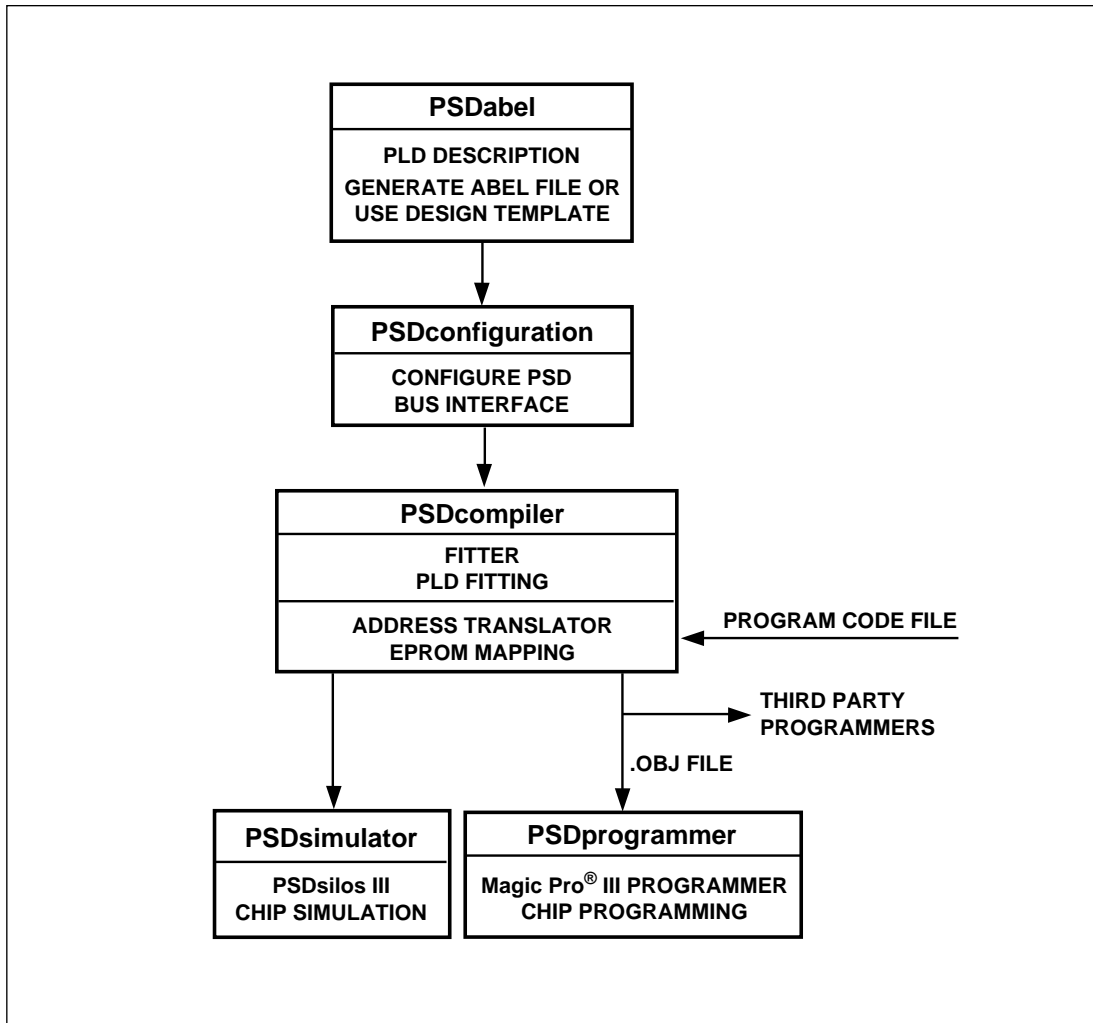
## *Device Versions*

The PSD7XX window package versions are ideal for general purpose embedded systems development. The PSD7XX OTP versions deliver the lowest cost PSD7XX solution.

## *PSD7XX Family*

There are 6 devices in the PSD7XX family. The part classifications are based on EPROM size and data bus width. The features of each part are listed in Table 1.

### *Table 1. PSD7XX Product Matrix*

| Part # | Bus Width | I/O Pins | EPROM K Bit | SRAM K Bit |
|--------|-----------|----------|-------------|------------|
| PSD701S5 | x8/x16 | 27 | 256 | 4 |
| PSD711S5 | x8 | 27 | 256 | 4 |
| PSD702S5 | x8/x16 | 27 | 512 | 4 |
| PSD712S5 | x8 | 27 | 512 | 4 |
| PSD703S5 | x8/x16 | 27 | 1024 | 4 |
| PSD713S5 | x8 | 27 | 1024 | 4 |

**Table 2.**
**PSD7XX Pin**
**Descriptions**

The following table describes the pin names and pin functions of the PSD7XX. Pins that have multiple names and/or functions are defined by configuration.

| Pin Name | Pin | Type | Function Description |
|---|---|---|---|
| ADIO0–7 | 30–37 | I/O | Address/Data Port, interface to Microcontroller Bus<br>1. Input pins for multiplexed low order address/data byte. ALE or AS latches address A0-7. The PSD drives data out only if read is active and one of the internal PSD functional blocks is selected.<br>2. Address A0-7 inputs for non-multiplexed bus or 80C251 mode<br>3. A4/D0-A11/D7 inputs in 80C51XA mode<br>4. Address (or latched address) inputs to PLD |
| ADIO8–15 | 39–46 | I/O | Address/Data Port, interface to Microcontroller Bus<br>1. Address A8-15 inputs in 8-bit data bus mode, or as multiplexed high order address/data byte inputs in 16-bit data bus mode. ALE or AS latches address A8-15. The PSD drives data out only if read is active and one of the internal PSD functional blocks is selected.<br>2. Address A8-15 inputs in non-multiplexed bus mode<br>3. AD8-AD15 inputs in 80C251 mode<br>4. A12-A19 or A12/D8 - A19/D15 inputs in 80C51XA mode<br>5. Address (or latched address) inputs to PLD |
| CNTL0)<br><br>($\overline{WR}$,<br>R_$\overline{W}$,<br>$\overline{WRL}$) | 47 | I | Write Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be:<br>1. $\overline{WR}$ – active low write input<br>2. R_$\overline{W}$ – read/write pin, low for write bus cycle<br>3. $\overline{WRL}$ – for 16 bit data bus only, write to low byte, active low<br>4. Control signal (CNTL0) input to PLD |
| CNTL1<br><br>($\overline{RD}$,<br>E,<br>$\overline{DS}$,<br>$\overline{LDS}$,<br>$\overline{PSEN}$) | 50 | I | Read or Data Strobe  Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be:<br>1. $\overline{RD}$ – active low read input<br>2. E – E clock input.<br>During a write bus cycle, E is high and R/W is low<br>During a read bus cycle, E is high and R/W is high<br>3. $\overline{DS}$ – Data Strobe, active low<br>4. $\overline{LDS}$ – Strobe for low data byte, 16-bit data bus mode, active low<br>5. $\overline{PSEN}$ – Program Select Enable, active low in read bus cycle (80C251 configuration)<br>6. Control signal (CNTL1) input to PLD |
| CNTL2<br><br>($\overline{PSEN}$,<br>$\overline{BHE}$,<br>$\overline{UDS}$,<br>SIZ0) | 49 | I | Read or other Control input pin with multiple configurations. Depending on the MCU interface selected, this pin can be:<br>1. $\overline{PSEN}$ – Program Select enable, active low in code fetch bus cycle<br>2. $\overline{BHE}$ – High byte enable, 16-bit data bus<br>3. $\overline{UDS}$ – Strobe for high data byte, 16-bit data bus mode, active low<br>4. SIZ0 – Byte enable input<br>5. Control signal (CNTL2) input or general input to PLD |

*Table 2.*
*PSD7XX Pin Descriptions*
*(cont.)*

| Pin Name | Pin | Type | Function Description |
|---|---|---|---|
| $\overline{\text{Reset}}$ | 48 | I | Active low input. Resets I/O Ports, PLD Micro⇔Cells and some of the Configuration Registers. Must be active at power up. |
| PA0<br>PA1<br>PA2<br>PA3 | 29<br>28<br>27<br>25 | I/O | Port A, PA0 – 3.  This port is pin configurable and has multiple functions:<br>1. MCU I/O – standard output or input port<br>2. External chip select (ECSPLD) output, or  input to GPLD<br>3. Latched address outputs (see Table 4)<br>4. As Address A0-3 inputs in 80C51XA mode<br>5. As Data Bus Port  (D0–3) in non-multiplexed bus configuration<br>6. Peripheral I/O mode |
| PA4<br>PA5<br>PA6<br>PA7 | 24<br>23<br>22<br>21 | I/O<br>CMOS<br>or<br>Open<br>Drain | Port A, PA4–7.  This port is pin configurable and has multiple functions:<br>1. MCU I/O – standard output or input port<br>2. GPLD Micro⇔Cell (McellAB) output or input<br>3. Latched address outputs (see Table 4)<br>4. As Data Bus Port (D4–7) in non-multiplexed bus configuration<br>5. Peripheral I/O mode |
| PB0<br>PB1<br>PB2<br>PB3 | 7<br>6<br>5<br>4 | I/O | Port B, PB0–3.  This port is pin configurable and has multiple functions:<br>1. MCU I/O – standard output or input port<br>2. External chip select (ECSPLD) output, or input to GPLD<br>3. Latched address outputs (see Table 4)<br>4. As Data Bus Port (D8-11) in non-multiplexed bus configuration with 16-bit data bus |
| PB4<br>PB5<br>PB6<br>PB7 | 3<br>2<br>52<br>51 | I/O<br>CMOS<br>or<br>Open<br>Drain | Port B, PB4–7. This port is pin configurable and has multiple functions:<br>1. MCU I/O – standard output or input port<br>2. GPLD Micro⇔Cell (McellAB) output or input<br>3. Latched address outputs (see Table 4)<br>4. As Data Bus Port  (D12–15) in non-multiplexed bus configuration with 16-bit data bus |
| PC0<br>PC1<br>PC2<br>PC3<br>PC4<br>PC5<br>PC6<br>PC7 | 20<br>19<br>18<br>17<br>14<br>13<br>12<br>11 | I/O<br><br><br>CMOS<br>or<br>Open<br>Drain | This port is pin configurable and has multiple functions:<br>1. MCU I/O – standard output or input port<br>2. GPLD Micro⇔Cell (McellC) output or input<br>3. PC7 pin only – Write strobe ($\overline{\text{WRH}}$) input for high byte. Active low for 16-bit MCU with $\overline{\text{WRH}}$<br>4. Supervisory Function (pin PC1–PC6), see Table 3. |

*Table 2.*
*PSD7XX Pin*
*Descriptions*
*(cont.)*

| Pin Name | Pin | Type | Function Description |
|---|---|---|---|
| PD0 (ALE) | 10 | I/O | Port D Pin PD0 can be configured as:<br>1. ALE input - latches addresses on ADIO0–15 pins<br>2. MCU I/O<br>3. GPLD input<br>4. ECSPLD output |
| PD1 (CLKIN) | 9 | I/O | Port D Pin PD1 can be configured as:<br>1. MCU I/O<br>2. GPLD input<br>3. External chip select (ECSPLD) output<br>4. CLKIN clock input – clock input to the GPLD Micro⇔Cells, the APD power down counter and GPLD AND Array |
| PD2 ($\overline{CSI}$) | 8 | I/O | Port D Pin PD2 can be configured as:<br>1. MCU I/O<br>2. GPLD input<br>3. External (ECSPLD) output<br>4. $\overline{CSI}$ input – When low, the $\overline{CSI}$ enables the PSD EPROM/SRAM. When high, the EPROM/SRAM are disabled to conserve power |
| $V_{CC}$ | 15<br>38 | | Power pins |
| GND | 1<br>16<br>26 | | Ground pins |

*Table 3.*
*PSD7XX*
*Supervisory*
*I/O Pins*

| Pin Name | Pin | Type | Function Description |
|---|---|---|---|
| PC1 ($\overline{RST\_OUT}$) | 19 | O | Active low reset output. |
| PC2 (VSTBY) | 18 | I | SRAM Standby Voltage (battery) input. |
| PC3 (CEOUT) | 17 | O | Chip select output that can be used for external non-volatile writable memory. This chip select becomes inactive automatically when the PSD7XX is switched to standby voltage. Use to conserve power in external battery backup SRAM or prevent unwanted writes to external EEPROM, SRAM, or FLASH. |
| PC4 (VSTBYON) | 14 | O | Pin is driven high when PSD7XX is switched over to Standby Voltage. |
| PC5 (RST_OUT) | 13 | O | Active high reset output. |
| PC6 (VTP) | 12 | I | External Reference voltage input for the Voltage Comparator. |

## I/O Port Latched Address Output Assignments*

### Table 4.  Latched Address Outputs

| Microcontroller | Port A (3:0) | Port A (7:4) | Port B (3:0) | Port B (7:4) |
|---|---|---|---|---|
| 8051XA (8-Bit) | N/A | Address [7:4] | Address [11:8] | N/A |
| 80C251 (Page Mode) | N/A | N/A | Address [11:8] | Address [15:12] |
| All Other 8-Bit Multiplexed | Address [3:0] | Address [7:4] | Address [3:0] | Address [7:4] |
| 8051XA (16-Bit) | N/A | Address [7:4] | Address [11:8] | Address [15:12] |
| All Other 16-Bit Multiplexed | Address [3:0] | Address [7:4] | Address [11:8] | Address [15:12] |
| 8-bit Non-Multiplexed Bus | N/A | N/A | Address [3:0] | Address [7:4] |

N/A = Not Applicable

*Refer to the I/O Port Section on how to enable the Latched Address Output function.

## PSD7XX Register Description and Address Offset

Tables 5 and 5A show the offset address to the PSD7XX registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD7XX registers. Some Motorola 16-bit microcontrollers, including the M68HC16, M68302 and M683XX, have a different data byte orientation requiring separate address offset maps.

Table 5 shows the CSIOP address offsets for all MCUs except those from Motorola in 16-bit mode. Table 5A shows the address offsets for Motorola MCUs in 16-bit mode.

*PSD7XX Register Description and Address Offset (cont.)*

**Table 5. Register Address Offset**

| Register Name | Port A | Port B | Port C | Port D | Other* | Description |
|---|---|---|---|---|---|---|
| Data In | 00 | 01 | 10 | 11 | | Reads Port pin as input, MCU I/O input mode |
| Control | 02 | 03 | | | | Selects mode between MCU I/O or Address Out |
| Data Out | 04 | 05 | 12 | 13 | | Stores data for output to Port pins, MCU I/O output mode |
| Direction | 06 | 07 | 14 | 15 | | Configures Port pin as input or output |
| Drive | 08 | 09 | 16 | 17 | | Configures Port pin between CMOS, Open Drain and Slew Rate |
| Input Micro⇔Cell | 0A | 0B | 18 | | | Reads Input Micro⇔Cell |
| Enable Out | 0C | 0D | 1A | | | Reads the status of the output enable to the I/O Port driver |
| Output Micro⇔Cell | 20 | 20 | 21 | | | Read – reads output of Micro⇔Cells (McellC, McellAB)<br>Write – loads Micro⇔cell Flip-Flops |
| PMMR0 | | | | | B0 | Power Management Register 0 |
| PMMR1 | | | | | B2 | Power Management Register 1 |
| Page | | | | | E0 | Page Register |
| VM | | | | | E2 | 8031/PIO Configuration Register |
| Status | | | | | D8 | Read only Supervisory register. Indicates the status and source of reset and reference voltage level. |
| Reset-Clr | | | | | D6 | Write only. A write to the register clears the reset status bits in the Status Register. |
| Supv-Pins | | | | | DA | Read only. Indicates the status of all Supervisory I/O pins. |
| WD-Conf | | | | | D4 | Read only. Indicates the configuration of the WatchDog Timer. |
| WD-Count | | | | | D0 | Contains WatchDog Timer count bits 0–7. |
| WD-Misc | | | | | D2 | Contains WatchDog Timer count bit 8, the clock source and reset pulse width. |

*Other registers that are not part of the I/O ports.

*PSD7XX*
*Register*
*Description*
*and Address*
*Offset*
*(cont.)*

**Table 5A.  Register Address Offset for 16-Bit Motorola Microcontrollers in 16-Bit Mode**

| Register Name | Port A | Port B | Port C | Port D | Other* | Description |
|---|---|---|---|---|---|---|
| Data In | 01 | 00 | 11 | 10 | | Reads Port pin as input, MCU I/O input mode |
| Control | 03 | 02 | | | | Selects mode between MCU I/O or Address Out |
| Data Out | 05 | 04 | 13 | 12 | | Stores data for output to Port pins, MCU I/O output mode |
| Direction | 07 | 06 | 15 | 14 | | Configures Port pin as input or output |
| Drive | 09 | 08 | 17 | 16 | | Configures Port pin between CMOS, Open Drain and Slew rate |
| Input Micro⇔Cell | 0B | 0A | 19 | | | Reads Input Micro⇔Cell |
| Enable Out | 0D | 0C | 1B | | | Reads the status of the output enable to the I/O Port driver |
| Output Micro⇔Cell | 21 | 21 | 20 | | | Read – reads output of Micro⇔Cells (McellC, McellAB) Write – loads Micro⇔cell Flip-Flops |
| PMMR0 | | | | | B1 | Power Management Register 0 |
| PMMR1 | | | | | B3 | Power Management Register 1 |
| Page | | | | | E1 | Page Register |
| VM | | | | | E3 | 8031/PIO Configuration Register |
| Status | | | | | D9 | Read only Supervisory register. Indicates the status and source of reset and reference voltage level. |
| Reset-Clr | | | | | D7 | Write only. A write to the register clears the reset status bits in the Status Register. |
| Supv-Pins | | | | | DB | Read only. Indicates the status of all Supervisory I/O pins. |
| WD-Conf | | | | | D5 | Read only. Indicates the configuration of the WatchDog Timer. |
| WD-Count | | | | | D1 | Contains WatchDog Timer count bits 0–7. |
| WD-Misc | | | | | D3 | Contains WatchDog Timer count bit 8, the clock source and reset pulse width. |

*Other registers that are not part of the I/O ports.

## PSD7XX Architectural Overview

PSD7XX devices consist of several major functional blocks. Figure 1 shows the architecture of the PSD7XX family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions, and are user configurable.

### PLDs

The device contains four PLD blocks each optimized for a different function as shown in Table 6. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance and ease of design entry.

The Decode PLD (DPLD) is used to decode and generate chip selects for the PSD7XX internal memory, registers and peripheral mode. The External Chip Select PLD (ECSPLD) is optimized to generate chip selects for devices external to the PSD7XX. The General Purpose PLD (GPLD) can implement user defined logic functions. The DPLD and ECSPLD have combinatorial outputs while the GPLD has 12 Output Micro⇔Cells. The PSD7XX also has 24 Input Micro⇔Cells that can be configured as inputs to the PLD. The PLDs receive their inputs from the PLD Input bus and are differentiated by their output destinations, number of product terms, and Micro⇔Cells.

The Peripheral PLD (PPLD) is dedicated to generate control signals for the WatchDog timer.

### Table 6.

| Name | Abbreviation | Inputs | Outputs | Product Terms |
|---|---|---|---|---|
| Decode PLD | DPLD | 46 | 12 | 13 |
| External Chip Select PLD | ECSPLD | 24 | 7 | 7 |
| General PLD | GPLD | 66 | 12 | 110 |
| Peripheral PLD | PPLD | 66 | 2 | 2 |

### I/O Ports

The PSD7XX has 27 I/O pins divided among four ports. Each I/O pin can be individually configured to provide many functions. Ports A, B, C and D can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

Ports A and B can also be configured as a data port for microcontrollers with a non-multiplexed bus. In these modes, Port A is connected to D0–7 and Port B to D8–15.

### Supervisory Functions

The PSD7XX provides all the supervisory functions required for an embedded system.

A voltage comparator monitors the system power supply and generates a reset if $V_{CC}$ drops below internal or external reference voltages (hysterisis included). The polarity and duration of the reset output signal is programmable.

A noise filter for the reset input is provided to debounce the source (pushbutton or other).

The internal PSD7XX SRAM is automatically switched to standby voltage if $V_{CC}$ drops below the standby voltage value. When switchover occurs, the internal SRAM is write protected and a single user defined chip select output immediately goes inactive. This special chip select supports the use of an additional external battery backup SRAM (to ensure low power consumption during a fault) or provides protection against inadvertent writes to external FLASH or EEPROM.

A WatchDog timer is provided to monitor software integrity. Normal program flow will continually reset the WatchDog timer. However, if program flow malfunctions and hangs up, the timer will timeout and reset the system. This 9-bit WatchDog timer is programmable and can supply its own independent clock source.

*PSD7XX
Architectural
Overview
(cont.)*

### Microcontroller Bus Interface

The PSD7XX easily interfaces with most popular eight and sixteen-bit microcontrollers with either multiplexed or non-multiplexed address/data busses. The device is configured to respond to the microcontroller control signals which are also used as inputs to the PLDs.

### Memory

The PSD7XX contains EPROM and SRAM. The EPROM densities available are 256 Kbit, 512 Kbit and 1 Mbit. The memory space is divided into eight equally-sized blocks. Each block can be located in a different address space defined by the user. The access time of the EPROM includes the address latching and DPLD decoding.

The 4 Kbit SRAM may be used as a scratch pad memory and an extension of the microcontroller SRAM.  The SRAM data is retained  in the event of a system power down, provided a backup battery is connected to the Vstby pin (PC2). Switching from the $V_{CC}$ supply to standby power occurs automatically when $V_{CC}$ drops below Vstby voltage.

### Page Register

The four-bit Page Register expands the address range of the microcontroller by sixteen times.  The paged address can be used as part of the address space to access external memory  and peripherals or internal EPROM, SRAM and I/O.

### Power Management Unit

The Power Management Unit (PMU) in the PSD7XX enables the user to control the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power Down unit (APD) that will turn off device functions due to microcontroller inactivity in one of two modes: the Power Down mode and Sleep mode.

Other power saving features, such as the CMiser in the PMU, allow the EPROM/SRAM to operate at a slower rate to conserve power.

## *The PSD7XX Functional Blocks*

The PSD7XX consists of five major functional blocks:

❏ *PLD Block*
❏ *Bus Interface*
❏ *I/O Ports*
❏ *Memory Block*
❏ *Power Management Unit*
❏ *Supervisory Function*

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

## *PLDs*

The PLDs bring programmable logic functionality to the PSD7XX. After specifying the logic for the PLDs by using the PSDabel tool in PSDsoft, the logic configuration is programmed into the device and available when power is applied.

The PLDs (DPLD, ECSPLD, GPLD, and PPLD) consist of an AND array. The GPLD architecture includes 12 Output Micro⇔Cells in addition to the AND array. There are 24 Input Micro⇔Cells that can be configured as inputs to the PLD. Figure 3 shows the organization of the PLD.

The AND array is used to form product terms specified using the PSDabel tool in the PSDsoft development system. When the inputs used in a term are true, the output is active. The GPLD Input Bus consists of 66 signals as shown in Table 7. Both the true and complement value of inputs are available to the AND array. The DPLD and ECSPLD Input Busses consists of fewer inputs and is a subset of the 66 inputs.
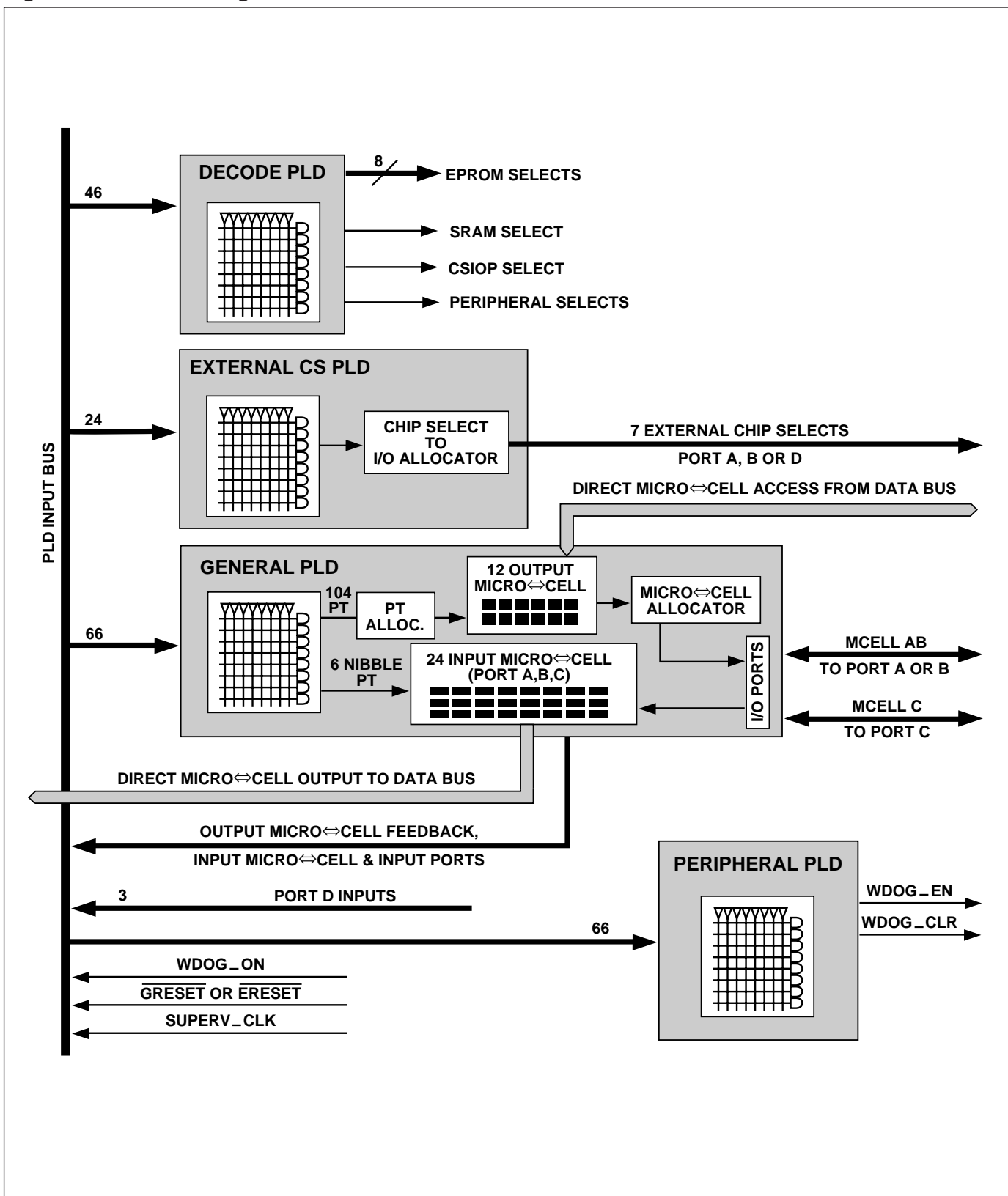
### *Table 7.  GPLD Inputs*

| *Input Source* | *Input Name* | *Number of Signals* |
|---|---|---|
| MCU Address Bus | A[15:0]* | 16 |
| MCU Control Signals | CNTL[2:0] | 3 |
| Power Down | PDN | 1 |
| I/O Ports Inputs (Input Micro⇔Cells) | PA[7:0], PB[7:0], PC[7:0] | 24 |
| Port D Inputs | PD[2:0] | 3 |
| Page Register | PGR[3:0] | 4 |
| Port A or B Micro⇔Cell Feedback | MCELLAB.FB[7:4] | 4 |
| Port C Micro⇔Cell Feedback | MCELLC.FB[7:0] | 8 |
| Supervisory Function WatchDog Time Out | WDOG_ON | 1 |
| Supervisory Function Global Reset or Expanded Reset | $\overline{\text{GRESET}}$ or $\overline{\text{ERESET}}$ | 1 |
| Supervisory Clock 2KHz Internal Oscillator or CLKIN/8192 | Superv_CLK | 1 |

*NOTE:  The address inputs are A[19:4] in 80C51XA mode.

## *PLDs* (cont.)
### *Figure 3. PLD Block Diagram*



**DECODE PLD**

8 → EPROM SELECTS

→ SRAM SELECT

→ CSIOP SELECT

→ PERIPHERAL SELECTS

46

**EXTERNAL CS PLD**

24

CHIP SELECT TO I/O ALLOCATOR

7 EXTERNAL CHIP SELECTS
PORT A, B OR D

DIRECT MICRO⇔CELL ACCESS FROM DATA BUS

**GENERAL PLD**

104 PT

PT ALLOC.

12 OUTPUT MICRO⇔CELL

MICRO⇔CELL ALLOCATOR

66

6 NIBBLE PT

24 INPUT MICRO⇔CELL (PORT A,B,C)

I/O PORTS

MCELL AB
TO PORT A OR B

MCELL C
TO PORT C

DIRECT MICRO⇔CELL OUTPUT TO DATA BUS

OUTPUT MICRO⇔CELL FEEDBACK,
INPUT MICRO⇔CELL & INPUT PORTS

3   PORT D INPUTS

**PERIPHERAL PLD**

66

WDOG_EN

WDOG_CLR

WDOG_ON

GRESET OR ERESET

SUPERV_CLK

PLD INPUT BUS

**PLDs**
*(cont.)*

Each of the three PLDs has unique characteristics suited for its applications. They are described in the following sections.

### Decode PLD

The Decode PLD (DPLD), shown in Figure 4, is used to select the internal PSD7XX functions: EPROM blocks, SRAM, Registers (CSIOP) and the Port A Peripheral Mode. All the select signals are active high and have one product term, except ES7 which has two. The CSIOP is the select line for the PSD7XX internal registers that occupies 256 bytes of memory space. A second level decoder selects a register based on the address inputs A[7-0].

Each EPROM block has its own chip select. The chip select of the eighth EPROM block has two product terms, ES7A and ES7B. This allows the eighth block to reside in two memory spaces, where ES7B can typically select reset vectors or configuration bytes that are stored in the MCU address space.

PSEL 0 & 1 are used as inputs to Port A to control the port's Peripheral I/O mode operation. Usually PSEL 0&1 are defined in term of the MCU address inputs. This mode is explained in the I/O Port section.
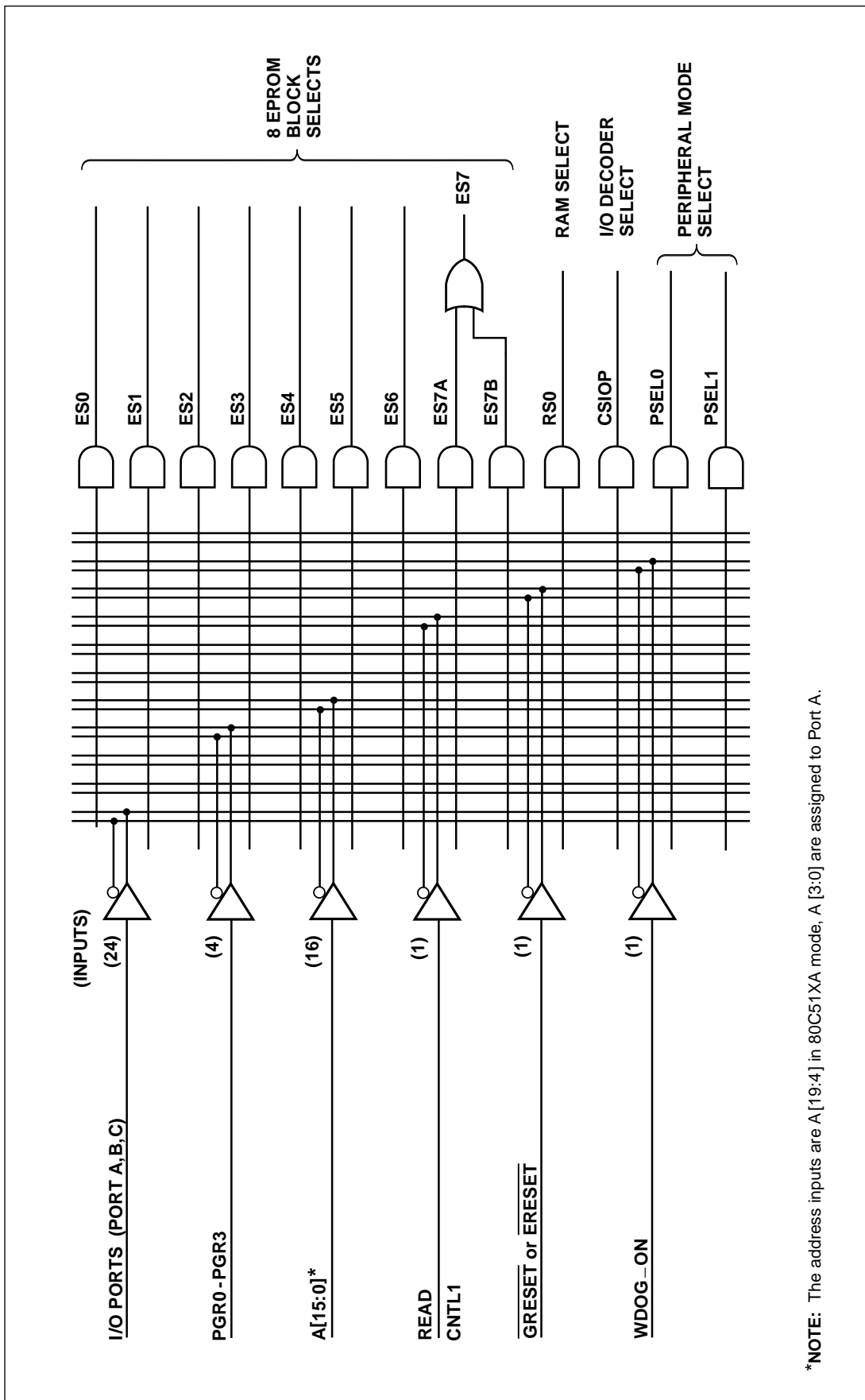
### Table 8. DPLD Inputs

| Input Source | Input Name | Number of Bits |
|---|---|---|
| MCU Address Bus | A[15:0]* | 16 |
| I/O Ports<br>Port A, B, C | PA[7:0], PB[7:0],<br>PC[7:0] | 24 |
| Page Register | PGR[3:0] | 4 |
| Control Signal | CNTL1 (Read) | 1 |
| Supervisory Function | $\overline{\text{GRESET}}$ or $\overline{\text{ERESET}}$ | 1 |
| Supervisory Function | WDOG_ON | 1 |

*__NOTE:__ The address inputs are A[19:4] in 80C51XA mode. A[3:0] are assigned to Port A.

**PLDs**
*(cont.)*

*Figure 4.  DPLD Logic Array*



*NOTE: The address inputs are A[19:4] in 80C51XA mode, A[3:0] are assigned to Port A.

**PLDs**
*(cont.)*

### External Chip Select PLD

The External Chip Select PLD (ECSPLD) provides the means to select external devices. The output buffer of the ECSPLD can be configured to operate in high slew rate by writing a "1" to the corresponding bit in the Drive Register. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower response. Refer to Table 26 in the I/O Section for setting up the Drive Register.

Faster transitions are more likely to cause line reflections and system noise than slower rates. Adjusting the slew rate allows a trade-off between greater speed and noise sensitivity. The selection should be based on the performance requirements of the system and its noise characteristics. Set the corresponding bits in the Drive Register to "0" (for normal speed) or "1" (for fast drive). The default value is zero.

The ECSPLD has 24 inputs as shown in Table 9. Its outputs are combinatorial, of either polarity, and have one product term each as shown in Figure 5.

**Table 9.  ECSPLD Inputs**

| Input Source | Input Name | Number of Bits |
|---|---|---|
| MCU Address Bus | A[15:0]* | 16 |
| MCU Control Signals | CNTL[2:0] | 3 |
| Power Down Signal | PDN** | 1 |
| Page Register | PGR[3:0] | 4 |

*In 80C51XA mode, the address inputs are A[19:4]
**APD output. When PDN is high, the PSD7XX is in power down mode

The seven ECSPLD outputs may be driven off the device through Ports A, B, or D, as shown in Table 10, via the Micro⇔Cell Allocator.  Port selection is specified in the PSDabel file or assigned by the PSDcompiler.
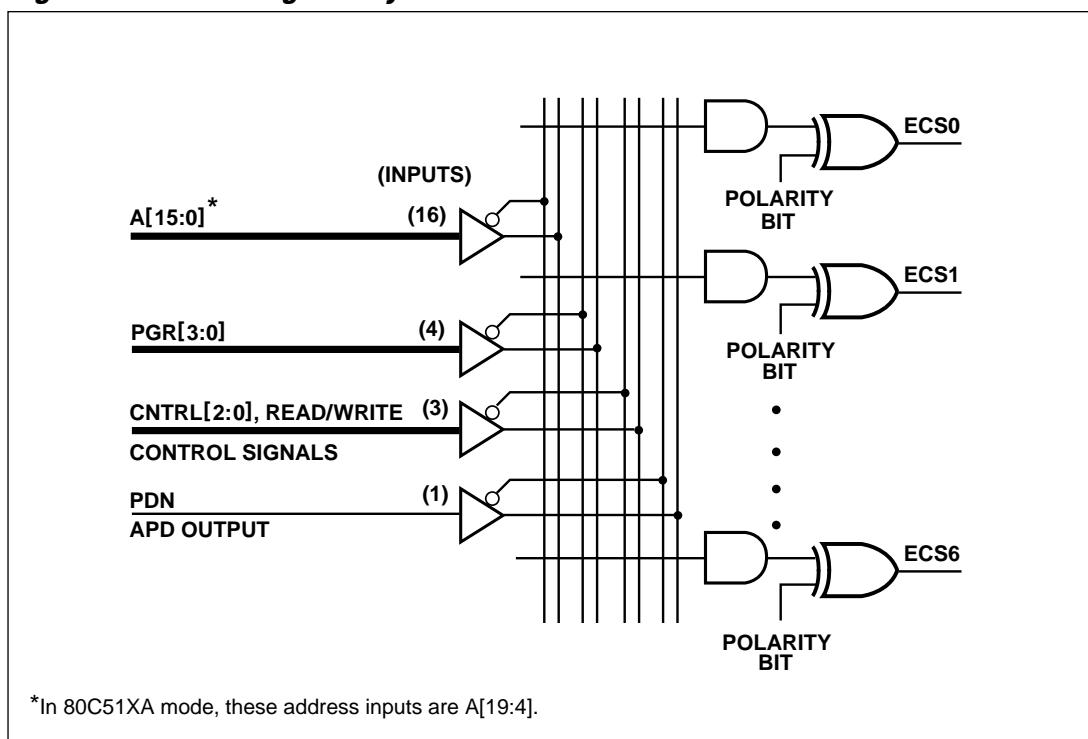
**Table 10.  ECSPLD Output Port Assignments**

| ECSPLD Output | Port A, B, or D Assignments |
|---|---|
| ECS0 | PA0, PB0 |
| ECS1 | PA1, PB1 |
| ECS2 | PA2, PB2 |
| ECS3 | PA3, PB3 |
| ECS4 | PD0* |
| ECS5 | PD1* |
| ECS6 | PD2* |

*Port D has no output enable (.oe) product terms for ECS4-6 outputs.

## PLDs
*(cont.)*

### Figure 5.  ECSPLD Logic Array



(INPUTS)

A[15:0]*      (16)

PGR[3:0]      (4)

CNTRL[2:0], READ/WRITE   (3)
CONTROL SIGNALS

PDN      (1)
APD OUTPUT

ECS0
ECS1
ECS6
POLARITY BIT

*In 80C51XA mode, these address inputs are A[19:4].

### General PLD

The General PLD (GPLD) is used to implement system logic such as MCU loadable counters, system mailboxes or handshaking protocols. In addition the GPLD can implement random logic and state machine functions.

The GPLD has Output and Input Micro⇔Cells. The GPLD, Output and Input Micro⇔Cells architectures appear in Figure 6 along with the Port. The Micro⇔Cells are configured using the PSDsoft development system. Like the other PLDs, the GPLD has an AND array which can generate up to 110 product terms, a maximum of nine product terms for each of the twelve Micro⇔Cells.

The Input and Output Micro⇔Cells are connected to the PSD7XX internal data bus and can be directly accessed by the microcontroller. This enables the MCU software to load data into the Output Micro⇔Cells or read data from both the Input and Output Micro⇔Cells. This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND logic array as required in most standard PLD macrocell architectures.

**PLDs**
*(cont.)*

**Figure 6. The GPLD and I/O Port**
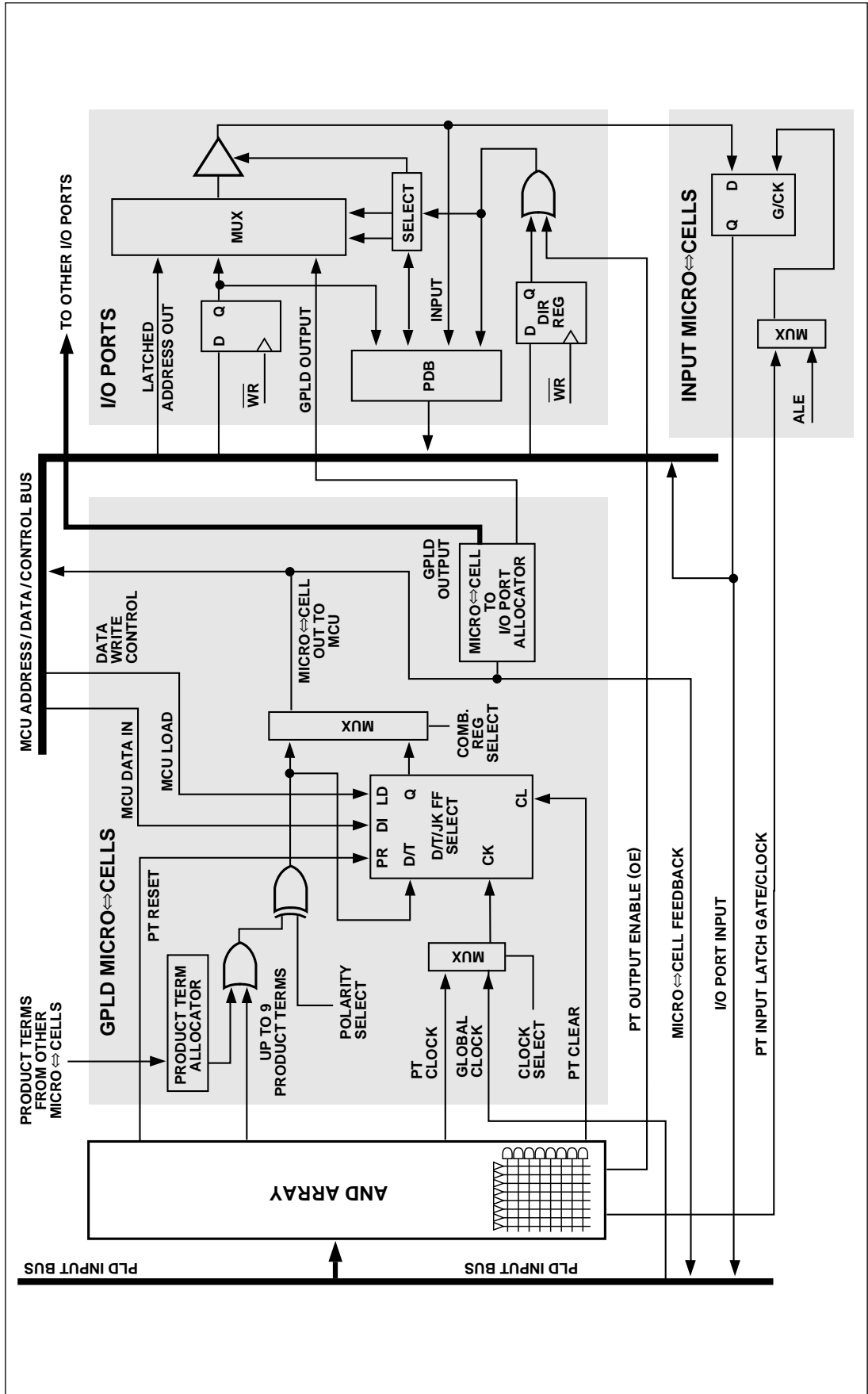
## PLDs
*(cont.)*

### Output Micro⇔Cell

Eight of the Output Micro⇔Cells are connected to Port C pins and are named as McellC0-7. The remaining four Micro-Cells can be connected to Port A or Port B and are named as McellAB4-7. If an McellAB output is not assigned to a specific pin in PSDabel, the Micro⇔Cell Allocator will assign it to either Port A or B. Table 11 shows the Micro⇔Cells and Port assignment.

**Table 11.  Output Micro⇔Cell Port and Data Bit Assignments**

| Output Micro⇔Cell | Port Assignment | Native Product Terms | Max Borrowed Product Terms | Data Bit for Loading or Reading in 8-Bit Mode | Data Bit for Loading or Reading in 16-Bit Mode |
|---|---|---|---|---|---|
| McellC0 | Port C0 | 4 | 5 | D0 | D8 |
| McellC1 | Port C1 | 4 | 5 | D1 | D9 |
| McellC2 | Port C2 | 4 | 5 | D2 | D10 |
| McellC3 | Port C3 | 4 | 5 | D3 | D11 |
| McellC4 | Port C4 | 4 | 5 | D4 | D12 |
| McellC5 | Port C5 | 4 | 5 | D5 | D13 |
| McellC6 | Port C6 | 4 | 5 | D6 | D14 |
| McellC7 | Port C7 | 4 | 5 | D7 | D15 |
| McellAB4 | Port A4, B4 | 3 | 6 | D4 | D4 |
| McellAB5 | Port A5, B5 | 3 | 6 | D5 | D5 |
| McellAB6 | Port A6, B6 | 3 | 6 | D6 | D6 |
| McellAB7 | Port A7, B7 | 3 | 6 | D7 | D7 |

### The Product Term Allocator

All Micro⇔Cells have the same basic cell architecture except McellC has four native product terms and McellAB has three product terms. The GPLD also has a Product Term Allocator with which the PSDcompiler can automatically borrow product terms from one Micro⇔Cell to another. The McellC may borrow up to five product terms from other Micro⇔Cells for a total of nine product terms. The McellAB has three native product terms and can borrow up to six product terms. Borrowing allows Micro⇔Cell outputs needing more product terms to use the unused product terms of others.

The architecture of the 12 Output Micro⇔Cells, as shown in Figure 7, consists of native product terms and borrowed product terms from other Micro⇔Cells. The polarity of the product term input is controlled by the XOR gate. The Micro⇔Cell can implement either sequential logic, using the Flip-Flop element, or combinatorial functions. The multiplexor selects the combinatorial or the sequential logic as the Micro⇔Cell output. The multiplexor output can drive a Port pin and has also a feedback path to the AND array inputs.

### Micro⇔Cell Flip-Flop Type

The Flip-Flop in the Micro⇔Cell can be configured as a D, Toggle, JK or SR type by using PSDabel in PSDsoft. The flip-flop Clock, Preset and Clear inputs are driven from a product term of the AND array. Alternatively, the device clock input (CLKIN) can be used for the flip-flop. The Preset and Clear are active high inputs; the Flip-Flop is clocked by the rising edge of the clock input.

**PLDs**
*(cont.)*

**Figure 7.  GPLD Output Micro⇔Cell**



NOTES: 1. MCELL C has 4 local product terms.
MCELL AB has 3 local product terms.
Max. total product terms : 9
2. Allocator is for MCELL AB only.

**PLDs**
*(cont.)*

## Loading and Reading the Micro⇔Cells

The GPLD Micro⇔Cells occupy a memory location in the MCU address space as defined by the CSIOP (refer to the I/O section). The Flip-Flops in each of the 12 Micro⇔Cells can be loaded from the data bus by a microcontroller write bus cycle to the Micro⇔Cell (see I/O Port section for Micro⇔Cell Addresses). A "1" in the data bit that associates with the Micro⇔Cell will load a "1" to the Flip-Flop, a "0" in the data bit will load a "0" to the Flip-Flop. The loading bus cycle takes priority over other Flip-Flop inputs that include the Preset, Clear and clock. See Table 12 for the data bits that are connected to the Micro⇔Cells. The ability to load the flip-flops and read them back is useful in such applications as loadable counters, shift registers, mailboxes or handshaking protocols.

### Table 12.  Micro⇔Cell Flip-Flop Loading

| LD | Din | Clk | In | PR | CLR | Q |
|----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | X | X | X | X | 1 |
| 1 | 0 | X | X | X | X | 0 |
| 0 | X | Normal Flip-Flop Function | | | | |

**NOTE:** LD is "1" when the MCU writes to the Micro⇔Cell address

### The Output Enable

The Micro⇔Cell can be connected to a PSD7XX I/O pin as PLD output. The output enable of each of the Port pin output driver is controlled by a single product term (.oe) from the AND array ORed with the Direction Register output. Upon power up, if no output enable (.oe) equation is defined and the pin is declared as a PLD output in PSDsoft, the pin is enabled.

If the Micro⇔Cell output is declared as internal node and not as Port pin output in the PSDabel file, then the Port pin can be used for other I/O functions. The internal node feedback can be routed as an input to the AND array.

### Input Micro⇔Cell

The Input Micro⇔Cells as shown in Figure 8 are used to latch, register or pass incoming Port signals prior to driving them onto the PLD Input bus. The outputs of these Micro⇔Cells can also be read by the microcontroller through the internal Data Bus. The GPLD has 24 Input Micro⇔Cells, one for each pin of Ports A, B and C. The Input Micro⇔Cells are individually configurable.

The enable/clock for the latch and flip-flop is driven by a multiplexor whose inputs are a product term from the GPLD AND array and the MCU address strobe (ALE). Each product term output is used to latch/clock four Input Micro⇔Cells. Port inputs [3:0] can be controlled by one product term and [7:4] can be controlled by another one.

The Input Micro⇔Cell configurations are specified by equations written in PSDabel. Outputs of the Micro⇔Cells can be read by the microcontroller via the "Input Micro⇔Cell" buffer. See the I/O Port section on how to read the Micro⇔Cells.
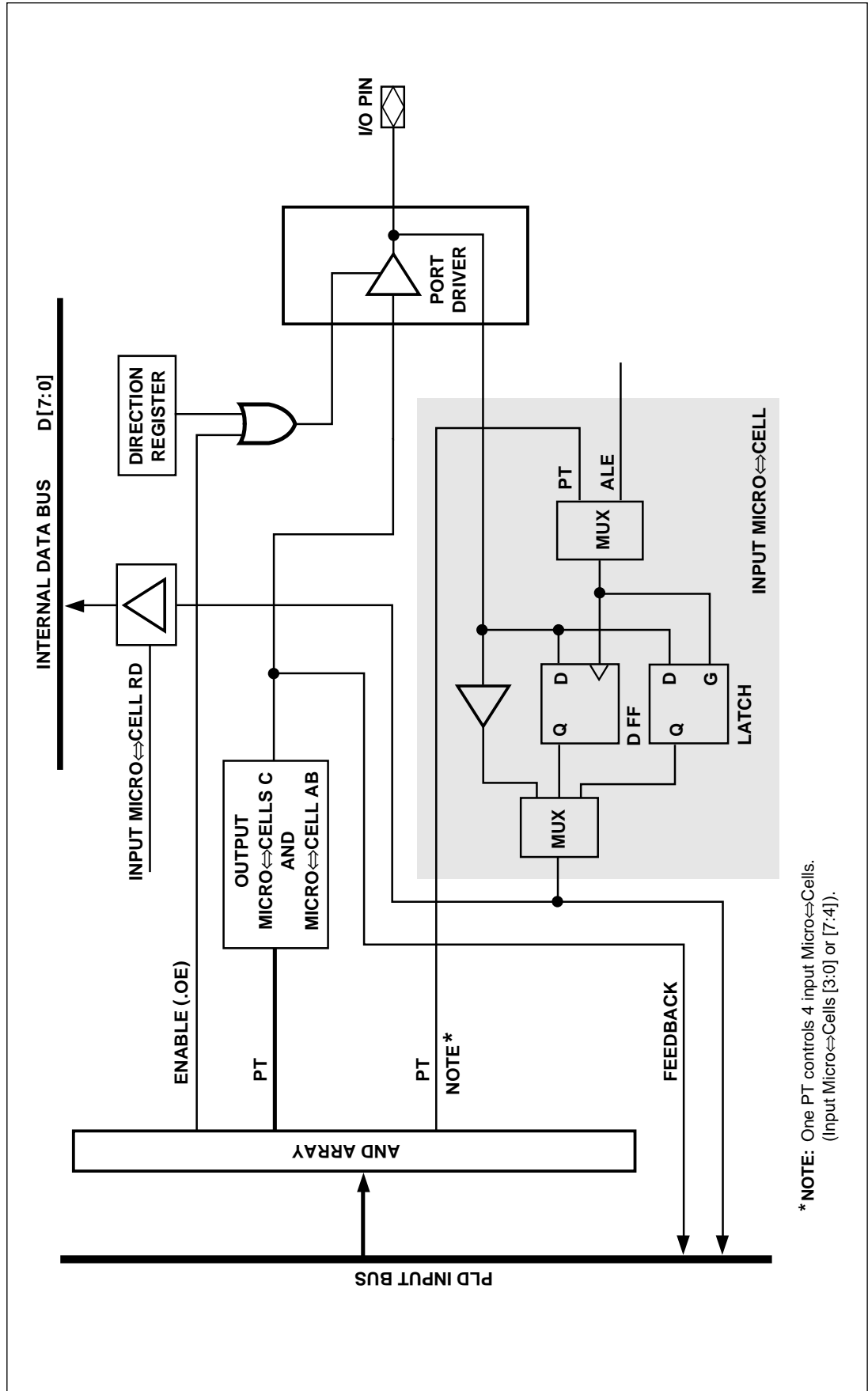
Input Micro⇔Cells can use the ALE to latch the higher address bits (A31 – A16). The latched addresses are routed to the PLD as inputs.

The Input Micro-Cell is particularly useful in handshaking communication applications where two MCUs wish to pass data between each other through a commonly accessible storage. Figure 9 shows a typical configuration where the Master MCU writes to the Port A Data Out Register that is read by the Slave MCU via the activation of the "Slave-Read" output enable product term. The Slave MCU can write to Port A Input Micro⇔Cells by activating the Slave-WR product term. The Master MCU can then read the Input Micro⇔Cells. The Slave-Read and Slave-WR signals are product terms that are derived from the Slave MCU signals RD, WR, and Slave_CS.

**PLDs**
*(cont.)*

*Figure 8.  Input Micro⇔Cell*



**INPUT MICRO⇔CELL**

**DIRECTION REGISTER**

**PORT DRIVER**

I/O PIN

**INTERNAL DATA BUS**  D[7:0]

INPUT MICRO⇔CELL RD

MUX

PT  ALE

D FF

LATCH

D  Q

D  G  Q

MUX

ENABLE (.OE)

PT

PT

NOTE*

FEEDBACK

**OUTPUT MICRO⇔CELLS C AND MICRO⇔CELL AB**
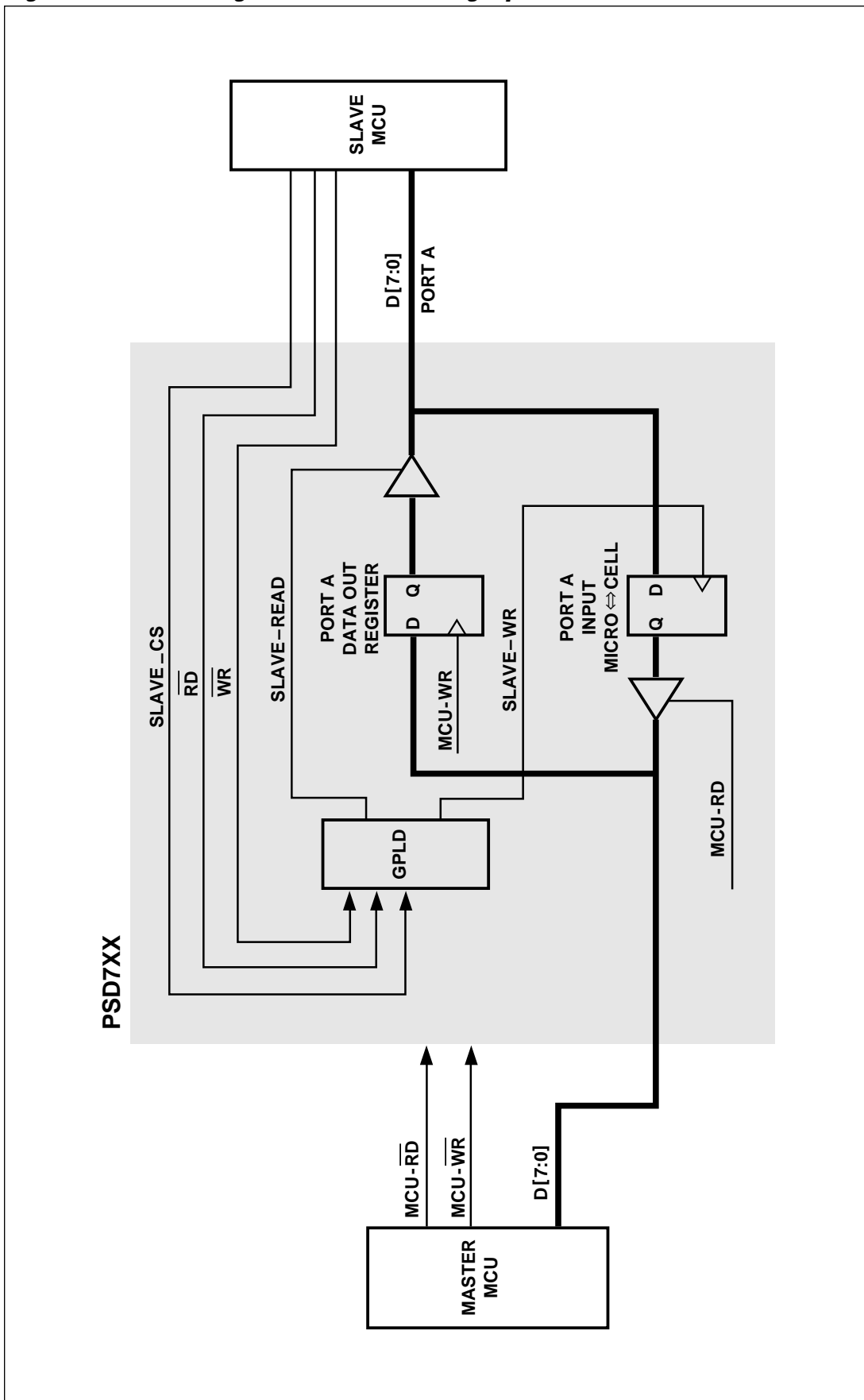
**AND ARRAY**

**PLD INPUT BUS**

**\*NOTE:** One PT controls 4 input Micro⇔Cells.
(Input Micro⇔Cells [3:0] or [7:4]).

*PLDs*
*(cont.)*

*Figure 9.  Handshaking Communication Using Input Micro⇔Cells*

## PLDs
*(cont.)*

### Peripheral PLD

The Peripheral PLD (PPLD), shown in Figure 10, controls the operation of the WatchDog Timer of the Supervisory Function. The input to the PPLD consists of the same 66 signals that are shared with the GPLD (refer to Table 7). The PPLD provides two active high outputs, each consists of one product term:

❏ **WDOG_EN**

The WatchDog Timer can be enabled either by the trailing edge of the reset generated by the Supervisory Function, or by an active high WDOG_EN pulse. The WDOG_EN product term can be defined to become active when the microcontroller writes to a certain address. The WDOG_EN signal can be activated only after the external reset (ERESET) expires.

❏ **WDOG_CLR**

This is an active high pulse that re-loads the counter in the WatchDog Timer and prevents the WatchDog from generating a timeout. The WDOG_CLR product term can be defined to become active when the microcontroller writes to a specific address.

### Figure 10. PPLD Logic Array
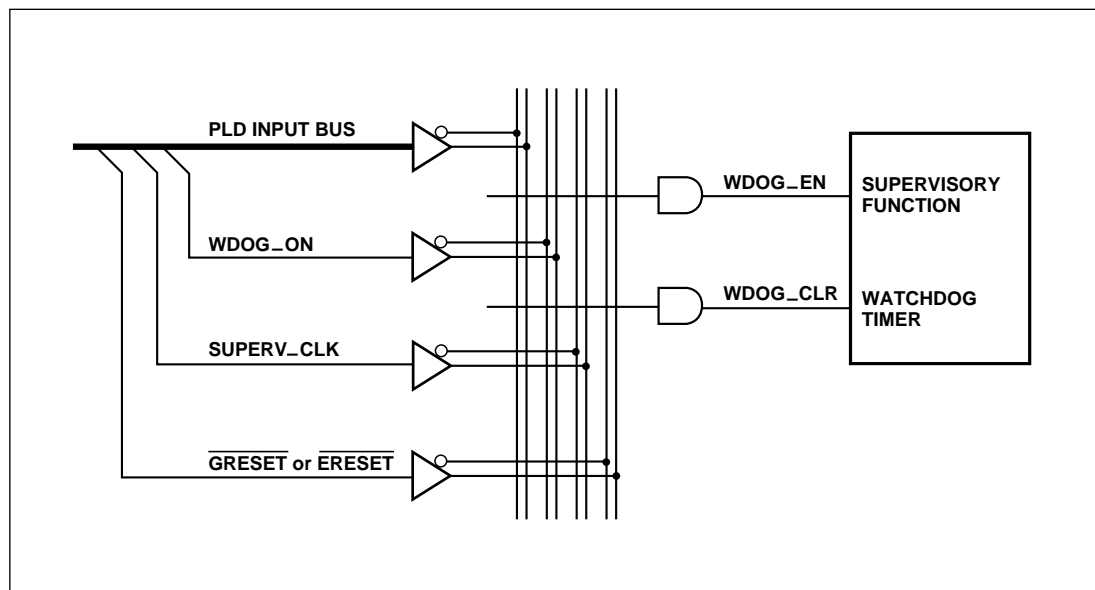
## *Bus Interface*

The "no-glue logic" PSD7XX Microcontroller Bus Interface can be directly connected to the most popular microcontrollers. Some of these microcontrollers with their bus types and control signals are shown in Table 13. The interface type is specified using the PSDsoft tools.

### *Table 13. Microcontroller Busses and Control Signals*

| *MCU* | *Data Bus* | *CNTL0* | *CNTL1* | *CNTL2* | *PC7* | *PD0\*\** | *ADIO0* | *PA3–PA0* |
|---|---|---|---|---|---|---|---|---|
| 8031 | 8 | $\overline{WR}$ | $\overline{RD}$ | $\overline{PSEN}$ | * | ALE | A0 | * |
| 68330 | 8 | R/W | $\overline{DS}$ | * | * | ALE | A0 | * |
| 80198 | 8 | $\overline{WR}$ | $\overline{RD}$ | * | * | ALE | A0 | * |
| 68HC11 | 8 | R/W | E | * | * | AS | A0 | * |
| 80C51XA | 8 | $\overline{WR}$ | $\overline{RD}$ | $\overline{PSEN}$ | * | ALE | A4 | A3 – A0 |
| 80C251 | 8 | $\overline{WR}$ | $\overline{PSEN}$ | * | * | ALE | A0 | * |
| 80C251 | 8 | $\overline{WR}$ | $\overline{RD}$ | $\overline{PSEN}$ | * | ALE | A0 | * |
| Z8 | 8 | R/$\overline{W}$ | $\overline{DS}$ | * | * | * | A0 | * |
| Neuron 3150 | 8 | R/$\overline{W}$ | $\overline{DS}$ | * | * | * | A0 | * |
| 80196 | 16 | $\overline{WRL}$ | $\overline{RD}$ | $\overline{BHE}$ | * | ALE | A0 | * |
| 80196 | 16 | $\overline{WRL}$ | $\overline{RD}$ | * | $\overline{WRH}$ | ALE | A0 | * |
| 68HC12\*\*\* | 16 | R/$\overline{W}$ | E | A0 | * | – | $\overline{LSTRB}$ | * |
| 68302 | 16 | R/$\overline{W}$ | $\overline{LDS}$ | $\overline{UDS}$ | * | AS | – | * |
| 68330 | 16 | R/$\overline{W}$ | $\overline{DS}$ | $\overline{BHE}$ | * | AS | A0/BLE | * |
| 68332 | 16 | R/$\overline{W}$ | $\overline{DS}$ | SIZ0 | * | AS | A0 | * |
| 80C51XA | 16 | $\overline{WRL}$ | $\overline{RD}$ | $\overline{PSEN}$ | $\overline{WRH}$ | ALE | A4/D0 | A3 – A1 |
| 68LC302 | 16 | $\overline{WEL}$ | $\overline{OE}$ | | $\overline{WEH}$ | AS | – | * |
| 80186 | 16 | $\overline{WR}$ | $\overline{RD}$ | $\overline{BHE}$ | * | ALE | A0 | * |
| 80C166 | 16 | $\overline{WR}$ | $\overline{RD}$ | $\overline{BHE}$ | * | ALE | A0 | * |

 \*Not used CNTL2 pin can be configured as GPLD input. Other not used pins (PC7, PD0, PA3-0) can be configured for other I/O functions.

  \*\*ALE/AS input is optional for microcontrollers with a non-multiplexed bus.

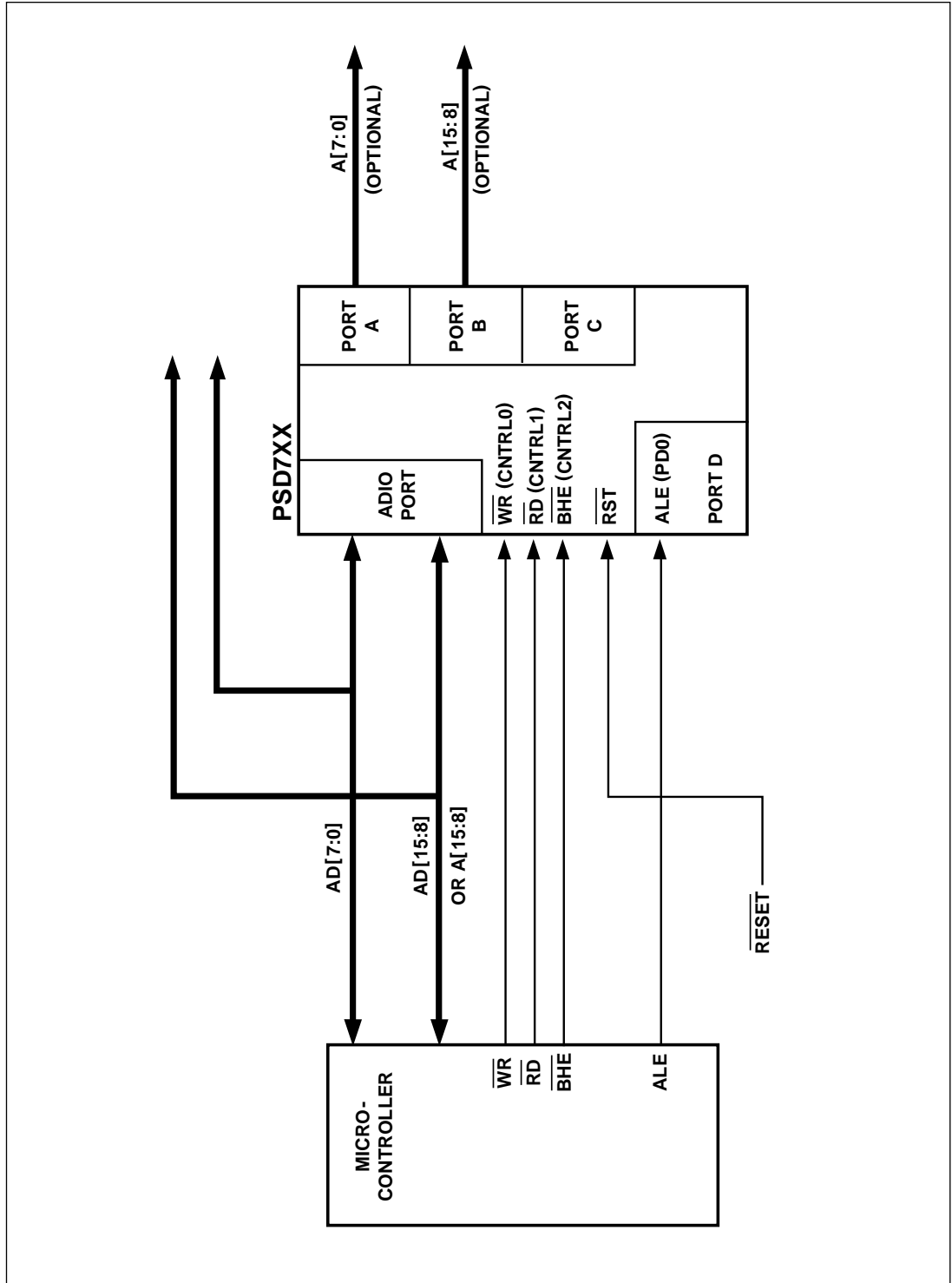\*\*\*This configuration is for 68HC12 with non-mux bus.

Table 13 shows the names of the PSD7XX bus interface control pins and their functions. The control pins have multiple functions and can be configured to interface to many microcontrollers. Depending on the microcontroller, some of the control input pins are not required and may be used as GPLD input or other I/O functions. Specific examples of interfaces to different microcontrollers are provided in the following sections. For microcontrollers that have more than 16 address lines, Port A, B, or C pins may be used as additional address inputs

**Bus Interface**

*(cont.)*

### PSD7XX Interface To a Multiplexed Bus

Figure 11 shows an example of a system using a microcontroller with a multiplexed bus and a PSD7XX. The ADIO port on the PSD7XX is connected directly to the microcontroller address/data bus. The bus may be multiplexed only on one byte (eight-bit data) or on both bytes (sixteen-bit data). The ALE latches the address lines internally; latched addresses can be brought out to Port A or B. The PSD7XX drives the ADIO data bus only when one of its internal resources is accessed and the $\overline{\text{RD}}$ input is active.

***Figure 11. An Example of a Typical Multiplexed Bus Interface, 8 or 16-Bit Data Bus***

## Bus Interface
*(cont.)*

### PSD7XX Interface To a Non-Multiplexed Bus

Figure 12 shows an example of a system using a microcontroller with a non-multiplexed bus and a PSD7XX. The address bus is connected to the ADIO Port, and the data bus is connected to Port A (D[7:0]) and to Ports B (D[15:8], 16-bit data bus only). The data Ports are in tri-state mode when the PSD7XX is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Port A, B, or C may be used as additional address inputs.

*Figure 12.  An Example of a Typical Non-Multiplexed Bus Interface,*
*8 or 16-Bit Data Bus*

## Bus Interface
*(cont.)*

### Data Byte Enable Reference

Microcontrollers have different data byte orientations. The following tables show how the PSD7XX interprets byte/word operation in different write bus configurations. Even-byte refers to locations with address A0 equal to zero and odd byte as locations with A0 equal to one.

*Table 14.  8-Bit Data Bus*

| BHE | A0 | D7 – D0 |
|-----|-----|-----------|
| X | 0 | Even Byte |
| X | 1 | Odd Byte |

*Table 15.  16-Bit Data Bus With $\overline{BHE}$*

| BHE | A0 | D15 – D8 | D7 – D0 |
|-----|-----|-----------|-----------|
| 0 | 0 | Odd Byte | Even Byte |
| 0 | 1 | Odd Byte | – |
| 1 | 0 | – | Even Byte |

*Table 16.  16-Bit Data Bus With $\overline{WRH}$ and $\overline{WRL}$*

| WRH | WRL | D15 – D8 | D7 – D0 |
|-----|-----|-----------|-----------|
| 0 | 0 | Odd Byte | Even Byte |
| 0 | 1 | Odd Byte | – |
| 1 | 0 | – | Even Byte |

*Table 17.  16-Bit Data Bus With SIZ0, A0 (Motorola MCU)*

| SIZ0 | A0 | D15 – D8 | D7 – D0 |
|------|-----|-----------|-----------|
| 0 | 0 | Even Byte | Odd Byte |
| 1 | 0 | Even Byte | – |
| 1 | 1 | – | Odd Byte |

*Table 18.  16-Bit Data Bus With $\overline{UDS}$, $\overline{LDS}$ (Motorola MCU)*

| LDS | UDS | D15 – D8 | D7 – D0 |
|-----|-----|-----------|-----------|
| 0 | 0 | Even Byte | Odd Byte |
| 1 | 0 | Even Byte | – |
| 0 | 1 | – | Odd Byte |

## Bus Interface
*(cont.)*

## *Microcontroller Interface Examples*

Figures 13 through 20 show examples of the basic connections between the PSD7XX and some popular microcontrollers. The PSD7XX control input pins are labeled as the microcontroller function for which they are configured. The MCU interface is specified using the PSDsoft tools.

### *80C31*

Figure 13 shows the interface to the 80C31 which has an 8-bit multiplexed address/data bus. The lower address byte is multiplexed with the data bus. The microcontroller RD and WR signals may be used for accessing internal SRAM and I/O Ports while the PSEN signal is used to read the EPROM. The ALE input (Port D PD0) latches the address. Refer to the Memory Section for additional 80C31 operating modes.

### *68HC11*

Figure 14 shows an interface to an 68HC11 where the PSD7XX is configured in 8-bit multiplexed mode with E and R/W settings. The ECSPLD can generate the READ and WR signals for external on board devices. The CNTL2 pin is not used and can be used as a PLD input.

### *80C196*

In Figure 15, the Intel 80C196 microcontroller, which has a multiplexed sixteen-bit bus, is shown connected to a PSD7XX. The $\overline{BHE}$ signal is used for high data byte selection. Port pins can be configured in the PSDabel as PLD outputs to control the READY and BUSWIDTH pins of the 80C196.

### *MC68331*

Figure 16 shows a Motorola MC68331 with non-multiplexed sixteen-bit data bus and 24-bit address bus. The data bus from the MC68331 is connected to Port A (D0−7) and Port B (D8−15). The SIZ0 and A0 inputs determine the high/low byte selection.

### *80C51XA*

The Philips 80C51XA microcontroller family has an 8 or 16 bit multiplexed bus that supports burst cycles. Address bits A[3:0] are not multiplexed while A[19:4] are multiplexed with data bits D[15:0] in 16-bit mode. In 8-bit mode, A[11:4] are multiplexed with data bits D[7:0].

The 80C51XA can be configured to operate with a PSD7XX in 8-bit (shown in Figure 17) or 16-bit (shown in Figure 18) data mode. With a 16-bit data bus, the 80C51XA's $\overline{WRH}$ pin is connected to the PC7 pin on the PSD7XX. Pin PA0 is grounded and not used.

The 80C51XA improves bus throughput and performance by executing Burst cycles to fetch codes from memory. In Burst cycles, address A19−4 are latched internally by the PSD7XX, while the 80C51XA changes the A3−0 lines to sequentially fetch up to 16 bytes of code. The PSD access time is then measured from address A3−A0 valid to data in valid. The PSD7XX bus timing requirement in Burst cycle is identical to the normal bus cycle except the address set up or hold time with respect to ALE is not required.

## *Bus Interface*

*(cont.)*

### *80C251*

The Intel 80C251 microcontroller features a user-configurable bus interface with four possible bus configurations as shown in Table 19.

***Table 19.  80C251 Configurations***

| *Configuration* | *80C251 Read/Write Pins* | *Connecting to PSD7XXE1 Pins* | *Page Mode* |
|---|---|---|---|
| 1 | $\overline{WR}$<br>$\overline{RD}$<br>$\overline{PSEN}$ | CNTL0<br>CNTL1<br>CNTL2 | Non-Page Mode, 80C31 compatible<br>A[7:0] multiplex with D[7:0} |
| 2 | $\overline{WR}$<br>$\overline{PSEN}$ only | CNTL0<br>CNTL1 | Non-Page Mode<br>A[7:0] multiplex with D[7:0} |
| 3 | $\overline{WR}$<br>$\overline{PSEN}$ only | CNTL0<br>CNTL1 | Page Mode<br>A[15:8] multiplex with D[7:0} |
| 4 | $\overline{WR}$<br>$\overline{RD}$<br>$\overline{PSEN}$ | CNTL0<br>CNTL1<br>CNTL2 | Page Mode<br>A[15:8] multiplex with D[7:0} |

Configuration 1 is 80C31 compatible. The bus interface to the PSD7XX is identical to that shown in Figure 13. Configurations 2 and 3 have the same bus connection as shown in Figure 19 . There is only one read input ($\overline{PSEN}$) connected to the CNTL1 pin on the PSD7XX. The A16 connection to the PA0 pin allows for a larger address input to the PSD7XX. Configuration 4 is shown in Figure 20. The $\overline{RD}$ signal is connected to CNTL 1 and the PSEN signal is connected to the CNTL2.

The 80C251 has two major operating modes:  Page Mode and Non-Page Mode. In Non-Page Mode, the data is multiplexed with the lower address byte. The ALE is active in every bus cycle. In Page Mode, data D[7:0] is multiplexed with address A[15:8]. In a bus cycle where there is a Page hit, the ALE signal is not active and only addresses A[7:0] are changing. The PSD7XX supports both modes. In Page Mode, the PSD bus timing is identical to Non-Page Mode except the address hold time and setup time with respect to ALE is not required. The PSD7XX access time is measured from address A[7:0] valid to data in valid.

Upon power up the 80C251 accesses data at addresses FFF8h and FFF9h where the bus configuration bytes reside. After the configuration register is set, the 80C251 starts executing codes from location 0000h. The 7th EPROM block in the PSD7XX has two chip selects, ES7A and ES7B. The second chip select, (ES7B) can be defined to occupy the configuration byte locations while ES7A is assigned to a different memory space.

## Bus Interface
*(cont.)*

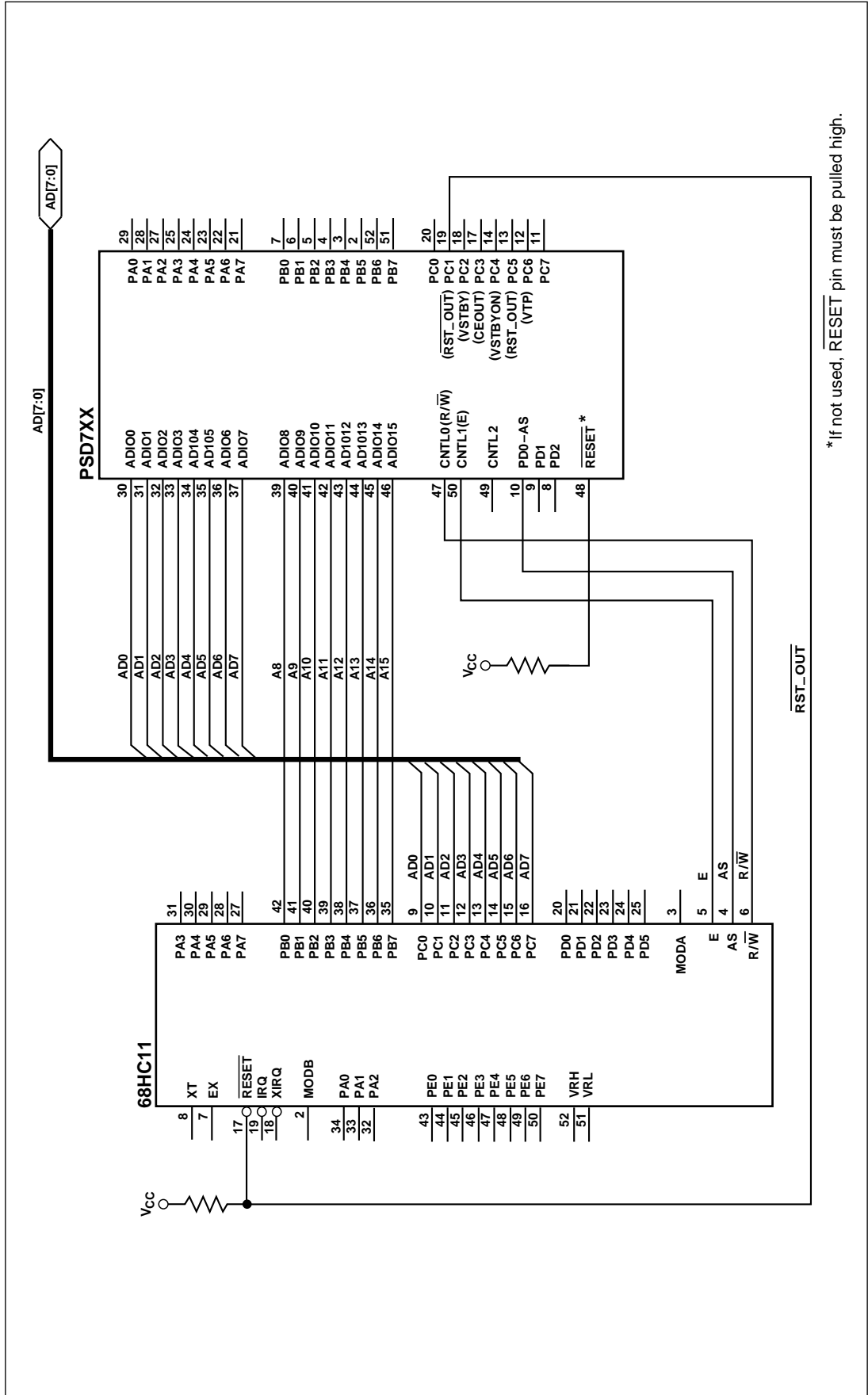### Figure 13. Interfacing the PSD7XX with an 80C31 MCU
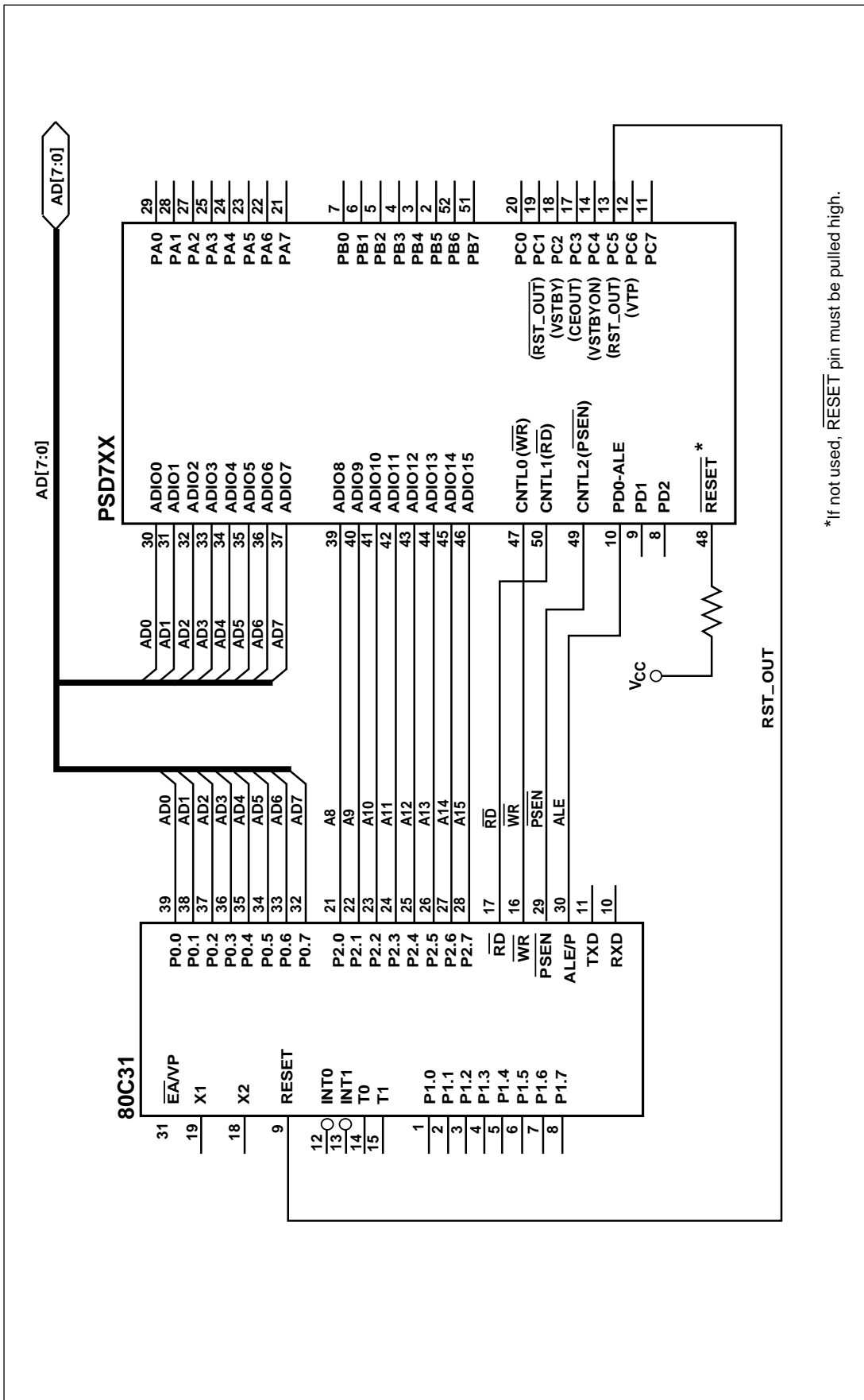
**Bus Interface**
*(cont.)*

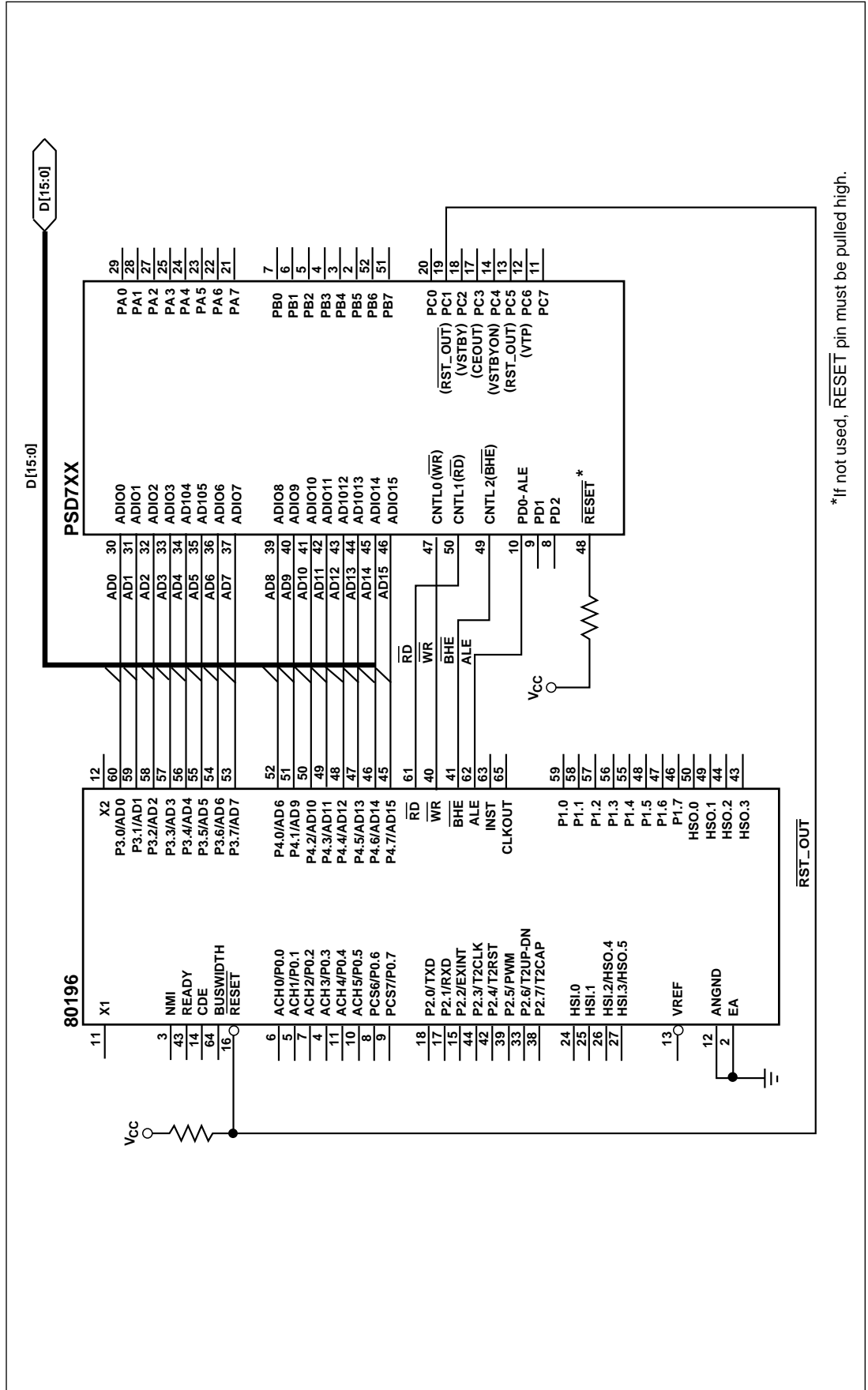*Figure 14.  Interfacing the PSD7XX with a 68HC11*



*If not used, RESET pin must be pulled high.

## Bus Interface
*(cont.)*

### Figure 15.  Interfacing the PSD7XX to an 80C196



*If not used, RESET pin must be pulled high.

**Bus Interface**
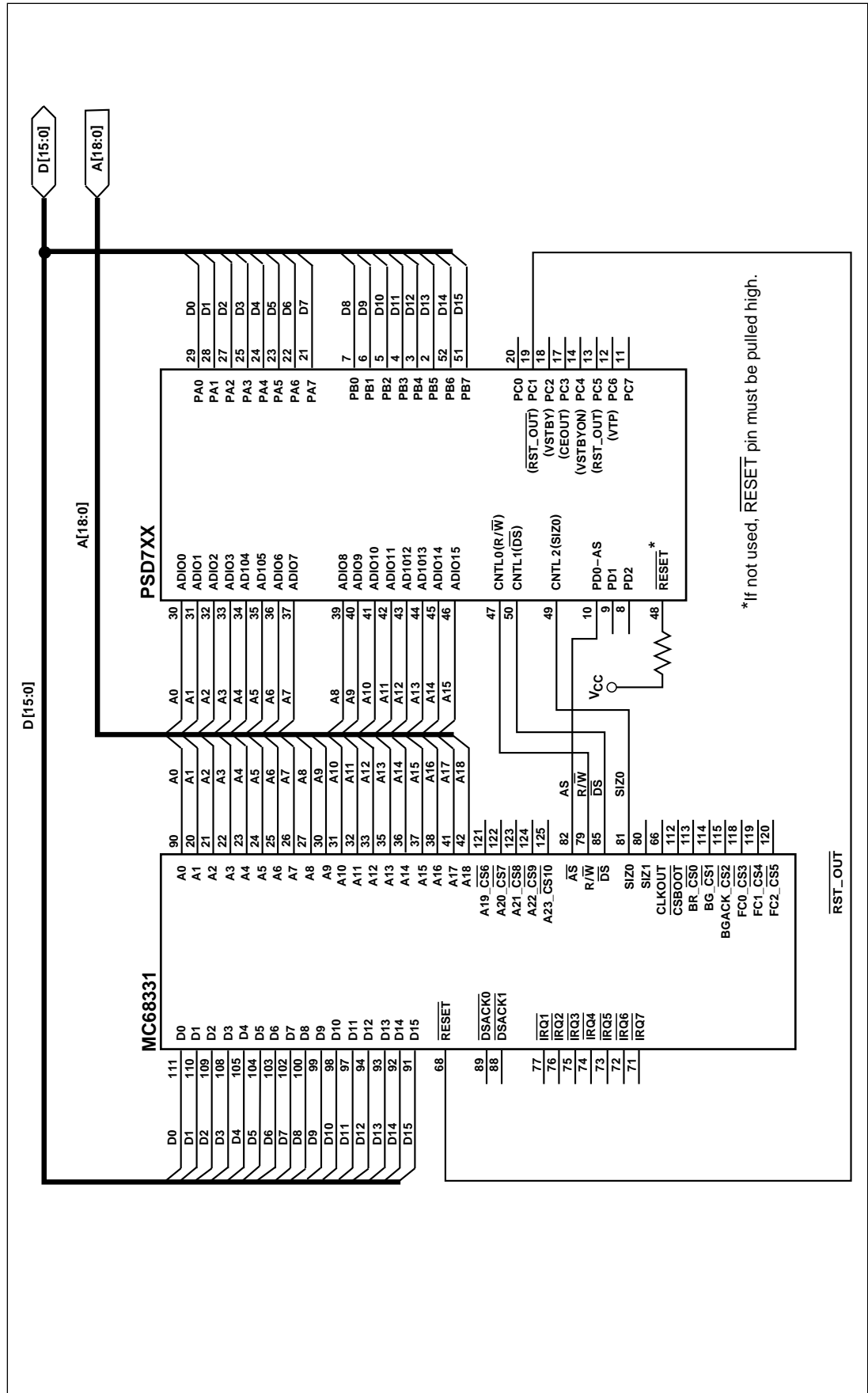*(cont.)*

*Figure 16.  Interfacing the PSD7XX to the MC68331*



*If not used, $\overline{RESET}$ pin must be pulled high.

**Bus Interface**
*(cont.)*

**Figure 17.  Interfacing the PSD7XX to the 80C51XA, 8-Bit Data Bus**
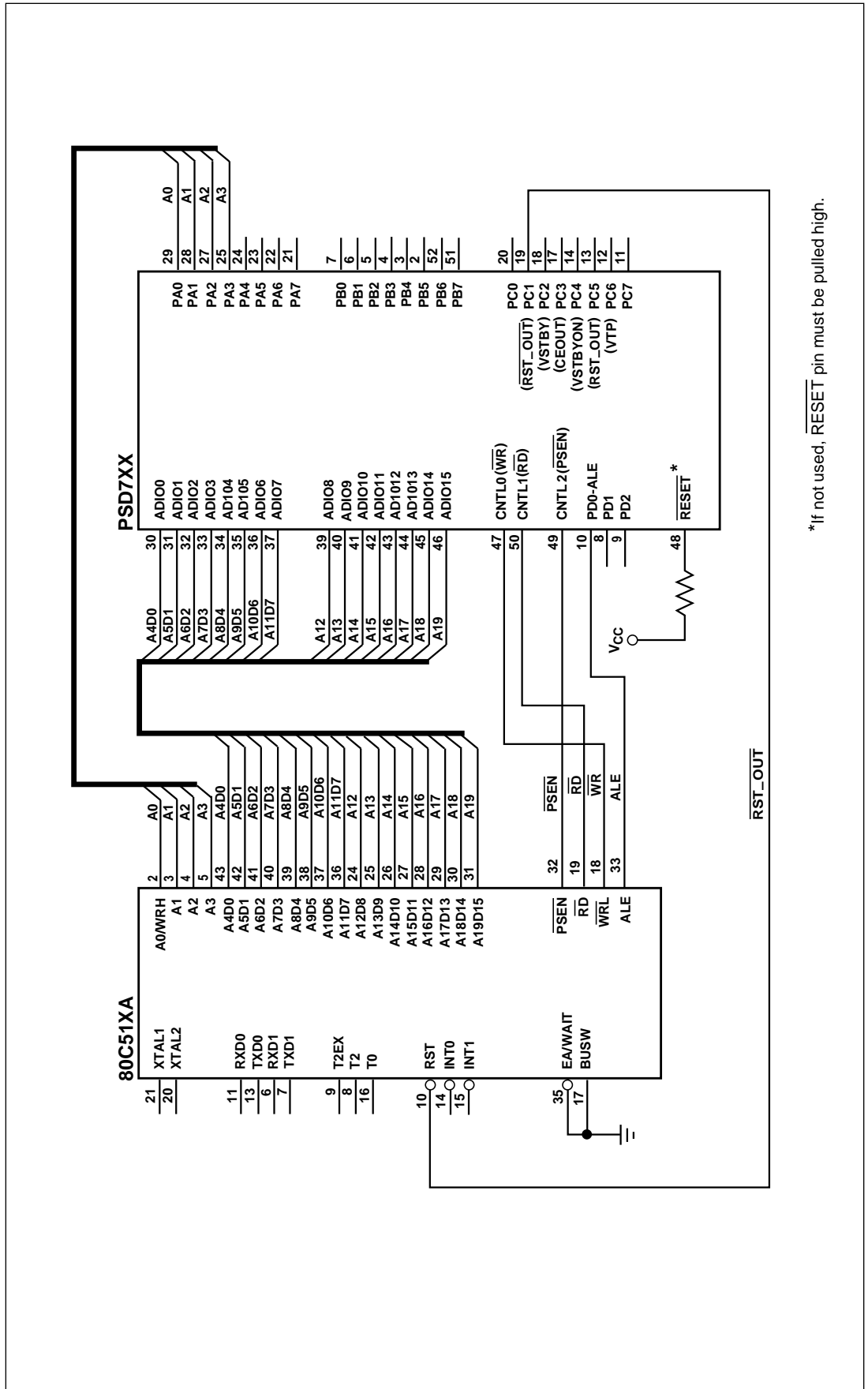
**Bus Interface**
*(cont.)*

***Figure 18. Interfacing the PSD7XX to the 80C51XA, 16-Bit Data Bus***
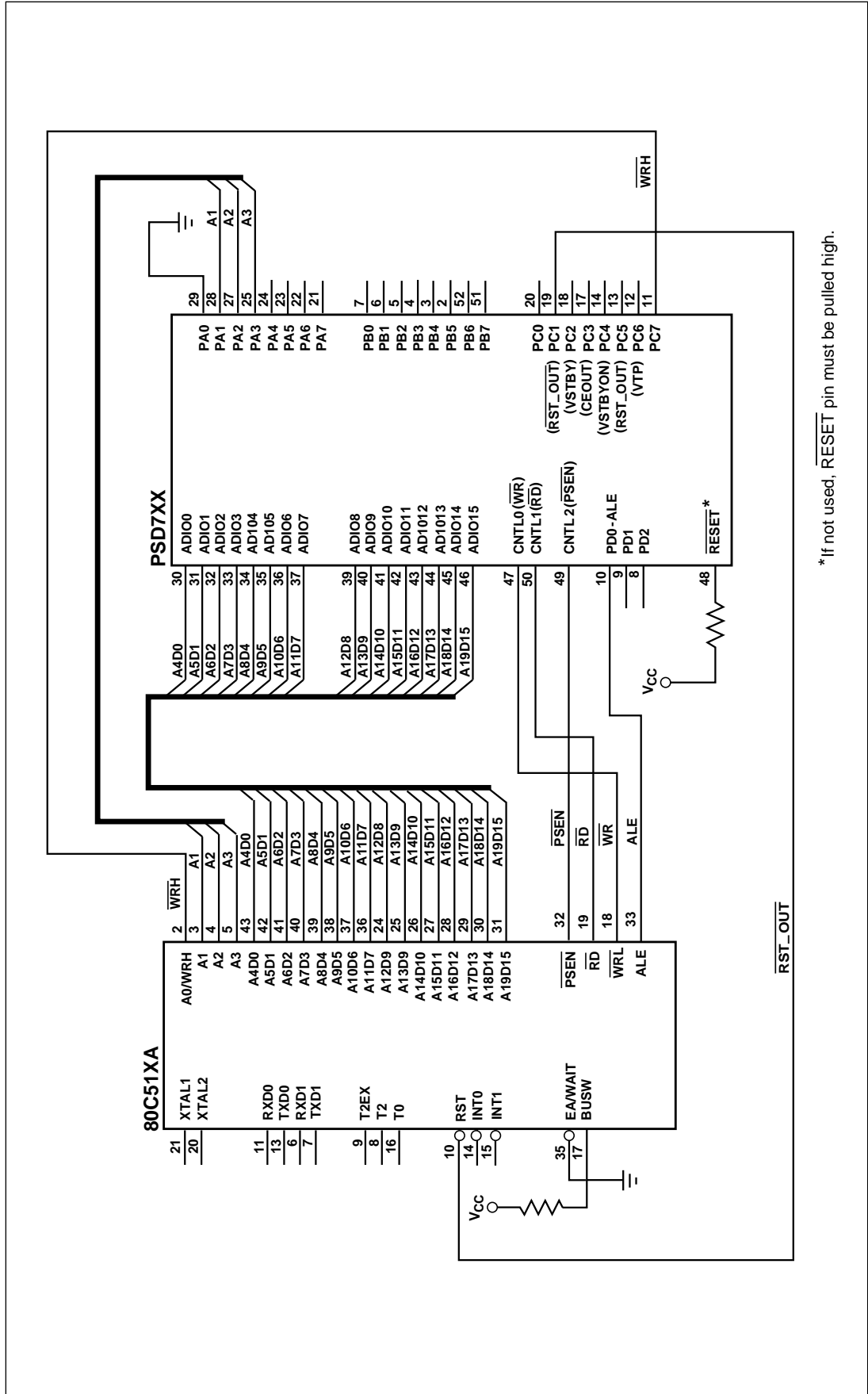
## Bus Interface
*(cont.)*

### Figure 19.  Interfacing the PSD7XX to the 80C251, with One READ Input
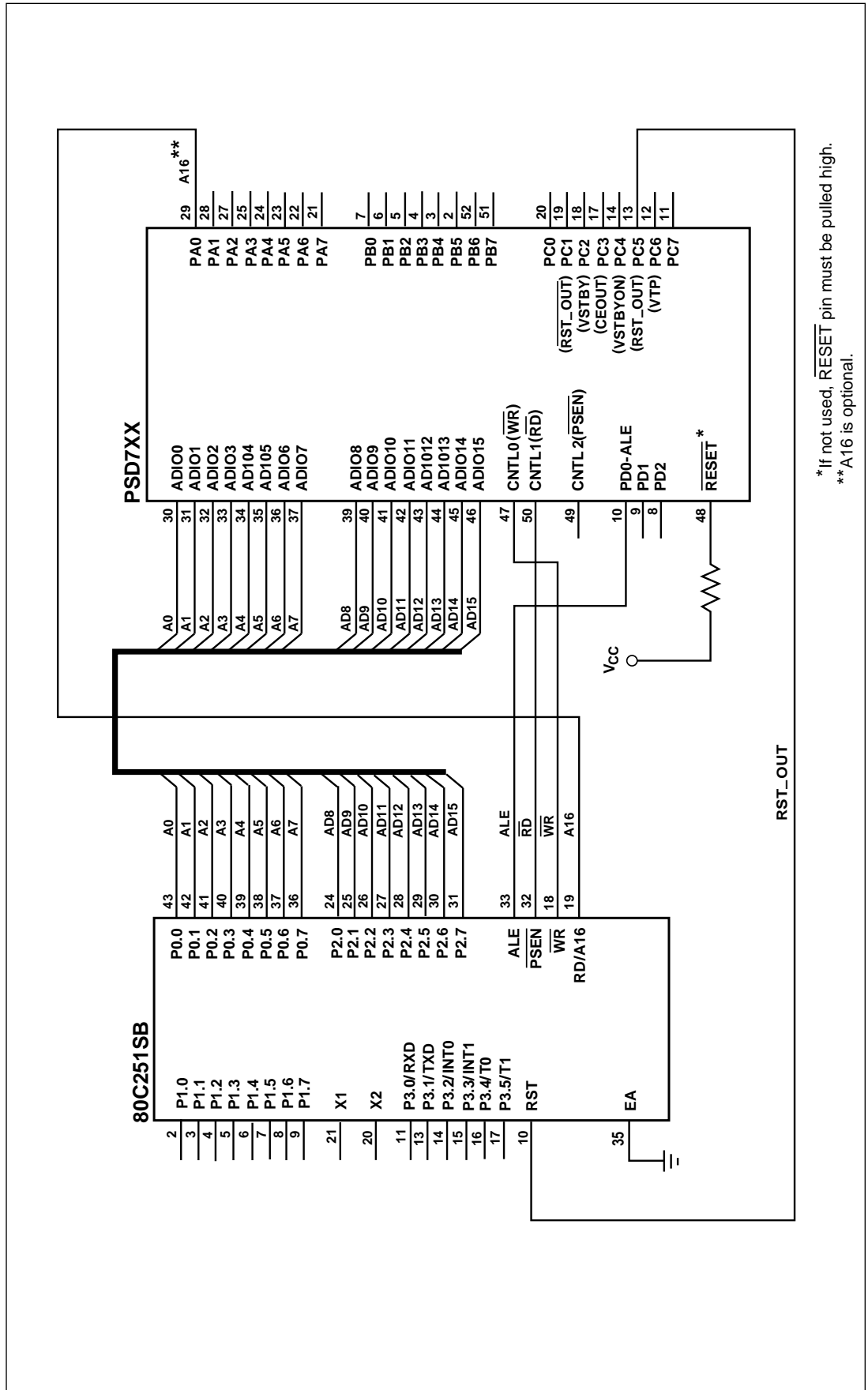
**Bus Interface**
*(cont.)*

***Figure 20.  Interfacing the PSD7XX to the 80C251, with READ and PSEN Input***



*If not used, RESET pin must be pulled high.
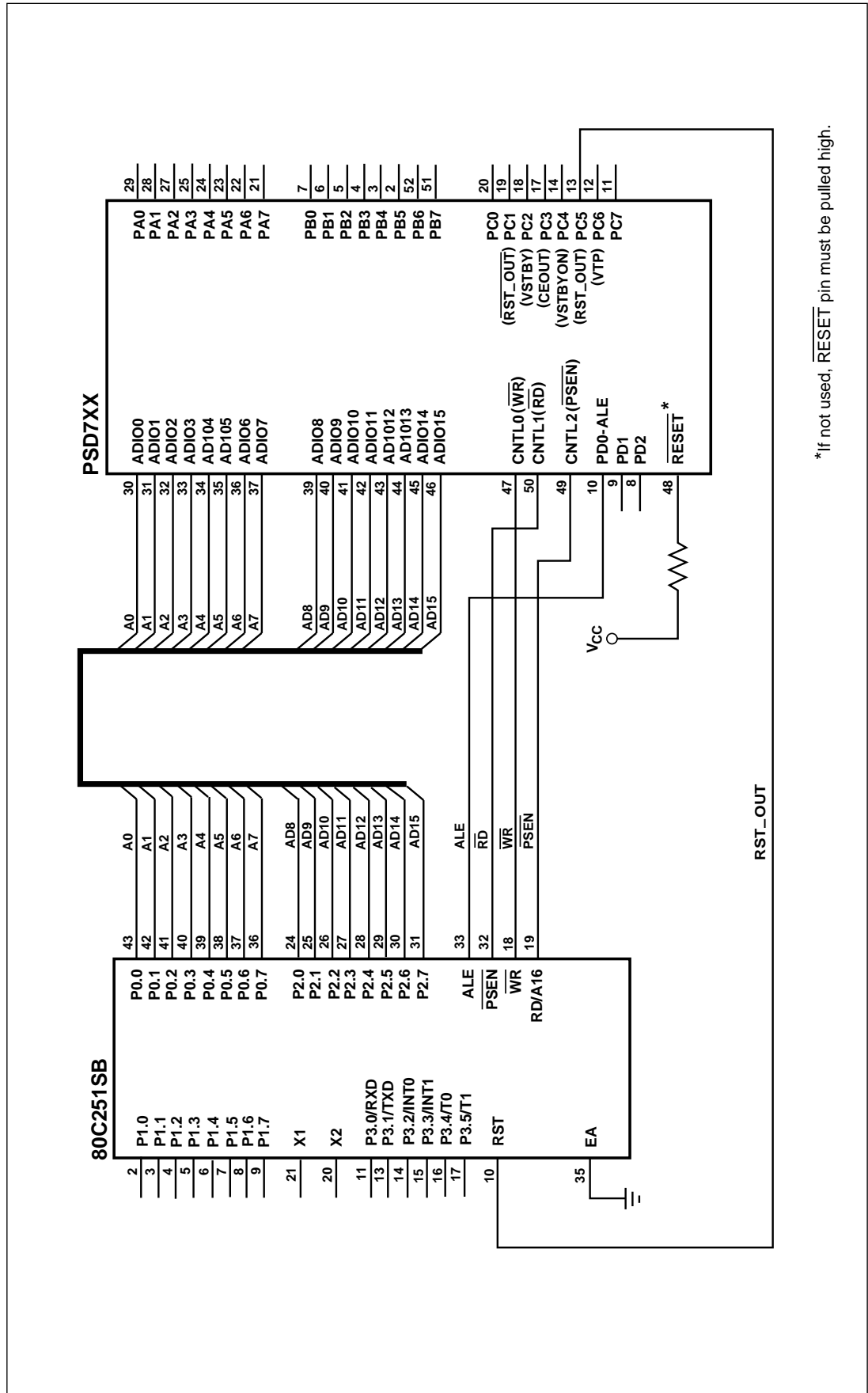
## *I/O Ports*

There are four programmable I/O ports: Ports A, B are 8 bits, Port C is seven bits and Port D is three bits. The ports can be configured to function in different modes of operation.

Each port pin is individually configurable allowing a single port to perform multiple functions. The configuration is defined either using the PSDsoft tools or by the microcontroller writing to the on-chip registers.

### *General Port Architecture*

The general architecture of the I/O Port is shown in Figure 21. Individual Port diagrams are shown in Figures 23, 24 and 25, and will be discussed in the section below. If the PSD7XX is configured to a non-multiplexed bus mode, Port A and/or Port B are connected to the MCU data bus and are not available as general purpose I/O ports.

As shown in Figure 21, the port pins contain an output multiplexer whose selects are driven by the configuration defined in PSDabel and the Control Registers. Inputs to the multiplexer include the following:

❑ Output data from the Data Out Register in the MCU I/O output mode
❑ Latched address outputs
❑ GPLD Micro⇔Cell output or ECSPLD external chip select output

The above inputs are also connected to the Port Data Buffer (PDB) for feedback to the Internal Data Bus that can be read by the microcontroller. The PDB is a three-state buffer operating like a multiplexer that allows only one source to be read at a time. The PDB also has inputs from the Direction Register, Control Register and direct port pin input (Data In).

The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the GPLD AND array Enable product term (.oe) and the Direction Register. If the enable product term of the array output is not defined, then the Direction Register has sole control of the buffer. Refer to Tables 20 and 21 on how the direction of a port pin is configured.

### *Table 20.  Port Pin Direction Control, Output Enable P.T. Not Defined*

| *Direction Register Bit* | *Port Pin Mode* |
|---|---|
| 0 | Input |
| 1 | Output |

### *Table 21.  Port Pin Direction Control, Output Enable P.T. Defined*

| *Direction Register Bit* | *Output Enable P.T.\** | *Port Pin Mode* |
|---|---|---|
| 0 | 0 | Input |
| 0 | 1 | Output |
| 1 | 0 | Output |
| 1 | 1 | Output |

\*Port D does not have an output enable P.T.

The register contents can be altered by the microcontroller.  The PDB feedback path allows the microcontroller to check the contents of the registers.

The A, B and C Ports have embedded Input Micro⇔Cells which can be configured as a latch, a register or direct input to the GPLD. The latch and register are clocked by the address strobe or a product term from the GPLD AND array. The output from the Input Micro⇔Cell drives the PLD input bus and can be read by the microcontroller. Refer to the Input Micro⇔Cell description in the PLD section.

Port A has additional logic (not shown in Figure 21) that enables it to operate in Peripheral I/O mode when the PIO bit in the VM Register is set.

*I/O Ports*
*(cont.)*

**Figure 21.  General I/O Port Architecture**
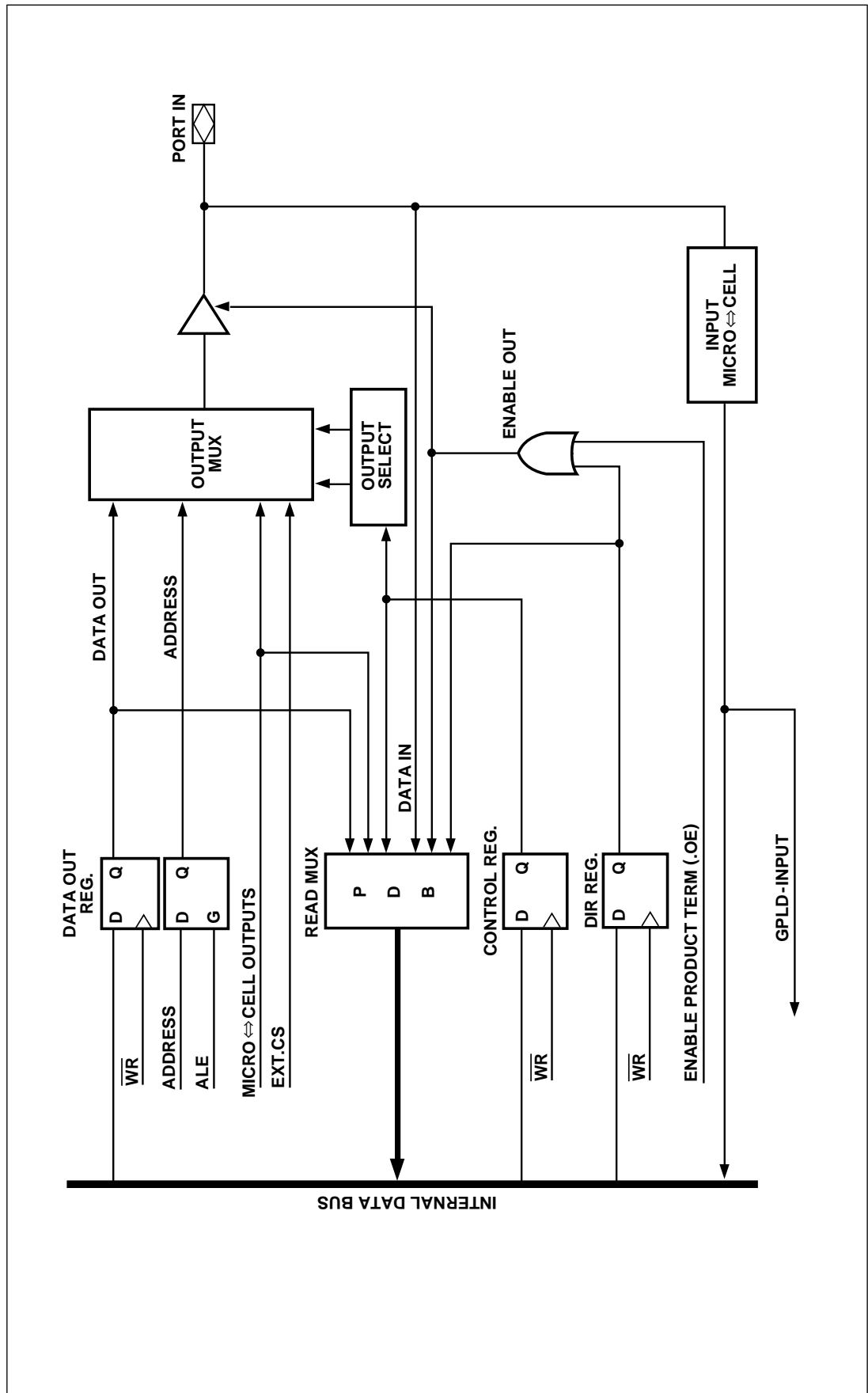
## I/O Ports
*(cont.)*

### Port Operating Modes

The I/O Ports have several modes of operation as shown in Table 22. The mode may be selected using the PSDabel tool and programmed into the device using Non-Volatile Memory (NVM) that is active when power is applied and cannot be altered unless the device is reprogrammed. If a mode is not defined in PSDsoft, then other modes can be set by the microcontroller writing to the Port configuration registers. The PLD I/O, Data Port Address Input and Supervisory Function modes are NVM configurations. The other modes are initiated by the microcontroller.

If the NVM modes are not selected, the port can be altered dynamically between MCU I/O or Address Out modes by writing to the Control Register. Each bit of the eight-bit Control Register may store a "1", setting its respective bit in the port to MCU I/O, or to a "0", setting it to Address Out. The Direction Register or the output enable product term determine if the pin is input or output.

Table 22 summarizes the operating modes of the I/O ports. Not all the functions are available to every port. Table 23 shows how and where the different modes are configured.

### Table 22.  Port Operating Modes

| Port Mode | Port A | Port B | Port C | Port D |
|---|---|---|---|---|
| MCU I/O | Yes | Yes | Yes | Yes |
| PLD I/O<br>    McellAB Outputs<br>    McellC Outputs<br>    ECSPLD Outputs<br>    PLD Inputs | PA7$-$4<br>No<br>PA3$-$0<br>Yes | PB7$-$4<br>No<br>PB3$-$0<br>Yes | No<br>PC7$-$0<br>No<br>Yes | No<br>No<br>PD2$-$0<br>Yes |
| Address Out | Yes (A7$-$0) | Yes (A7$-$0, A15$-$8) | No | No |
| Address In | Yes | Yes | Yes | No |
| Data Port | Yes (D7$-$0) | Yes (D15$-$8) | No | No |
| Open Drain | Yes (PA7$-$4) | Yes (PB7$-$4) | Yes | No |
| Slew Rate | Yes (PA3$-$0) | Yes (PB3$-$0) | No | Yes |
| Peripheral I/O | Yes | No | No | No |
| Supervisory Function | No | No | Yes | No |

*I/O Ports*
*(cont.)*

**Port Operating Modes** (cont.)

**Table 23. Port Operating Mode Settings**

| *Mode* | *Defined In PSDabel* | *Defined In PSDconfiguration* | *Control Register Setting* | *Direction Register Setting* | *VM Register Setting* |
|---|---|---|---|---|---|
| MCU I/O | Declare pins only | NA | 0 | 1 = output, 0 = input (Note 1) | NA |
| PLD I/O | Logic equations | NA | NA* | (Note 1) | NA |
| Data Port (Port A,B) | NA | Specify bus type | NA | NA | NA |
| Address Out (Port A,B) | Declare pins only | NA | 1 | 1 (Note 1) | NA |
| Address In (Port A,B,C) | Logic equation for Input Micro⇔Cells | NA | NA | NA | NA |
| Peripheral I/O (Port A) | Logic equations (PSEL0 & 1) | NA | NA | NA | PIO bit = 1 |
| Supervisory Function | Logic equations (WDOG_EN and WDOG_CLR) | 1. Specify clock source 2. WatchDog configuration 3. Reset output 4. Reference voltage level 5. Standby voltage configuration | NA | NA | NA |

*NA – Not Applicable

NOTE 1:  The direction of the Port A, B, C pins are controlled by the Direction Register ORed with the individual output enable product term (.oe) from the GPLD AND array.

## I/O Ports
*(cont.)*

### PLD I/O Mode

The PLD I/O mode uses the port as an input to the GPLD Input Micro⇔Cell, and/or as an output from the GPLD, ECSPLD. The Port assignments are shown in Tables 10 and 11. The output can be tri-stated with a control signal defined by a product term (.oe) from the PLD, or, by setting a zero in the Direction Register. The Direction Register **must not** be set to "1" if the pin is defined as a PLD input pin. The PLD I/O mode is specified in PSDabel by declaring the port pins, then writing an equation assigning it to the port.

### MCU I/O Mode

In the MCU I/O Mode the microcontroller uses the PSD7XX ports to expand its own I/O ports. The ports on the PSD7XX are mapped into the microcontroller address space. The addresses of the ports are listed in Table 28.

A port pin will be put into MCU I/O mode by writing a zero to the corresponding bit in the Control Register. The direction may be changed by writing to the Direction Register for the port where a "1" makes it an output and  a "0" an input. The output enable product term also can change the direction of the pin (see Table 20 and 21). When the pin is configured as output, the content of the Data Out Register drives the pins. In input mode, the microcontroller reads the port input through the Data In buffer

Ports C and D do not have a Control Register and are in MCU I/O mode by default for pins that are not configured as PLD I/O.

### Address Out Mode

For microcontrollers with a multiplexed address/data bus, the ports in Address Out mode drive latched addresses to external devices. Address [7:0] are always assigned to Port A. See Table 29 for the address output pin assignments on Ports A and B. The Direction Register and the Control Register must be set to a "1" for port pins using Address Out mode.

In non-multiplexed 8 bit bus mode, address[7:0] are available on Port B in Address Out Mode.

## *I/O Ports*
*(cont.)*

### *Port Operating Modes (cont.)*

#### *Address In Mode*

For microcontrollers that have more than 16 address lines, the higher addresses can be connected to Port A, B, or C. The address input can be latched in the Input Micro⇔Cell by ALE. Any input that is included in the DPLD equations for the PSD EPROM and SRAM is considered as address input.

#### *Data Port Mode*

Port A and B can be used as data bus ports for a microcontroller with a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port A or B if the port is configured as Data Port.

#### *Supervisory Function Mode*

Port C (pins PC1–PC6) can be configured to implement the Supervisory Function. Refer to the Supervisory section for a detailed description.

#### *Peripheral I/O Mode*

Only Port A supports the Peripheral I/O mode where all of Port A I/O serves as a tri-state capable bi-directional data buffer of the microcontroller's data bus. Peripheral mode is enabled by setting Bit 7 of the VM Register to a "1". Figure 22 shows that when Peripheral mode is enabled and either PSEL0 and PSEL1 from the DPLD is active, Port A acts as a bi-directional buffer for the microcontroller D[7:0] data bus. The buffer is tri-stated when PSEL 0 or 1 is not active. The Peripheral I/O mode can be used to interface with external peripherals.

#### *Open Drain/Slew Rate Mode*

Ports A (pins PA7-4) and B (pins PB7-4) and C can be configured as an open drain instead of CMOS outputs. The Open Drain configuration is useful for sinking large currents to operate LEDs, for example. The Open Drain mode is enabled by writing a "1" to the corresponding bit in the Drive Register.

Port A (PA3–0), Port B (PB3–0) and Port D can be configured as ECSPLD outputs that have a high slew rate. The high slew rate is enabled by writing a "1" to the corresponding bit in the Drive Register.

#### *Figure 22.  Port A Peripheral Mode*
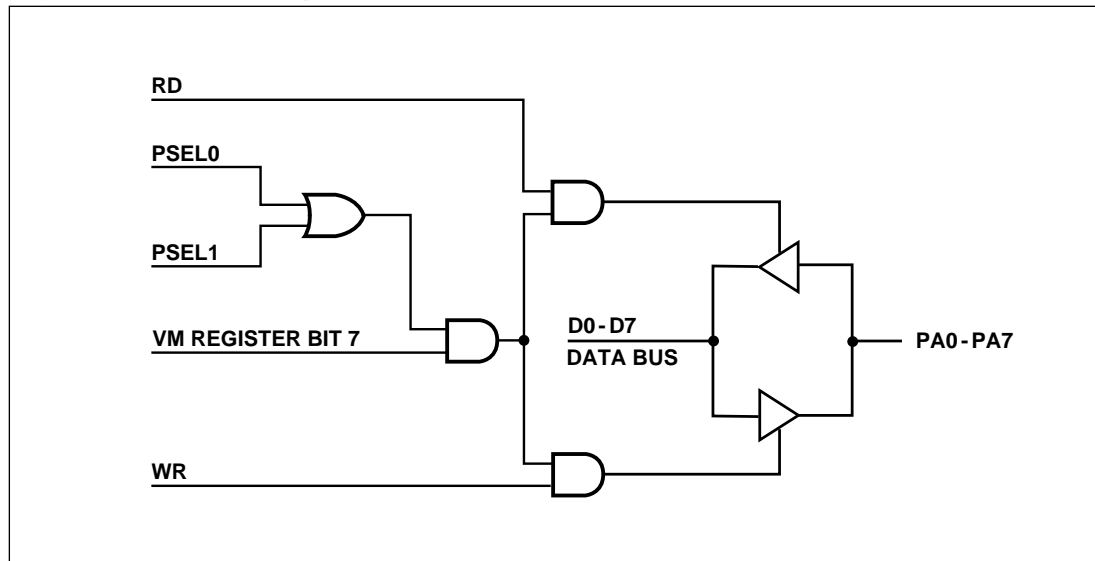
## I/O Ports
*(cont.)*

### Port Registers

Each port has a set of registers used for configuration (PCR, Port Configuration Registers) and data transfers (PDR, Port Data Registers). The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in Tables 28 and 28a. The register addresses are comprised of the CSIOP output from the DPLD plus an address offset as listed in the tables.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 in its port. The three Port Configuration Registers, shown in Table 24, are used for setting the port configuration. Each register is set to zero at power up.

### Table 24.  Port Configuration Registers

| Register Name | Port | MCU Access |
|---|---|---|
| Control | A,B | Write/Read |
| Direction | A,B,C,D | Write/Read |
| Drive* | A,B,C,D | Write/Read |

*Note: See Table 25 for Drive Register bit definition.

### Control Register

A zero in the Control Register sets the Port pin to MCU I/O for Port A and B.  A "1" sets the Port pin to Address Out mode. The default mode is MCU I/O.

### Direction Register

Controls the direction of data flow in the I/O Ports. A "1" configures the port to be an output, and a "0" to an input. The I/O configuration can be read from the Direction Register. The default mode is input.

As shown in the Port Architecture diagram, the direction of data flow in Port A,B and C pins are also controlled by the output enable (.oe) product term from the GPLD AND array. If the .oe product term is not active, the Direction Register has sole control of the pin direction.

An example of a configuration for a port with  the three least significant bits set to output and the remainder set to input is shown in Table 25. The Port D register has only the three least significant bits active.

### Table 25.  Port Direction Assignment Example

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

## *I/O Ports*
### *(cont.)*

### *Port Registers (cont.)*

#### *Drive Register*

The Drive Register configures the pin driver as Open Drain, or in the case of ECSPLD outputs, sets the pin to operate in high slew rate. An external pull-up resistor is not required when the pin is in the slew rate mode.

For Ports A and B the register sets different functions for the lower and higher nibbles. The four upper bits set the corresponding bits as CMOS ("0") or Open Drain ("1") driver. The four lower bits are used for slew rate control. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower, lower slope, response. The pin operates in high slew rate when the corresponding bit in the Drive Register is set to "1".

Table 26 shows the Drive Registers of Port A, B, C and D and which pin has the Open Drain or Slew Rate configuration.

#### *Table 26.   Drive Register Pin Assignment*

| Drive Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Port A | Open Drain | Open Drain | Open Drain | Open Drain | Slew Rate | Slew Rate | Slew Rate | Slew Rate |
| Port B | Open Drain | Open Drain | Open Drain | Open Drain | Slew Rate | Slew Rate | Slew Rate | Slew Rate |
| Port C | Open Drain | Open Drain | Open Drain | Open Drain | Open Drain | Open Drain | Open Drain | Open Drain |
| Port D | NA | NA | NA | NA | NA | Slew Rate | Slew Rate | Slew Rate |

**NOTE:**  NA  =  Not Applicable, bit should set to "0".

## *I/O Ports*
*(cont.)*

### Port Data Registers

The Port Data Registers, shown in Table 27, are used by the microcontroller to write or read data to or from the ports. Table 27 shows the register name, the ports having each register type and microcontroller access for each register. The registers are described below.

### *Table 27.  Port Data Registers*

| *Register Name* | *Port* | *MCU Access* |
|---|---|---|
| Data In | A,B,C,D | Read – the input on pin |
| Data Out | A,B,C,D | Write/Read |
| Output Micro⇔Cell | A,B,C | Read – outputs of Micro⇔Cells<br>Write – loading Micro⇔Cells Flip-Flop |
| Input Micro⇔Cell | A,B,C | Read – outputs of the Input Micro⇔Cells |
| Enable Out | A,B,C | Read – the output enable control of the port driver |

### *Data In*

Port pins are connected directly to the Data In buffer. In MCU I/O input mode,  the pin input is read through the Data In buffer.

### *Data Out Register*

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are driven out to the pins if the Direction Register or the .oe product term is set to "1". The contents of the register can also be read back by the microcontroller.

### *Output Micro⇔Cell*

The GPLD Output Micro⇔Cells occupy a location in the microcontroller's address space. The microcontroller can read the output of the Micro⇔Cells. Writing to the Micro⇔Cell loads data to the Micro⇔Cell Flip-Flops. Refer to the PLD section for more detail.

### *Input Micro⇔Cell*

The Input Micro⇔Cells can be used to latch or store external inputs. The outputs of the Input Micro⇔Cells are routed to the PLD input bus and also can be read by the microcontroller. Refer to the PLD section for detail description.

### *Enable Out*

The Enable Out buffer allows the microcontroller to read the outputs of the "OR" gate that is the enable input to the port output driver. A "1" indicates the driver is in output mode, a "0" indicates the driver is in tri-state and the pin is in input mode.

## I/O Ports
*(cont.)*

### Port Data Registers *(cont.)*

### Register I/O Address Offset

The base address of the Registers is defined in the CSIOP equation that occupies 256 bytes of address space and is defined by the user in PSDsoft. The lower address byte A[7:0], or address offset, selects the register. Table 28 shows the address offset for all MCUs except those Motorola microcontrollers with a 16-bit data bus. Table 28A shows the address offset for Motorola MCUs in 16-bit mode.

For example, when the CSIOP is defined to occupy the address range of 1000h to 10FFh in PSDabel, the address of the Port A Control Register is then 1002h.

**Table 28. I/O Register Address Offset (relative to CSIOP)**

| Register Name | Port A | Port B | Port C | Port D |
|---|---|---|---|---|
| Data In | 00 | 01 | 10 | 11 |
| Control | 02 | 03 | | |
| Data Out | 04 | 05 | 12 | 13 |
| Direction | 06 | 07 | 14 | 15 |
| Drive | 08 | 09 | 16 | 17 |
| Input Micro⇔Cell | 0A | 0B | 18 | |
| Enable Out | 0C | 0D | 1A | |
| Output Micro⇔Cell | 20 | 20 | 21 | |

**Table 28A. Register Address Offset for 16-Bit Motorola Microcontrollers in 16-Bit Mode (relative to CSIOP)**

| Register Name | Port A | Port B | Port C | Port D |
|---|---|---|---|---|
| Data In | 01 | 00 | 11 | 10 |
| Control | 03 | 02 | | |
| Data Out | 05 | 04 | 13 | 12 |
| Direction | 07 | 06 | 15 | 14 |
| Drive | 09 | 08 | 17 | 16 |
| Input Micro⇔Cell | 0B | 0A | 19 | |
| Enable Out | 0D | 0C | 1B | |
| Output Micro⇔Cell | 21 | 21 | 20 | |

## I/O Ports
*(cont.)*

## Port A and B – Functionality and Structure

Port A and B have similar functionality and structure as shown in Figure 23. The two ports can be configured to perform one or more of the following functions:

❏ MCU I/O Mode

❏ GPLD Output – Micro⇔Cells McellAB[7:4] can be connected to Port A PA[7:4} or Port B PB[7:4].

❏ ECSPLD Output – External chip select output can be connected to either Port A PA[3:0] or Port PB[3:0].

❏ Latched Address output – Provide latched address output per Table 29.

❏ Address In – Additional high address inputs using the Input Micro⇔Cells.

❏ Open Drain/Slew Rate – pins PA[3:0] and PB[3:0] can be configured to Open Drain Mode pins PA[7:4] and PB[7:4] can be configured to fast slew rate

❏ Data Port – Port A to D[7:0} for 8 bit non-multiplexed bus Port B to D[15:8] for 16-bit non-multiplexed bus

❏ Peripheral Mode – Port A only

### Table 29. I/O Port Latched Address Output Assignments

| Microcontroller | Port A (3:0) | Port A (7:4) | Port B (3:0) | Port B (7:4) |
|---|---|---|---|---|
| 8051XA (8-Bit) | N/A* | Address (7:4) | Address (11:8) | N/A |
| 80C251 (Page Mode) | N/A | N/A | Address (11:8) | Address (15:12) |
| All Other 8-Bit Multiplexed | Address (3:0) | Address (7:4) | Address (3:0) | Address (7:4) |
| 8051XA (16-Bit) | N/A | Address (7:4) | Address (11:8) | Address (15:12) |
| All Other 16-Bit Multiplexed | Address (3:0) | Address (7:4) | Address (11:8) | Address (15:12) |
| 8-Bit Non-Multiplexed Bus | N/A | N/A | Address (3:0) | Address (7:4) |

N/A = Not Applicable.

**I/O Ports**
*(cont.)*

**Figure 23.  Port A and B Structure**
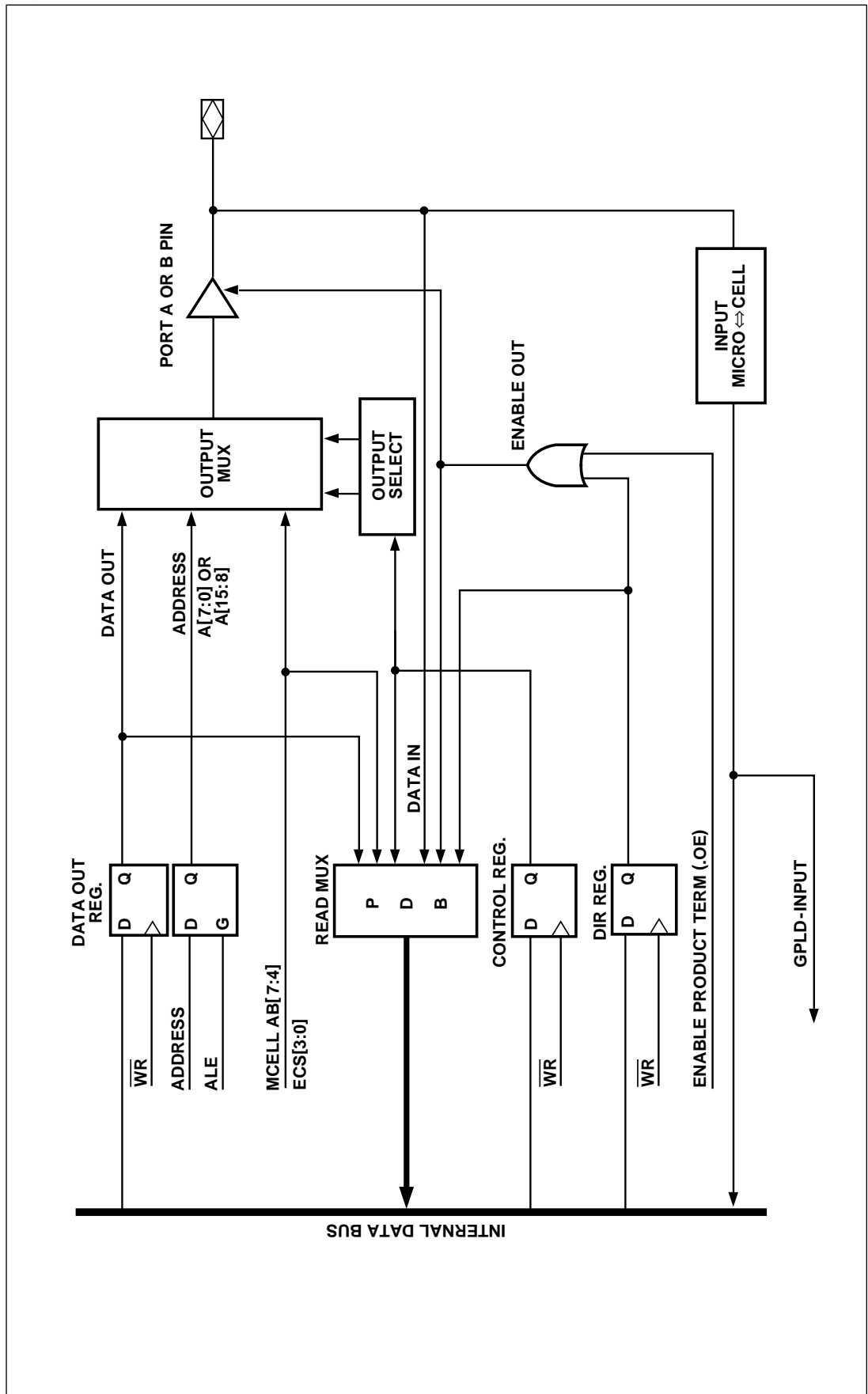
## I/O Ports
*(cont.)*

### Port C – Functionality and Structure

Port C does not support Address Out mode and the Control Register is not required. Port C can be  configured to perform one or more of the following functions:

❏ MCU I/O Mode

❏ GPLD Output  –  McellC outputs can be connected to Port C pins

❏ GPLD Input  –  via the eight Input Micro⇔Cells

❏ Address In  –  Additional high address inputs using the Input Micro⇔Cells.

❏ Open Drain  –  Port C pins can be configured in Open Drain Mode

❏ Supervisory Function – Port C (PC1 – PC6) pins can be configured to perform the Supervisory Function.

Pin PC7 may be configured as the $\overline{WRH}$ input in certain microcontroller interface designs.

### Port D – Functionality and Structure

Port D has only three I/O pins, does not support Address Out mode, and no Control Register is required. Port D can be  configured to perform one or more of the following functions:

❏ MCU I/O Mode

❏ ECSPLD Output  –  External chip select output

❏ PLD Input  –  direct input to PLD, no Input Micro⇔Cells

❏ Slew rate  –  pins can be set up for fast slew rate

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

❏ PD0  –  ALE, as address strobe input

❏ PD1  –  CLKIN, as clock input to the Micro⇔Cells Flip-Flops and APD counter

❏ PD2  –  CSI, as active low chip select input. A high input will disable the PSD EPROM/SRAM.

*I/O Ports*
*(cont.)*

*Figure 24.  Port C Structure*
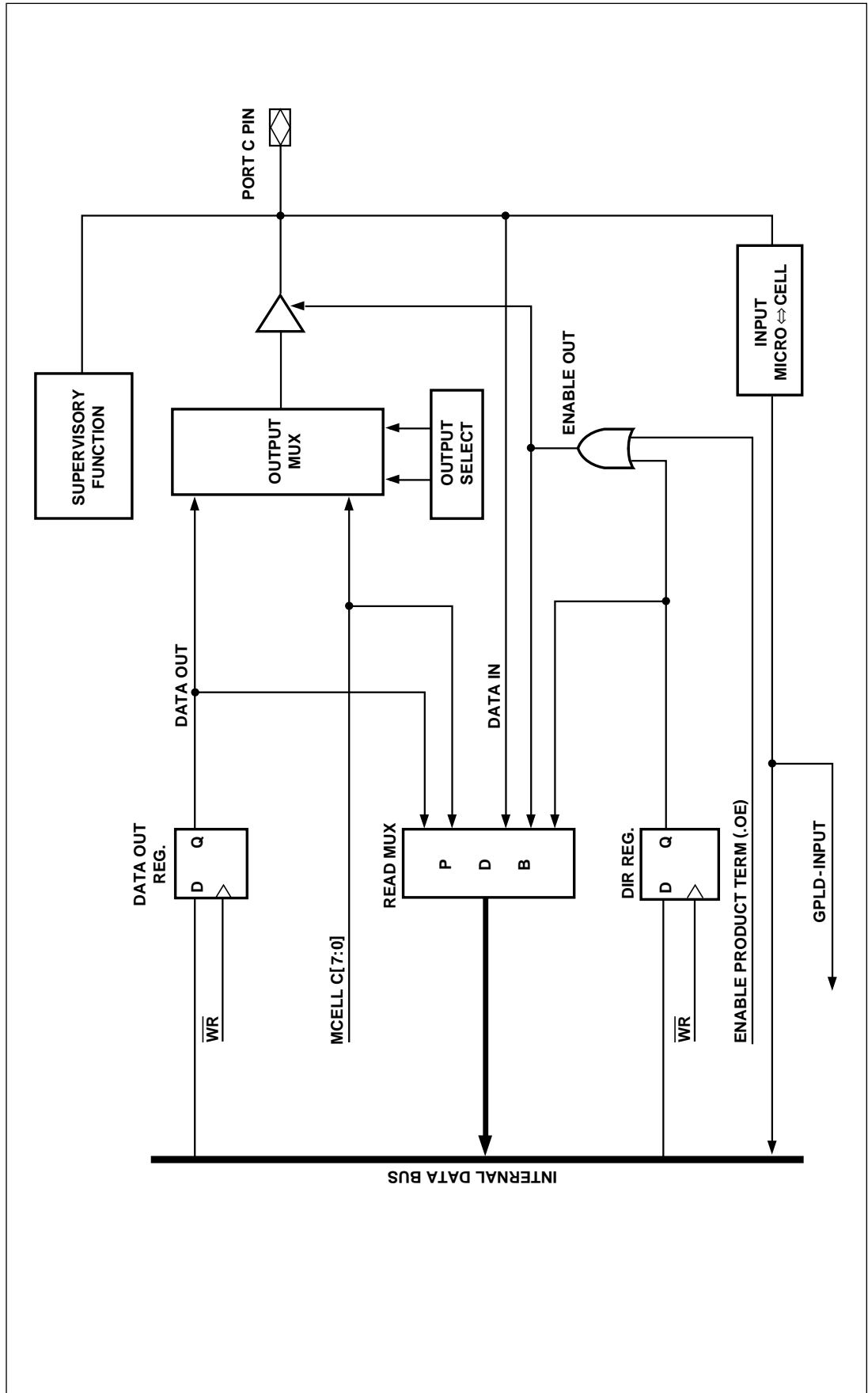
## I/O Ports
(cont.)

**Figure 25.  Port D Structure**
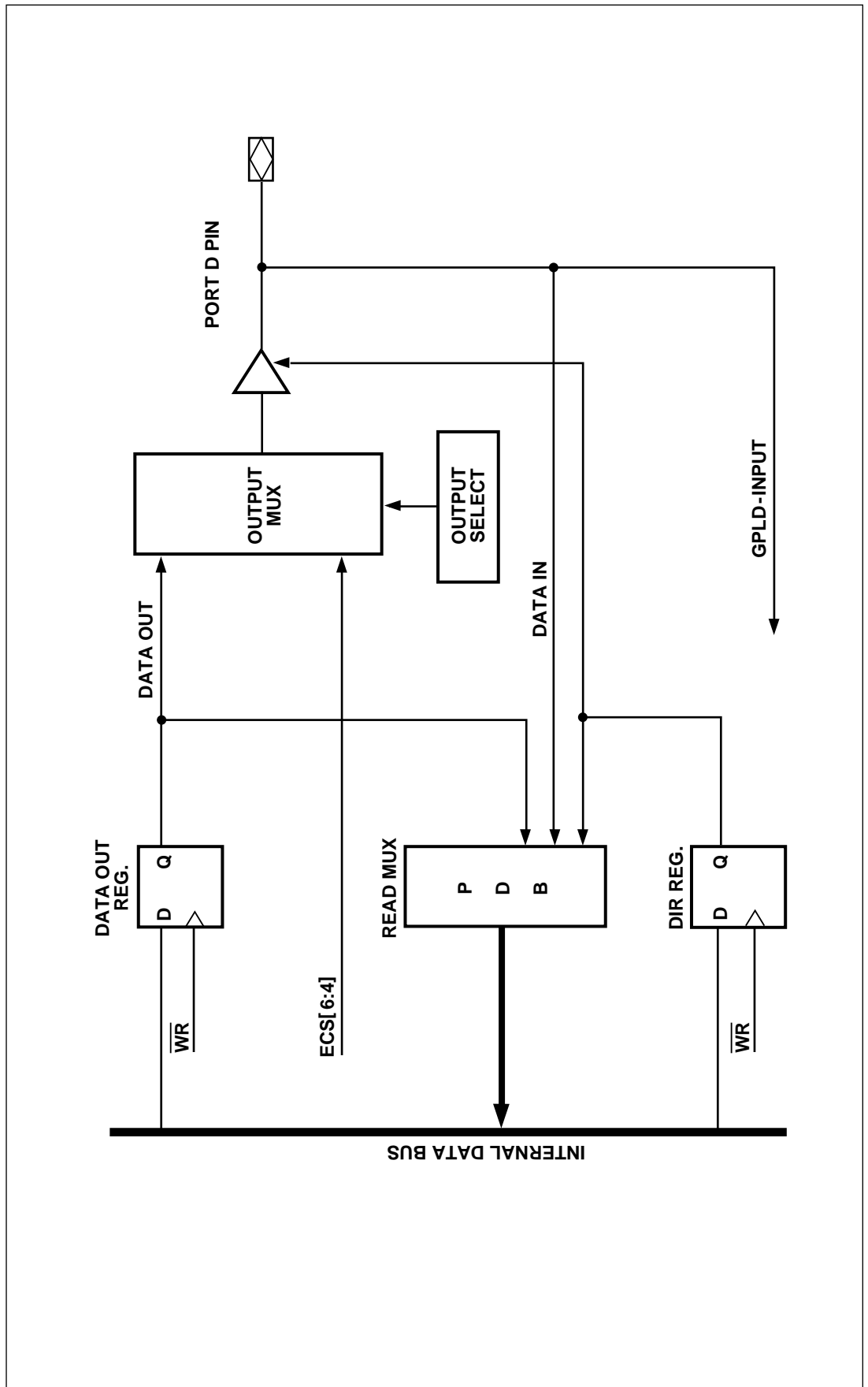
## Memory Blocks

The PSD7XX has internal EPROM and SRAM memory blocks. The memory select signals come from the DPLD and are user-defined in the PSDsoft Software.

### EPROM

The PSD7XX provides three EPROM densities:  256K bit, 512K bit or 1M bit. The EPROM is divided into eight  blocks. The EPROM can be configured as 32K x 8, 64K x 8 or 128K x 8 for eight-bit data busses and 16K x 16, 32K x 16 or 64K x 16 for 16-bit data buses.

Each block has its own EPROM select. Blocks zero to six have one select (ES0-ES6) and block 7 has two selects, ES7A and ES7B, either of which enables Block 7. The dual selects allow Block 7 to reside in two separate memory spaces.

A typical application would be to store an MCU reset vector residing in the memory space and accessed by ES7B. The rest of the Block 7 memory space would be accessed by ES7A. The same technique can also be used to store the Configuration bytes of the Intel 80251 microcontroller which reside at the high end of the memory space.

### SRAM

The SRAM has 4K bits of memory that can be configured as 512 x 8 or 256 x 16. The SRAM is enabled from the RS0 output of the DPLD. The SRAM has a battery back-up mode which is automatically invoked when the supply voltage drops under the standby voltage. SRAM write protection is provided in back-up mode.

### Memory Select Map

The EPROM and SRAM select are outputs from the DPLD whose equations are defined using PSDabel. The following rules apply to the memory space definitions:

1. EPROM block select space should not be larger than the physical block size
2. EPROM block select space must not overlap
3. SRAM, I/O and Peripheral I/O spaces cannot overlap
4. SRAM, I/O and Peripheral I/O spaces can overlap EPROM with priority given to the SRAM or I/O. This allows the SRAM or I/O to utilize the EPROM space that is not used.

## Memory Blocks
*(cont.)*

### Page Register

The four-bit Page Register increases the addressing capability of the microcontroller by a factor of 16. The contents of the Register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR3) are inputs to the PLD and can be included in the EPROM or SRAM chip select equations.

Figure 26 shows the Page Register. The four Flip-Flops in the Register are connected to the internal data bus D0–D3. The microcontroller can write to or read from the Page Register. The Register can operate as an independent register to the microcontroller if page mode is not implemented.

*Figure 26. Page Register for Memory Bank Switching*
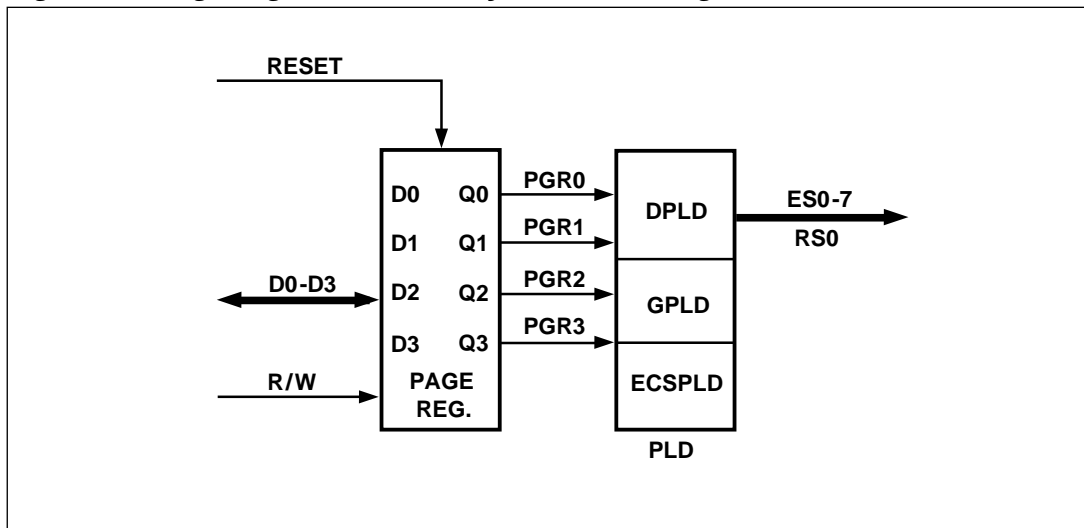


### Security Protection

The PSD7XX has a programmable security bit which acts as a duplication barrier. When the bit is set, the contents of the EPROM, non-volatile configuration bits, and PLD cannot be read by device programmers.

The security bit is set through the PSDsoft Design Tools and is embedded in the compiled output file. The security bit is UV erasable and a secured PSD7XX in a windowed package can be erased and re-programmed.

## Memory Blocks
*(cont.)*

### Memory Select for 8031 Microcontrollers

The 8031 family of microcontrollers, including 80C251 and 80C51XA, has a separate address space for code memory (enabled by $\overline{PSEN}$) and data memory (enabled by $\overline{RD}$). The PSD7XX allows the EPROM and SRAM to reside in the program space, data space or both. Three different configurations are possible:

❏ **Separate Space Mode**

   Code memory space is separated from data memory space. The $\overline{PSEN}$ signal is used to access the program code from the EPROM, and the $\overline{RD}$ signal is used to access data from the SRAM and I/O Ports. This is the default configuration.

❏ **Combined Space Mode**

   The program and data memory spaces are combined into one 64KB block space that allows the EPROM or SRAM to be accessed by either $\overline{PSEN}$ or $\overline{RD}$. The EPROM and SRAM blocks address space must not overlap. This mode is enabled by the microcontroller by setting the bits in the VM Register as shown in Table 30. If Bit 0 is "1", either $\overline{PSEN}$ or $\overline{RD}$ can access the SRAM. If Bit 1 is a "1", either $\overline{RD}$ or $\overline{PSEN}$ can access the EPROM. Figure 26 shows the memory select logic for Combined Space Mode.

❏ **Mixed Mode**

   Allows individual EPROM blocks to be configured in either Data Space or Program Space. EPROM block chip selects must be qualified with the 8031 $\overline{RD}$ input in the ES0−ES7 equations. An active low $\overline{RD}$ will select EPROM blocks in data space and disable the blocks that are in program space. For EPROM blocks that reside in data space, the access time is calculated from $\overline{RD}$ valid to data valid. This mode is set automatically by PSDsoft whenever the $\overline{RD}$ signal is included in the EPROM chip select equations.

### Table 30.   VM Register

| Bit 7 PIO_EN | Bit 6* | Bit 5* | Bit 4* | Bit 3* | Bit 2* | Bit 1 RD_EN | Bit 0 PSEN_EN |
|---|---|---|---|---|---|---|---|
| 0 = disable PIO mode | | | | | | 0 = RD access SRAM, I/O | 0 = PSEN access EPROM only |
| 1 = enable PIO mode | | | | | | 1 = RD access EPROM, SRAM, I/O | 1 = PSEN access EPROM, SRAM, I/O |

*Bit 6-2 are not used, set to "0".
 Bits 7, 1 and 0 are set to "0" after reset.

**Memory Blocks**
*(cont.)*

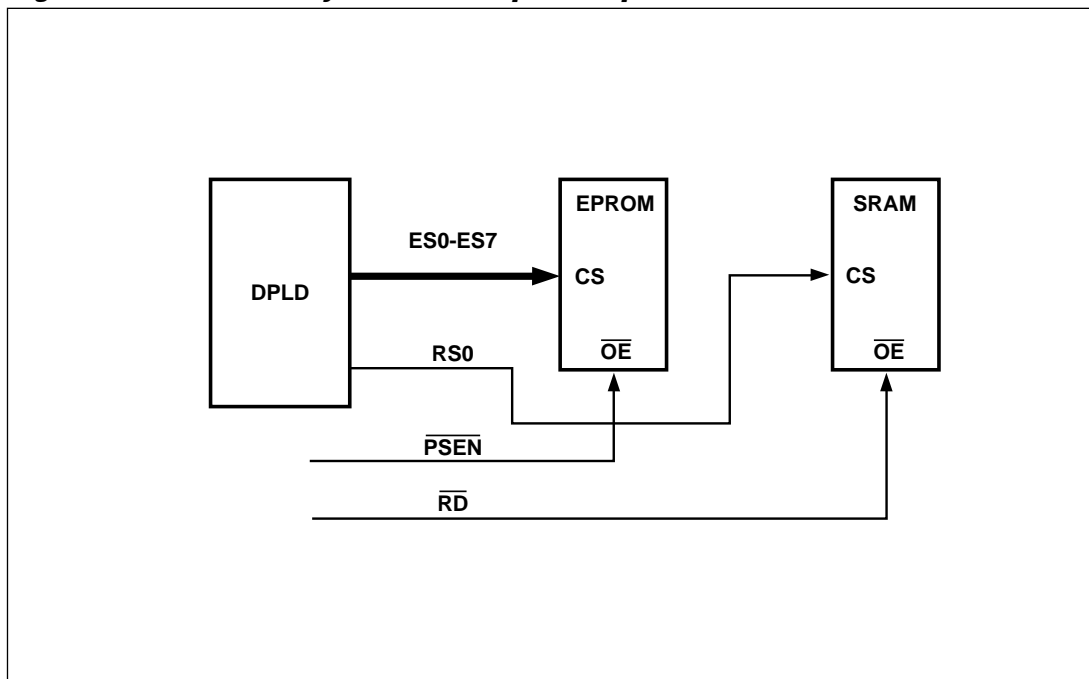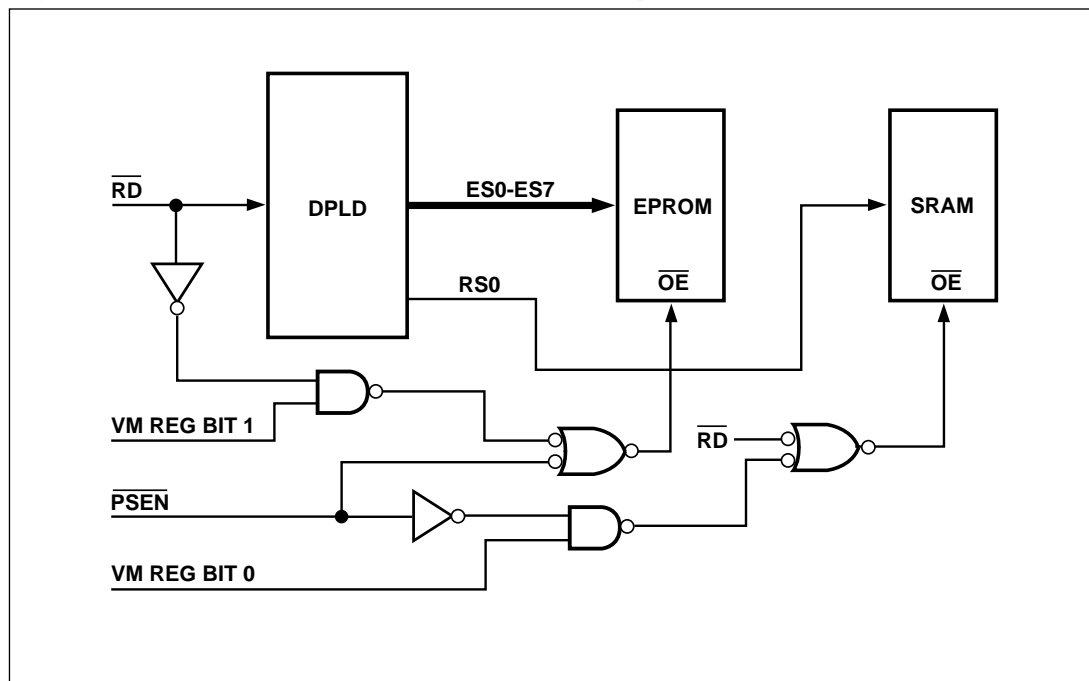*Figure 27.  8031 Memory Modes  –  Separate Space Mode*



*Figure 28.  80C31 Memory Mode  –  Combined Space Mode*

## *Power Management Unit*

The PSD7XX offers a number of configurable power saving options which include the Automatic Power Down (APD) Logic and the Power Management Mode Registers (PMMR0 and PMMR1). The APD Logic allows the PSD7XX to enter into either Power Down or Sleep Mode automatically, while the PMMRs can be configured at run time by the microcontroller to selectively reduce the power consumption of the PSD functional blocks.

### *The APD Logic and Power Down Mode*

The Automatic Power Down (APD) logic puts the PSD7XX into power savings mode by monitoring the activity of the address strobe (ALE/AS). If the APD unit is enabled, the four-bit APD counter starts counting whenever the address strobe is inactive. If the strobe remains inactive for fifteen CLKIN clock periods, the power down (PDN) signal will become active and the PSD7XX enter into either Power Down or Sleep Mode. Immediately after ALE starts pulsing the PSD7XX will return to normal operation. The APD counter clock source comes from the CLKIN pin which is pin PD1 on Port D or the Superv_Clk from the Supervisory Function. In order to guarantee that the APD counter will not overflow when enabled, there should be less than 15 clocks between two successive ALE pulses.

Usually, microcontrollers entering power down mode will freeze their ALE at logic high or low level. By programming bit 0 of PMMR0, the APD knows when the MCU is in power down mode. If the APD detects the ALE level is in the power down state for 15 CLKIN periods, then the PSD7XX will enter a power down mode. To enable the APD operation, the APD bit in the PMMR0 should be set to "1".

When the address strobe starts pulsing again, or the CSI input switches from high to low, the PSD7XX will return to normal activity.

When the PDN signal is set to "1" (active state) in Power Down (or Sleep Mode), the PSD7XX MCU bus interface is disabled and all MCU inputs (address, data and control signals) are blocked from entering the device. If the clock input to the PLD is not needed in Power Down mode, it should be blocked to save power by setting Bit 4 and 5 in the PMMR0 to "1".

### *Sleep Mode*

The Sleep Mode is activated if the Sleep mode bit, the APD bit and the ALE Polarity bit in the PMMRs are set, and the APD Counter has overflowed after 15 CLKIN clocks (see Figure 29). In Sleep Mode the PSD7XX consumes less power than the Power Down Mode, with typical $I_{CC}$ reduced to 25µA.

In this mode, the PLD still monitors the inputs and responds to them. As soon as the ALE starts pulsing or the CSI input switches from high to low, the PSD7XX exits the Sleep Mode. The PSD7XX access time from Sleep Mode is specified by tLVDV1. The PLD response time to an input transition is specified by tLVDV2.

### *Table 31.  Power Down Effect on Ports*

| Port Function | Pin Level |
|---|---|
| MCU I/O | No Change |
| PLD Out | No Change |
| Address Out | Undefined |
| Data Port | Three-State |
| Peripheral I/O | Three-State |

*Power
Management
Unit
(cont.)*

*Table 32.  Summary of PSD7XX Timing and Standby Current During
Power Down and Sleep Mode*

| Mode | PLD Propagation Delay | PLD Recovery Time to Normal Operation | Access Time | Access Recovery Time to Normal Access | Typical Standby Current |
|------|------------------------|----------------------------------------|-------------|----------------------------------------|--------------------------|
| Power Down | Normal tpd (Note 1) | 0 | No Access | tLVDV | 50µA (Note 4) |
| Sleep | tLVDV2 (Note 2) | tLVDV3 (Note 3) | No Access | tLVDV1 | 25µA (Note 4) |

**NOTES:**  1. Power Down does not affect the operation of the PLD.
2. In Sleep Mode any input to the PLD will have a propagation delay of tLVDV2.
3. PLD recovery time to normal operation after existing Sleep Mode. An input to the PLD during the transition will have a propagation delay of tLVDV3.
4. Typical current consumption assuming CLKIN is disabled.

*Figure 29.  APD Logic Block*

*Power Management Unit*
*(cont.)*
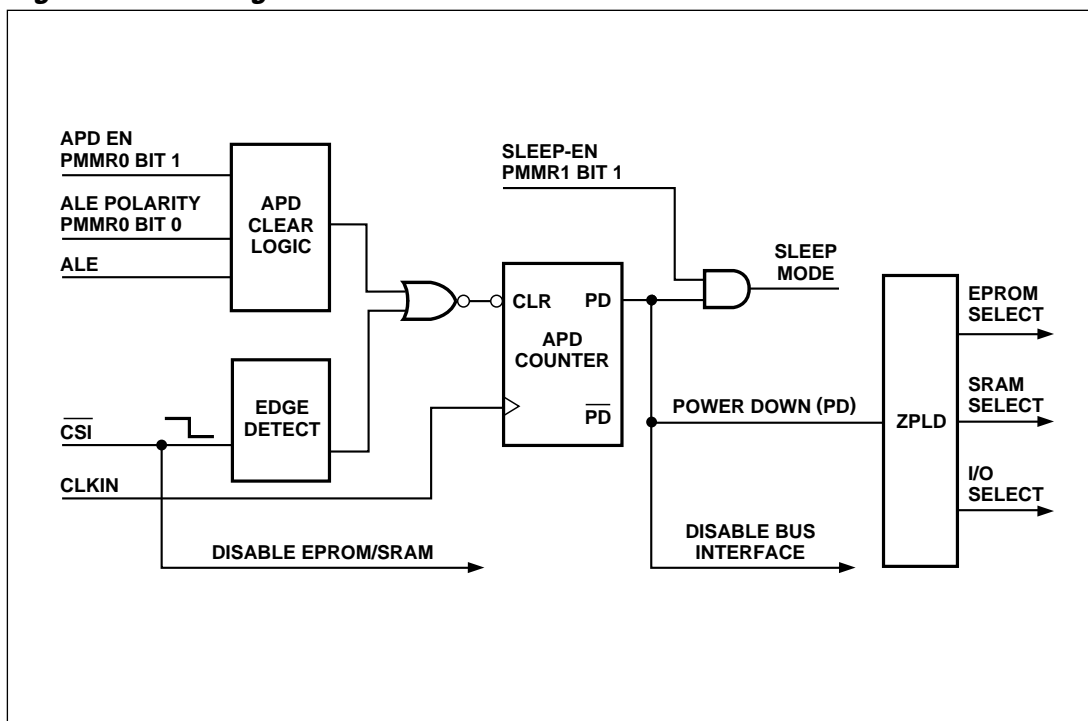
**Figure 30. Enable Power Down Flow Chart**

```
                          RESET
                            │
                  ┌─────────────────────┐
                  │    APD DISABLED      │
                  └─────────────────────┘
                            │
                  ┌─────────────────────┐
                  │  SET ALE POLARITY    │
                  │   IN PMMR0 BIT 0     │
                  └─────────────────────┘
                            │
                       ◇ NEED         YES    ┌──────────────────────┐
                         SLEEP  ─────────────▶│  ENABLE SLEEP MODE    │
                         MODE ◇               │  SET PMMR1 BIT 1      │
                            │                 └──────────────────────┘
                           NO                           │
                  ┌─────────────────────┐     ┌──────────────────────┐
                  │    ENABLE APD        │     │     ENABLE APD        │
                  │ SET PMMR0 BIT 1 = 1  │     │ SET PMMR0 BIT 1 = 1   │
                  └─────────────────────┘     └──────────────────────┘
                            │                           │
                  ┌─────────────────────┐     ┌──────────────────────┐
                  │  DISABLE PLD CLKIN   │     │  DISABLE PLD CLKIN    │
                  │ SET PMMR0 BIT 4,5 = 1│     │ SET PMMR0 BIT 4,5 = 1 │
                  └─────────────────────┘     └──────────────────────┘
                            │                           │
                   ALE IDLE AND                ALE IDLE AND
                   15 CLKIN CLOCK              15 CLKIN CLOCK
                            │                           │
                  ┌─────────────────────┐     ┌──────────────────────┐
                  │      PSD7XX          │     │  PSD7XX IN SLEEP MODE │
                  │  IN POWER DOWN MODE  │     └──────────────────────┘
                  └─────────────────────┘
```
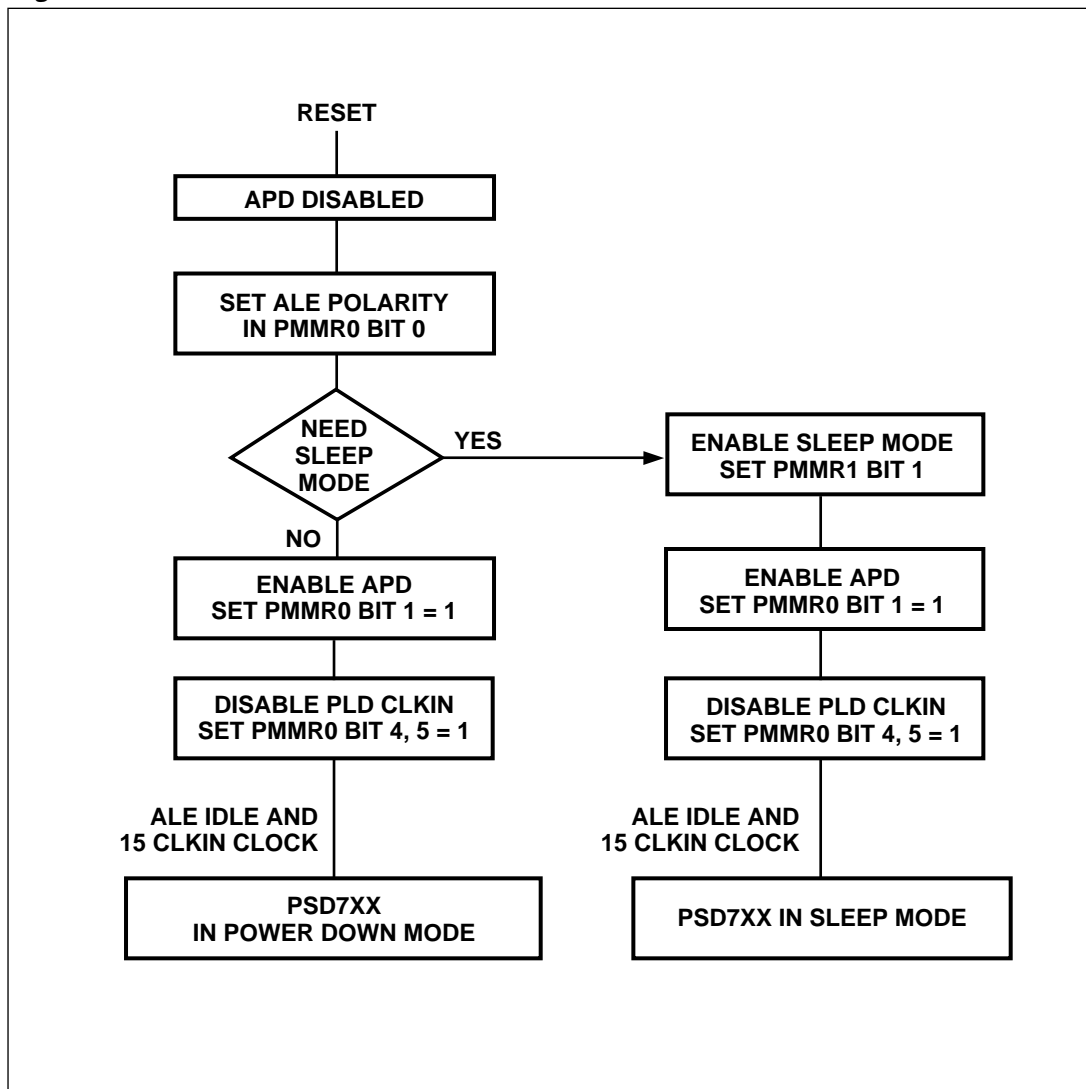
*Power
Management
Unit*
*(cont.)*

### Table 33.  Power Management Mode Registers (PMMR0, PMMR1)**

**PMMR0**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| * | Superv clk | PLD Mcell clk | PLD Array clk | * | CMiser | APD Enable | ALE PD Polarity |
| | 1 = off | 1 = off | 1 = off | | 1 = on | 1 = on | 1 = high |

*Bits 3 and 7 are not used, and should set to 0.

**Both the PMMR0 and PMMR1 register bits are clear to zero following power up.
Subsequent reset pulses will not clear the registers.

Bit 0   0 = ALE power down polarity low
        1 = ALE power down polarity high

Bit 1   0 = Automatic Power Down (APD) is disabled
        1 = Automatic Power Down (APD) is enabled

Bit 2   0 = EPROM/SRAM CMiser is off
        1 = EPROM/SRAM CMiser is on

Bit 4   0 = CLKIN input to the PLD AND array is connected
            Every CLKIN change will power up the PLD when Turbo bit is off
        1 = CLKIN input to PLD AND array is disconnected

Bit 5   0 = CLKIN input to the PLD Micro⇔Cells is connected
        1 = CLKIN input to the PLD Micro⇔Cells is disconnected

Bit 6   0 = Supervisory Clock input to the GPLD is connected
        1 = Supervisory Clock input to the GPLD is disconnected

**PMMR1**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| * | * | * | * | * | * | Sleep Mode Enable | APD Clk Source |
| | | | | | | 1 = on | 1= CLKIN |

*Unused bits should be set to 0.

Bit 0   0 = Supervisory Clock serves as APD clock
        1 = CLKIN serves as the APD clock

Bit 1   0 = Sleep Mode is Disabled
        1 = Sleep Mode is Enabled

### Table 34.  APD Counter Operation

| APD Enable Bit | ALE PD Polarity | ALE Level | APD Counter |
|---|---|---|---|
| 0 | X | X | Not Counting |
| 1 | X | Pulsing | Not Counting |
| 1 | 1 | 1 | Counting (Generates PDN after 15 Clocks) |
| 1 | 0 | 0 | Counting (Generates PDN after 15 Clocks) |

*Power
Management
Unit*
*(cont.)*

## Other Power Saving Options

The PSD7XX offers other reduced power saving options that are independent of the
Power Down or Sleep Mode. Except for the SRAM Standby and CSI input features, they are
enabled by setting bits in the PMMR 0 register.

❏ **CMiser Bit**

The CMiser bit resides in PMMR0. This bit controls the AC power consumption and
access time of the EPROM and SRAM. When in 8 bit data bus mode and CMiser is set,
the PSD7XX will consume the lowest level of AC power. However, the access time will
be slower (see CMiser adder in timing parameters). When CMiser bit is off, the AC
power is higher and the PSD7XX will return to standard access time.

❏ **SRAM Standby Mode**

The SRAM has a Vstby pin (PC2) that can be connected to a battery. When $V_{CC}$
becomes lower than Vstby then the PSD7XX will automatically connect the Vstby as
a power source to the SRAM. The SRAM Standby Current (Istby) is typically 0.5µA.
SRAM data retention voltage is 2V minimum.

❏ **The CSI Input**

Pin PD2 of Port D can be configured in PSDsoft as the CSI input . When low, the signal
selects and enables the internal EPROM and SRAM for read or write operations.
A high on the CSI pin will disable the EPROM and SRAM and reduce the PSD power
consumption. However, the PLD remains operational when CSI is high.

❏ **Input Clock**

The PSD7XX provides the option to turn off the CLKIN and the Supervisory Clock
input to the PLD to save AC power consumption. The CLKIN is an input to the PLD
AND array and the Output Micro⇔Cells. During power down or if any of the CLKIN
input is not being used as part of the PLD logic equation, the clock should be disabled
to save AC power.

The CLKIN will be disconnected from the PLD AND array or the Micro⇔Cells by
setting bit 4 or 5 to "1" in the PMMR0.

## Supervisory Function

The Supervisory Function in the PSD7XX significantly improves microcontroller system reliability with programmable features such as power supply monitoring, reset control and WatchDog Timer.

These features are:
❏ 5% and 10% power supply monitoring
❏ Reset generation based on various conditions:
  – Power-On reset; voltage comparator with programmable internal or external trip point
  – Push Button or System reset input
  – WatchDog Timer output
❏ User programmable WatchDog Timer (controlled by PPLD product terms).
❏ Battery-backup of internal SRAM.
❏ Write protect of internal SRAM and external memory.
❏ Reset input debouncer filter.
❏ Programmable reset pulse width generator

Figure 31 is the block diagram of the Supervisory Function. The input and output supervisory pins are listed in Table 35. Pins that are not used can be configured for other PSD7XX I/O functions. Table 36 shows the inputs and outputs of the PPLD that are involved in controlling the Supervisory Function.

### Table 35. Supervisory I/O Pins

| Input Pin | | Output Pin | |
|---|---|---|---|
| **Pin Name** | **Description** | **Pin Name** | **Description** |
| VSTBY (PC2) | SRAM Battery Backup input | VSTBYON (PC4) | Pin is driven high when PSD7XX is switched over to Standby Voltage |
| VTRIP (PC6) | External Trip voltage input for the voltage comparator | CEOUT (PC3) | Chip select output that can be used for external non-volatile writable memory. This chip select becomes inactive automatically when the PSD7XX is switched to standby voltage. Use to conserve power in external battery backup SRAM or prevent unwanted writes to external EEPROM, SRAM, or FLASH. |
| $\overline{\text{RESET}}$ | System or push button reset input | RST_OUT (PC5) | Active high reset output |
| CLKIN (PD1) | External clock input | $\overline{\text{RST\_OUT}}$ (PC1) | Active low reset output |

*Supervisory*
*Function*
*(cont.)*

### Table 36.  PPLD Supervisory I/O Signals

| Input Signals | Description | Output Signals | Description |
|---|---|---|---|
| $\overline{\text{GRESET}}$ or $\overline{\text{ERESET}}$ | Reset generated by the WatchDog Timer, Voltage Comparator or Reset pin input. ERESET is the output of the Pulse Generator that is triggered by GRESET. GRESET or ERESET is an active low signal. | WDOG_EN | A product term that enables the WatchDog Timer. An active high pulse of minimum 20ns duration. |
| WDOG_ON | Active high WatchDog output. Will remain active until the WatchDog is cleared by WDOG_CLR. | WDOG_CLR | A product term that clears and re-loads the WatchDog Timer. An active high pulse of minimum 20ns duration. |
| GPLD Inputs | Other GPLD inputs, refer to the GPLD chapter. | | |
| SUPERV_CLK | The clock generated by the Supervisory Function. If the WatchDog Timer runs on the internal oscillator, SUPERV_CLK is connected to the 2KHz oscillator. Otherwise SUPERV_CLK is connected to the external CLKIN/8192. | | |

## *Supervisory Function* (cont.)
### *Figure 31. Supervisory Function Block Diagram*
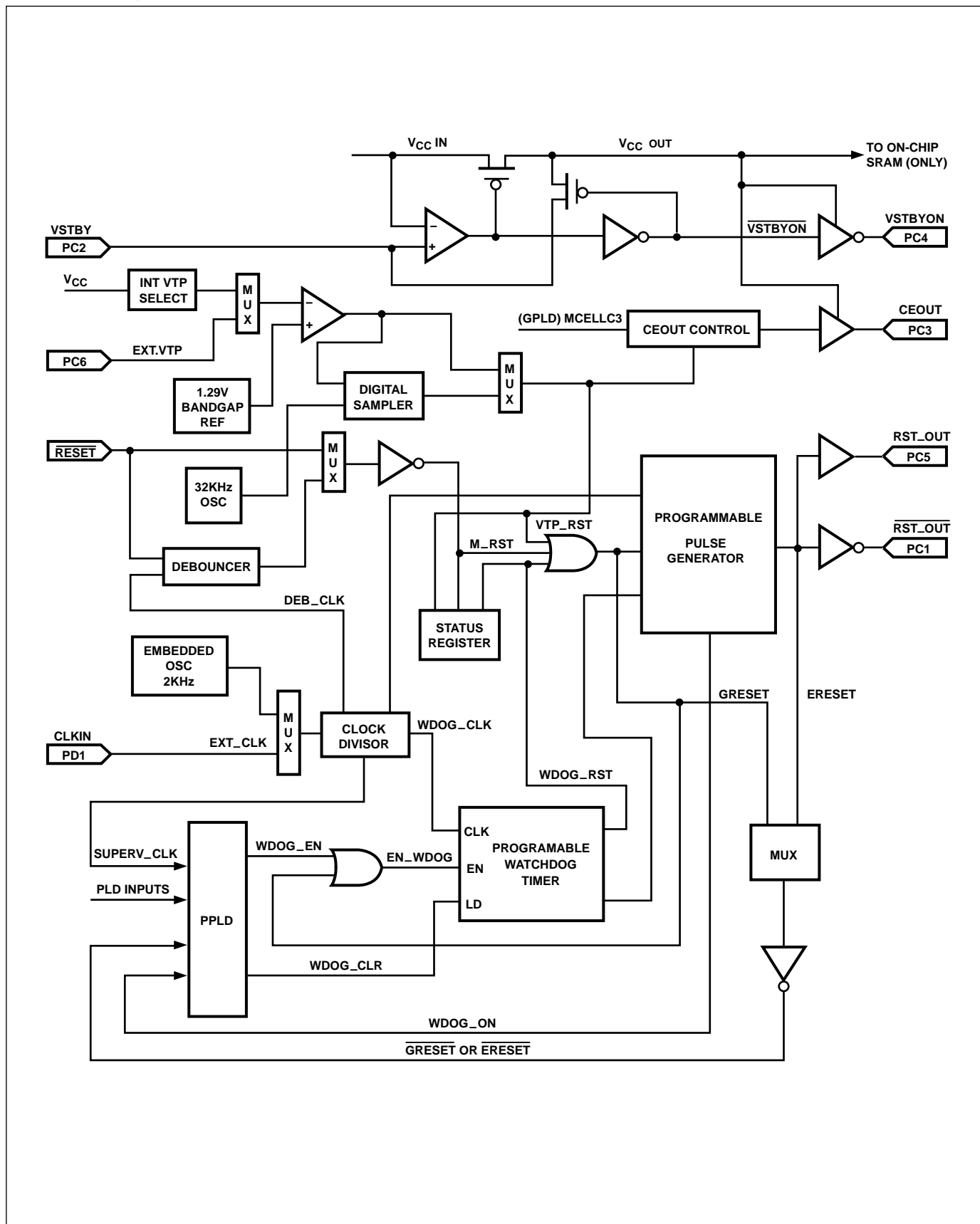
*Supervisory*
*Function*
*(cont.)*

### Reset Generation

The PSD7XX can generate output reset signals that go out to the external peripherals and the microcontroller. Three sources are capable of issuing reset:

❏  Power-On reset; voltage comparator with programmable internal or external trip point.
❏  Push button or system reset input from the RST pin.
❏  WatchDog Timer timeout output when enabled

The microcontroller can read the PSD7XX Status Register to determine the source of the reset. The internal global reset (GRESET) can be brought out to pins on Port C as an active low or high output. The width of the extended reset output (ERESET) pulse is user configurable and is controlled by the Programmable Pulse Generator. Either GRESET or ERESET (active high) can be declared as an internal node in PSDabel and participate in the logic equation definition.

### Push Button Reset Input

The PSD7XX has a dedicated active-low reset input pin that can be connected to a system reset or a push button reset. The system reset is a direct input to the reset generator, while the Push Button input is routed through a selectable debouncer filter that filters out transitions shorter than three clock cycles. The clock source of this debouncer is either a 125Hz internal oscillator or CLKIN/128K.

Figure 46 shows the reset pin input timing requirement. The active low range has a minimum tNLNH duration. After the rising edge of reset, the PSD7XX remains in the reset state during tOPR range. Table 37 shows the I/O pin status of the PSD7XX during the reset and power down mode.

### *Table 37.  Status During Reset and Power Down Mode*

| *Port Configuration* | *Reset* | *Power Down Mode* |
|---|---|---|
| MCU I/O | Input | Unchanged |
| PLD Output | Active | Depends on inputs to the PLD |
| Address Out | Tri-stated | Not defined |
| Data Port | Tri-stated | Tri-stated |
| Peripheral I/O | Tri-stated | Tri-stated |

| *Register* | *Reset* | *Power Down Mode* |
|---|---|---|
| PMMR0  & 1 | Cleared (power up reset) | Unchanged |
|  | Unchanged (warm reset) |  |
| Micro⇔Cell Flip-Flop | Unchanged* | Unchanged* |
| All other registers | Cleared to "0" | Unchanged |

*The Micro⇔Cell flip-flop can be cleared or set by the reset input or the PDN (Power Down) signal, depending on the .re and .pr equations that are defined in the PSDabel file.

## *Supervisory Function*
*(cont.)*

### *The Power Monitor*

The Power Monitor circuitry monitors the $V_{CC}$ supply and generates a reset pulse whenever $V_{CC}$ drops below the selected reference voltage. The Voltage Comparator compares $V_{CC}$ either with an internally generated reference voltage or with an external reference voltage applied at the Vtp (PC6) pin.

The voltage comparator output can be applied directly to the reset generator or go through a 100-microsecond digital sampler. The digital sampler acts as a filter to eliminate any false trips that are created by $V_{CC}$ noises. The digital sampler runs on an internal 32KHz oscillator, masking out any Voltage Comparator output that is less than 3 oscillator clock cycles in duration.

If the external voltage reference is selected, an external resistor voltage divider is used to provide the desired voltage input level that is compared with the internal bandgap reference voltage of 1.29V. The voltage divider is shown in Figure 32 where Vmon is connected to the monitored $V_{CC}$ supply. A typical application would be R2 is 10K ohm and Vmon is 4.75V. The value of R1 is calculated as follows:

$$Vtp = Vmon \times (R2 /( R1 + R2))$$
$$R1 = (4.75V \times 10K)/1.29V - 10K = 26.8K$$

An internal reset is generated when Vmon drops below 4.75V.

### *Figure 32.  Voltage Divider Circuit for Vtp*
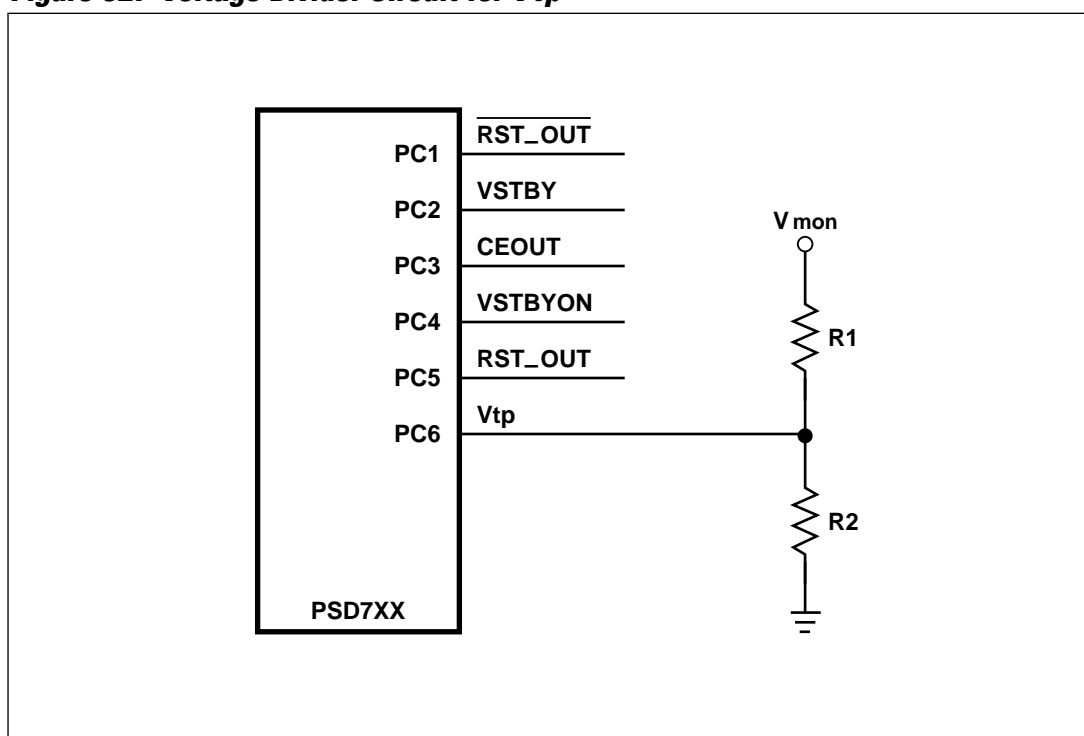
## *Supervisory Function (cont.)*

### *The Power Monitor (cont.)*

The configuration options of the Voltage Comparator provided in the PSDsoft Design Tool are:

❏ Reference voltage source
❏ Internal reference voltage level
❏ Digital Sampler
❏ Voltage Comparator disable

The internal Vtp level selections are shown in Table 38. Two $V_{CC}$ power supply options are available: $V_{CC}$ ± 5% or $V_{CC}$ ± 10%. Depending on the selected $V_{CC}$ power supply option, a fixed Vtp value is provided.

### *Table 38.  Internal Vtp Selection*

| | | Vtp Range | | |
|---|---|---|---|---|
| *Device* | *$V_{CC}$ Power* | *Min.* | *Typical* | *Max.* |
| PSD7XXS5 | 5V ± 5%<br>5V ± 10% | 4.47<br>4.08 | 4.61<br>4.29 | 4.75<br>4.50 |

### *Programmable Watchdog Timer*

The WatchDog Timer consists of a retriggerable 9 bit counter. Once enabled, it starts counting down from an initial value that is specified by the user in the PSDSoft Design Tool. A WatchDog timeout is generated when the count reaches zero. The timeout output is connected to the PPLD and the internal reset pulse generator.

The WatchDog Timer is enabled and controlled by the internal reset and the PPLD outputs:

❏ *Internal Reset*
The WatchDog Timer starts to count immediately after the trailing edge on the extended reset (ERESET) pulse if it is enabled in the PSDsoft design tool.

❏ *PPLD Outputs*
**WDOG_EN** – If the WDOG_EN signal is defined in PSDabel, the Watchdog Timer starts counting only after WDOG_EN generates a high pulse. This signal can be defined in terms of the microcontroller address and the write signal. Writing to this address by the microcontroller will enable the Watchdog Timer. The WDOG_EN signals can be activated only after the extended reset (ERESET) expires.

**WDOG_CLR** – This PPLD output signal re-loads and re-triggers the Watchdog Timer. This signal is used to clear the WatchDog before a timeout is reached, and can be defined in terms of the microcontroller address and the write signal. Writing to this address by the microcontroller will clear the WatchDog.

*Supervisory Function*
*(cont.)*

### Watchdog Timeout Output

Once enabled, the Watchdog Timer counts down using the selected clock rate. It is re-loaded by the PPLD output WDOG_CLR or internal reset. If the WatchDog is not re-loaded in the time period specified in the PSDsoft Design Tool, the WatchDog times out and generates the WDOG_RST signal to the Reset Generator and WDOG_ON to the PPLD. The WDOG_ON signal can be used as a GPLD output to generate an interrupt to the microcontroller.

The WDOG_RST signal can create an internal reset pulse and activate the RST_OUT pins. The pulse width of the RST_OUT and WDOG_ON output is controlled by the Pulse Generator.

### Watchdog Timer in Power-Down Mode

When the PSD7XX enters into power down mode, the WatchDog Timer continues to count and the operation is not affected. The RST_OUT and PPLD are still fully functional.

The PSD7XX consumes considerably less power in the power-down mode if the internal oscillator is selected as the WatchDog clock source instead of CLKIN.

### Battery Backup

The PC2 (VSTBY) pin is the input for an external battery backup voltage for the onboard SRAM. As $V_{CC}$ falls below the value of VSTBY, an automatic internal power switchover occurs which connects the external battery power to the onboard SRAM. The minimum SRAM data retention voltage is 2.0V and the standby current is typically 0.5μA.

At switchover, the PC3 (CEOUT) chip select pin is automatically forced inactive and the PC4 (VSTBYON) pin is driven active.

CEOUT can be defined in PSDsoft as a chip select for an external battery backup SRAM, FLASH, or EEPROM. During normal operation, CEOUT is driven directly by the output of a Micro⇔cell (Mcell3) to select or deselect the memory device. In battery backup mode, CEOUT is driven high automatically to deselect the memory device. This ensures minimal power consumption (external battery backup SRAM) and protects against inadvertent writes during standby mode.

VSTBYON is an external indication that the PSD has switched to standby power mode. It can be used at the designer's discretion.

*Supervisory*
*Function*
*(cont.)*

**Figure 33.  Supervisory Functions**



The figure above shows optional usage of the supervisory functions. These features are included in this diagram: reset input debounce, external trip voltage configuration, external nonvolatile writable memory, and external standby power source.
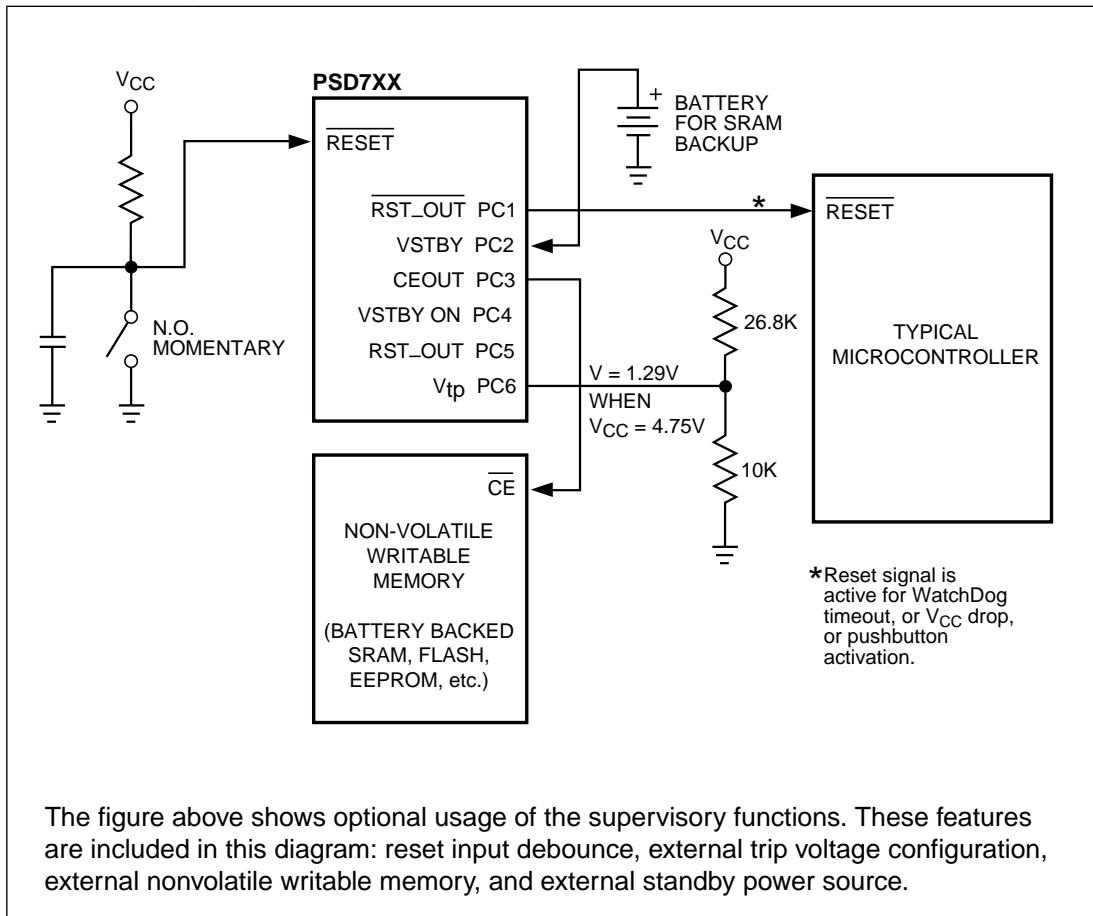
### Clock Source and Frequency Selection

With the exception of the Digital Sampler which has a dedicated 32KHz internal oscillator, all other Supervisory circuitry can run on either the 2KHz internal oscillator or the external CLKIN input.

Table 39 shows the available clock sources and clock inputs to the different circuitry. Based on the selected clock source, the PSDsoft Design Tool provides the user with programmable WatchDog timeout periods and reset pulse widths.

**Table 39.  Clock Sources**

| Clock Source | Reset Debouncer Clock | WatchDog Timer Clock | | Pulse Generator Clock | |
|---|---|---|---|---|---|
| | Frequency | Frequency | Timeout Periods | Frequency | Pulse Width (ms) |
| Internal Oscillator 2KHz | 2KHz/16 | 2KHz or 2KHz/256 | From 0.5ms to 63.875s (0.5ms increment) | 2KHz/2 | 8,16,32,64, 128,256,512 |
| External Clock CLKIN | CLKIN/128K | CLKIN/8K or CLKIN/2M | Depends on CLKIN Frequency | CLKIN/16K | Depends on CLKIN Frequency |

*Supervisory Function (cont.)*

### Status Register

The PSD7XX is able to generate a reset to the microcontroller from three different sources: the WatchDog Timer, the Voltage Comparator and the Push Button reset input. In order to determine which source causes the reset, the microcontroller needs to read the Status Register. After the source of reset is identified, the microcontroller writes to the Reset_Clr Register to clear the reset bits in the Status Register.

### Table 40

| Status Register<br>Address    :CSIOP + D8h<br>            :CSIOP + D9h (Motorola 16 bit) | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| NA | Vext_en | Vtp2 | Vtp1 | Vtp0 | Wdog RST | RST_IN RST | Vtp Rst |

### Bit definitions:

**Vtp RST**

0 = $V_{CC}$ is above Vtp

1 =  A Reset pulse was generated when $V_{CC}$ level had dropped below  Vtp.

**RST_IN**

0 =  RSTIN pin is driven high.

1 =  A Reset pulse was generated when RSTIN pin had been driven low.

**Wdog RST**

0 = No WatchDog reset occurred.

1 = A Reset pulse was generated when the WatchDog Timer expired

**Vtp<2:0> :**

Indicates the selected internal threshold voltage reference level. A Vtp reset is issued whenver $V_{CC}$ stays below the selected reference level.

            0,0,0 – Vtpref = 4.61v
            0,0,1 – Vtpref = 2.57v
            0,1,0 – Vtpref = 2.76v
            0,1,1 – Vtpref = 2.83v
            1,0,0 – Vtpref = 3.03v
            1,0,1 – Vtpref = Not used
            1,1,0 – Vtpref = 4.29v
            1,1,1 – Vtpref = 0, no trip point.

**Vext_en:**

0 –  Select an internal Vtp reference level from the above table.

1 –  Enable PC6 pin to serve as an external Vtp input pin. A Vtp reset is issued whenever $V_{CC}$ stays below PC6 reference voltage level.

| Reset_Clr Register<br>Address    :CSIOP + D6h<br>            :CSIOP + D7h (Motorola 16 bit) |
|---|

Writing 00h to this register clears the reset bits in the Status Register.

## *Supervisory Function (cont.)*

### *Supervisory Diagnostic Registers*

The Supervisory Function has four read-only registers that provide additional Supervisory and WatchDog Timer status for debugging purposes. The contents of the registers are described in the following tables.

### *Sup-Pins (read only)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|----------|------------|------------|---------|---------|
| Cen_resf | CEout | Stby | Vstby_on | Cresb <1> | Cresb <0> | RST_En | Deb_En |

**Deb_En**

0 = RSTIN  pin  has no input filter.
1 = RSTIN  pin is using a debounce filter.

**RST_En**

0 = PC5 pin serves as an active-high reset output.
1 = PC5 pin doesn't serve as an active-high reset output.

**Cresb<1:0>**

0,0 = PC1 pin serves as an active-low, CMOS reset output.
0,1 = PC1 pin  serves as an active-low, open-drain reset output.
1,0 = PC1 pin doesn't serve as an active-low reset output.
1,1 = Reserved

**Vstby_on**

0 = PC4 pin serves as a battery backup mode indicator (high when Vstby > Vcc).
1 = PC4 is not used as a battery backup indicator.

**VStby**

0 = PC2 pin serves as a battery backup input.
1 = PC2 is not used as a battery backup input.

**Ceout**

0 = PC3 pin serves as an external memory select, backed-up by the battery input.
1 = PC3 is not used as a battery-backed, external memory select.

**Cen_resf**

0 = Bypass the Vtp reset digital sampler.
1 = Vtp reset  is using the digital sampler.

## *Supervisory Function (cont.)*

## *WDRST_Stat (read only)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| * | RST_On | Crst2pld | Wdog_ enable | En_ Wdck | Wdog On | Wd2_ res | Wpt_ pwr |

**Wpt_pwr**

0 = Watchdog is enabled  by the En_Wdog PT only.
1 = The Watchdog starts counting following reset.

**Wd2_res**

0 = Watchdog  can't issue a reset pulse.
1 = Watchdog issues a reset pulse upon completion of its count.

**Wdog_on**

0 = Watchdog count hasn't expired.
1 = Watchdog count has expired.

**En_WdCk**

0 = Watchdog counter is disabled.
1 = Watchdog counter is enabled.

**Wdog_enable**

0 = En_Wdog PT hasn't been activated yet.
1 = En_Wdog PT has already been activated, Watchdog is enabled.

**Crst2pld**

0 = The GRESET serves as the reset input of the GPLD.
1 = The ERESET serves as the reset input of the GPLD.

**RST_On**

0 = Reset is not active.
1 = The extended Reset pulse is on.

*Supervisory Function*
*(cont.)*

### WD-timeout1 (read only)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WdTmo<7> | WdTmo<6> | WdTmo<5> | WdTmo<4> | WdTmo<3> | WdTmo<2> | WdTmo<1> | WdTmo<0> |

### WDRST-Var (read only)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WD_Rst<2> | Wd_Rst<1> | Wd_Rst<0> | * | Wclk_ src<1> | Wclk_ src<0> | * | WdTmo<8> |

**WdTmo<8:0>**

Current Watchdog count. Must be read twice. Only when  two successive reads fetch identical count-values, the count is correct.

    WdTmo<8> is the most significant bit,
    WdTmo<0> is the least significant bit.

**Wclk_src<1:0>**

Determines the Watchdog clock source.
    0,0 = Embedded 2KHz oscillator.
    0,1 = Embedded  8Hz oscillator.
    1,0 = CLKin frequency / 8192  (= CLKin / 8K).
    1,1 = CLKin frequency / 2,097,152 (CLKin / 2M).

**Wd_Rst<2:0>**

Defines the Watchdog  pulse length or reset pulse extension.
    **With Wclk_src<1> = 0:**
    0,0,0 = 8 ms
    0,0,1 = 16 ms
    0,1,0 = 32 ms
    0,1,1 = 64 ms
    1,0,0 = 128 ms
    1,0,1 = 256 ms
    1,1,0 = 512 ms
    1,1,1 = 1024 ms (~ 1sec)
    **With Wclk_src<1> = 1:**
    0,0,0 = {   8 x [16384 /CLKin(hz)]} sec
    0,0,1 = {  16 x [16384 /CLKin(hz)]} sec
    0,1,0 = {  32 x [16384 /CLKin(hz)]} sec
    0,1,1 = {  64 x [16384 /CLKin(hz)]} sec
    1,0,0 = { 128 x [16384 /CLKin(hz)]} sec
    1,0,1 = { 256 x [16384 /CLKin(hz)]} sec
    1,1,0 = { 512 x [16384 /CLKin(hz)]} sec
    1,1,1 = {1024 x [16384 /CLKin(hz)]} sec

**NOTE:**   The Supervisory functions have no control/configuration registers that are accessible during run-time. All Supervisory function control/configuration is done using PSDsoft.

### Absolute Maximum Ratings

| Symbol | Parameter | Condition | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
| T$_{STG}$ | Storage Temperature | CLDCC | − 65 | + 150 | °C |
| | | PLDCC | − 65 | + 125 | °C |
| | Operating Temperature | Commercial | 0 | + 70 | °C |
| | | Industrial | − 40 | + 85 | °C |
| | Voltage on any Pin | With Respect to GND | − 0.6 | + 7 | V |
| V$_{PP}$ | Programming Supply Voltage | With Respect to GND | − 0.6 | + 14 | V |
| V$_{CC}$ | Supply Voltage | With Respect to GND | − 0.6 | + 7 | V |
| | ESD Protection | | >2000 | | V |

**NOTE:** Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

### Operating Range

| Range | Temperature | V$_{CC}$ | V$_{CC}$ Tolerance | | |
|-------|-------------|----------|--------|-----|-----|
| | | | -70 | -90 | -15 |
| Commercial | 0° C to +70°C | + 5 V | ± 10% | | ± 10% |
| Industrial | −40° C to +85°C | + 5 V | | ± 10% | ± 10% |

### Recommended Operating Conditions

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| V$_{CC}$ | Supply Voltage | All Speeds | 4.5 | 5 | 5.5 | V |

## AC/DC Parameters

The following tables describe the AD/DC parameters of the PSD7XX family:

❏ DC Electrical Specification

❏ AC Timing Specification
- PLD Timing
  - Combinatorial Timing
  - Synchronous Clock Mode
  - Asynchronous Clock Mode
  - Input Micro⇔Cell Timing
- Microcontroller Timing
  - Read Timing
  - Write Timing
  - Peripheral Mode Timing
  - Power Down and Reset Timing

Following are some issues concerning the parameters presented:

❏ In the DC specification the Supply Current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD7XX is in each mode. Also the supply power is considerably different if the EPROM_CMISER is "ON".

❏ The AC power component gives the PLD, EPROM, and SRAM mA/MHz specification.

❏ In the MCU timing specification add the required time delay when EPROM_CMISER is "ON".

## DC Characteristics (5 V ± 10% Versions)

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|--------|-----------|--|------------|-----|-----|-----|------|
| $V_{CC}$ | Supply Voltage | | All Speeds | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High Level Input Voltage | | 4.5 V < $V_{CC}$ < 5.5 V | 2 | | $V_{CC}$ +.5 | V |
| $V_{IL}$ | Low Level Input Voltage | | 4.5 V < $V_{CC}$ < 5.5 V | −0.5 | | 0.8 | V |
| $V_{IH1}$ | Reset High Level Input Voltage | | (Note 1) | .8 $V_{CC}$ | | $V_{CC}$ +.5 | V |
| $V_{IH2}$ | $V_{TP}$ Pin | | | | | $V_{CC}$ +.5 | V |
| $V_{IL1}$ | Reset Low Level Input Voltage | | (Note 1) | −.5 | | .2 $V_{CC}$ −.1 | V |
| $V_{HYS}$ | Reset Pin Hysteresis | | | 0.3 | | | V |
| $V_{TP}$ | Power Supply Trip Point | | 5% $V_{CC}$ = 5V, $V_{tp}$(2:0) = 0 | 4.47 | 4.61 | 4.75 | V |
| | | | 10% $V_{CC}$ = 5V, $V_{tp}$(2:0) = 6 | 4.08 | 4.29 | 4.50 | V |
| | | | $V_{tp}$(2:0) = 7, No Power On Reset | | 0 | | V |
| $V_{ETP}$ | External Trip Point (PC6) | | | 1.23 | 1.29 | 1.35 | V |
| $V_{OL}$ | Output Low Voltage | | $I_{OL}$ = 20 µA, $V_{CC}$ = 4.5 V | | 0.01 | 0.1 | V |
| | | | $I_{OL}$ = 8 mA, $V_{CC}$ = 4.5 V | | 0.15 | 0.45 | V |
| $V_{OH}$ | Output High Voltage Except VSTBYON, CEOUT | | $I_{OH}$ = −20 µA, $V_{CC}$ = 4.5 V | 4.4 | 4.49 | | V |
| | | | $I_{OH}$ = −2 mA, $V_{CC}$ = 4.5 V | 2.4 | 3.9 | | V |
| $V_{OH1}$ | Output High Voltage VSTBYON, CEOUT | | $I_{OH1}$ = 1 µA | | | $V_{SBY}$ −0.5 | |
| $V_{SBY}$ | SRAM Standby Voltage | | | 2.0 | | $V_{CC}$ | V |
| $I_{SBY}$ | SRAM Standby Current | | $V_{CC}$ = 0 V | | 0.5 | 1 | µA |
| $I_{IDLE}$ | Idle Current ($V_{STBY}$ Pin) | | $V_{CC}$ > $V_{SBY}$ | −0.1 | | 0.1 | µA |
| $V_{DF}$ | SRAM Data Retention Voltage | | Only on $V_{STBY}$ | 2 | | | V |
| $I_{SB}$ | Standby Supply Current | Power Down Mode | $\overline{CSI}$ >$V_{CC}$ −.3 V (Note 2) | | 50 | 100 | µA |
| | | Sleep Mode | $\overline{CSI}$ >$V_{CC}$ −.3 V (Note 3) | | 25 | 50 | µA |
| $I_{LI}$ | Input Leakage Current | | $V_{SS}$ < $V_{IN}$ > $V_{CC}$ | −1 | ±.1 | 1 | µA |
| $I_{LO}$ | Output Leakage Current | | .45 < $V_{IN}$ > $V_{CC}$ | −10 | ±5 | 10 | µA |
| $I_{CC}$ (DC) (Note 4) | Operating Supply Current | PLD Only | f = 0 MHz | | 400 | 700 | µA/PT |
| | | EPROM Adder | CMiser = ON and Not Selected | | 0 | 0 | mA |
| | | | CMiser = ON and EPROM Selected (x8 Data Bus) | | 10 | 15 | mA |
| | | | CMiser = ON and EPROM Selected (x16 Data Bus) | | 15 | 20 | mA |
| | | | CMiser = OFF | | 15 | 20 | mA |
| | | SRAM Adder | SRAM Not Selected | | 0 | 0 | mA |
| | | | CMiser = ON, SRAM Selected (x8 Data Bus) | | 25 | 40 | mA |
| | | | CMiser = ON, SRAM Selected (x16 Data Bus) | | 30 | 45 | mA |
| $I_{CC}$ (AC) | PLD | | | | 2 | 3 | mA/MHz |
| | EPROM or SRAM | | | | 2 | | mA/MHz |

NOTES: 1. Reset input has hysteresis. $V_{IL1}$ is valid at or below .2$V_{CC}$ −.1. $V_{IH1}$ is valid at or above .8$V_{CC}$.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. $I_{OUT}$ = 0 mA.

*PSD7XX
AC/DC
Parameters –
GPLD and ECSPLD
Timing*

(5V ± 10% Versions)

## GPLD and ECSPLD Combinatorial Timing   (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 Min | -70 Max | -90 Min | -90 Max | -15 Min | -15 Max | PT Aloc | Slew Rate | Unit |
|--------|-----------|------------|------|------|------|------|------|------|---------|-----------|------|
| $t_{PD1}$ | ECSPLD Input Pin to ECSPLD Combinatorial Output | (Notes 1 & 2) | | 18 | | 20 | | 24 | | Add 3 | ns |
| $t_{PD2}$ | GPLD Input Pin/Feedback to GPLD Combinatorial Output Port C | (Note 2a) | | 25 | | 28 | | 32 | Add 2 | | ns |
| $t_{PD3}$ | GPLD Input Pin/Feedback to GPLD Combinatorial Output Port A or B | (Note 2a) | | 27 | | 30 | | 34 | | | ns |
| $t_{EA}$ | GPLD Input to ECSPLD Output Enable | (Notes 2 & 2a) | | 23 | | 25 | | 29 | | Add 3 | ns |
| | GPLD Input to GPLD Output Enable | (Notes 2a & 2b) | | 26 | | 28 | | 32 | | | ns |
| $t_{ER}$ | GPLD Input to ECSPLD Output Disable | (Notes 2 & 2a) | | 23 | | 25 | | 29 | | Add 3 | ns |
| | GPLD Input to GPLD Output Disable | (Notes 2a & 2b) | | 26 | | 28 | | 32 | | | ns |
| $t_{ARP}$ | GPLD Register Clear or Preset Delay | (Notes 2a & 2b) | | 26 | | 29 | | 33 | | | ns |
| $t_{ARPW}$ | GPLD Register Clear or Preset Pulse Width | (Notes 2a & 2b) | 20 | | 25 | | 29 | | | | ns |
| $t_{ARD}$ | GPLD Array Delay | Any Micro⇔cell | | 16 | | 18 | | 22 | Add 2 | | ns |

**NOTES:** 1.  ECSPLD Input pins are A(0:15), PGR(0:3), CNTL(0:2), PDN.
2.  ECSPLD Outputs are PA(0:3), PB(0:3), PD(0:2).
2a.  GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN, RESET, WDOG_ON and WCLK.
2b.  GPLD Outputs are PA(4:7), PB(4:7), PC(0:7).

**PSD7XX AC/DC Parameters – GPLD and ECSPLD Timing**

(5V ± 10% Versions)

**GPLD Micro⇔cell Synchronous Clock Mode Timing**  (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 Min | -70 Max | -90 Min | -90 Max | -15 Min | -15 Max | PT Aloc | Slew Rate | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Frequency External Feedback | $1/(t_S + t_{CO})$ | | 30.30 | | 27.03 | | 25.00 | | | MHz |
| | Maximum Frequency Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CO} - 10)$ | | 43.48 | | 37.04 | | 31.25 | | | MHz |
| | Maximum Frequency Pipelined Data | $1/(t_{CH} + t_{CL})$ | | 50.00 | | 41.67 | | 35.71 | | | MHz |
| $t_S$ | Input Setup Time | (Notes 2a) | 15 | | 17 | | 20 | | Add 2 | | ns |
| $t_H$ | Input Hold Time | (Notes 2a) | 0 | | 0 | | 0 | | | | ns |
| $t_{CH}$ | Clock High Time | Clock Input | 10 | | 12 | | 15 | | | | ns |
| $t_{CL}$ | Clock Low Time | Clock Input | 10 | | 12 | | 15 | | | | ns |
| $t_{CO}$ | Clock to Output Delay | Clock Input | | 18 | | 20 | | 22 | | | ns |
| $t_{ARD}$ | GPLD Array Delay | Any Micro⇔cell | | 16 | | 18 | | 22 | Add2 | | ns |
| $t_{MIN}$ | Minimum Clock Period | $t_{CH} + t_{CL}$ | 20 | | 24 | | 29 | | | | ns |

**NOTE:** 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN, Reset, WDOG_ON, and WCLK.

2c. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

**PSD7XX AC/DC Parameters – GPLD and ECSPLD Timing**

(5V ± 10% Versions)

## GPLD Micro⇔cell Asynchronous Clock Mode Timing (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 Min | -70 Max | -90 Min | -90 Max | -15 Min | -15 Max | PT Aloc | Slew Rate | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAXA}$ | Maximum Frequency External Feedback | $1/(t_{SA} + t_{COA})$ | | 26.32 | | 25.00 | | 21.74 | | | MHz |
| | Maximum Frequency Internal Feedback ($f_{CNTA}$) | $1/(t_{SA} + t_{COA} -10)$ | | 35.71 | | 33.33 | | 27.78 | | | MHz |
| | Maximum Frequency Pipelined Data | $1/(t_{CH} + t_{CL})$ | | 41.67 | | 41.67 | | 35.71 | | | MHz |
| $t_{SA}$ | Input Setup Time | (Note 2a) | 8 | | 8 | | 12 | | Add 2 | | ns |
| $t_{HA}$ | Input Hold Time | (Note 2a) | 8 | | 8 | | 12 | | | | ns |
| $t_{CHA}$ | Clock Input High Time | (Note 2a) | 12 | | 12 | | 15 | | | | ns |
| $t_{CLA}$ | Clock Input Low Time | (Note 2a) | 12 | | 12 | | 15 | | | | ns |
| $t_{COA}$ | Clock to Output Delay | (Note 2a) | | 30 | | 32 | | 37 | | | ns |
| $t_{ARDA}$ | GPLD Array Delay | Any Micro⇔cell | | 16 | | 18 | | 22 | Add 2 | | ns |
| $t_{MINA}$ | Minimum Clock Period | $1/f_{CNTA}$ | 28 | | 30 | | 43 | | | | ns |

**NOTE:** 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN, Reset, WDOG_ON, and WCLK.

2c. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

## PSD7XX AC/DC Parameters – GPLD and ECSPLD Timing
(5V ± 10% Versions)

### Input Micro⇔cell Timing (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 | | -90 | | -15 | | PT Aloc | Unit |
|--------|-----------|------------|-----|-----|-----|-----|-----|-----|---------|------|
| | | | Min | Max | Min | Max | Min | Max | | |
| $t_{IS}$ | Input Setup Time | (Note 2d) | 0 | | 0 | | 0 | | | ns |
| $t_{IH}$ | Input Hold Time | (Note 2d) | 20 | | 22 | | 26 | | | ns |
| $t_{INH}$ | NIB Input High Time | (Note 2d) | 12 | | 14 | | 18 | | | ns |
| $t_{INL}$ | NIB Input Low Time | (Note 2d) | 12 | | 14 | | 18 | | | ns |
| $t_{INO}$ | NIB Input to Combinatorial Delay | (Note 2d) | | 46 | | 51 | | 59 | Add 2 | ns |

**NOTE:** 2d. Inputs from Port A, B and C relative to register/latch clock from the PLD. ALE latch timings refer to $t_{AVLX}$ and $t_{LXAX}$.

*Microcontroller Interface – AC/DC Parameters*

(5V ± 10% Versions)

### Explanation of AC Symbols for PLD Timing.

**Example:** $t_{AVLX}$ – Time from Address Valid to ALE Invalid.

### Signal Letters

**A** – Address Input
**C** – CEout Output
**D** – Input Data
**E** – E Input
**G** – Internal WDOG_ON signal
**I** – Interrupt Input
**L** – ALE Input
**N** – Reset Input or Output
**P** – Port Signal Output
**Q** – Output Data
**R** – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ Inputs
**S** – Chip Select Input
**T** – R/$\overline{W}$ Input
**W** – Internal PDN Signal
**B** – Vstby Output
M – Output Micro⇔Cell

### Signal Behavior

**t** – Time
**L** – Logic Level Low or ALE
**H** – Logic Level High
**V** – Valid
**X** – No Longer a Valid Logic Level
**Z** – Float
**PW** – Pulse Width

## Microcontroller Interface – AC/DC Parameters

(5 V ± 10% Versions)

### Read Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 Min | -70 Max | -90 Min | -90 Max | -15 Min | -15 Max | CMiser ON | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{LVLX}$ | ALE or AS Pulse Width | | 18 | | 20 | | 28 | | | ns |
| $t_{AVLX}$ | Address Setup Time | (Note 4) | 5 | | 6 | | 10 | | | ns |
| $t_{LXAX}$ | Address Hold Time | (Note 4) | 7 | | 8 | | 11 | | | ns |
| $t_{AVQV}$ | Address Valid to Data Valid | (Note 4) | | 70 | | 90 | | 150 | Add 10 | ns |
| $t_{SLQV}$ | $\overline{CS}$ Valid to Data Valid | | | 80 | | 100 | | 150 | Add 10 | ns |
| $t_{RLQV}$ | $\overline{RD}$ to Data Valid 8/16-Bit Bus | (Note 3) | | 20 | | 32 | | 40 | | ns |
| | $\overline{RD}$ to Data Valid 8-Bit Bus, 8031, 80251 Separate Mode | (Note 3a) | | 32 | | 38 | | 45 | | ns |
| $t_{RHQX}$ | $\overline{RD}$ Data Hold Time | (Note 3) | 0 | | 0 | | 0 | | | ns |
| $t_{RLRH}$ | $\overline{RD}$ Pulse Width | (Note 3) | 30 | | 32 | | 38 | | | ns |
| $t_{RHQZ}$ | $\overline{RD}$ to Data High-Z | (Note 3) | | 22 | | 25 | | 33 | | ns |
| $t_{EHEL}$ | E Pulse Width | | 30 | | 32 | | 38 | | | ns |
| $t_{THEH}$ | R/$\overline{W}$ Setup Time to Enable | | 8 | | 10 | | 18 | | | ns |
| $t_{ELTL}$ | R/$\overline{W}$ Hold Time After Enable | | 0 | | 0 | | 0 | | | ns |
| $t_{AVPV}$ | Address Input Valid to Address Output Delay | In 16-Bit Bus Mode (Note 5) | | 20 | | 30 | | 38 | | ns |
| | | In 8-Bit Bus Mode (Note 5) | | 22 | | 32 | | 48 | | ns |

NOTES:
3. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{PSEN}$ (in 8031 combined mode) signals.
3a. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 separate mode.
4. Any input used to select an internal PSD7XX function.
5. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

## Microcontroller Interface – AC/DC Parameters

(5 V ± 10% Versions)

### Write Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 Min | -70 Max | -90 Min | -90 Max | -15 Min | -15 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| t$_{LVLX}$ | ALE or AS Pulse Width | | 18 | | 20 | | 28 | | ns |
| t$_{AVLX}$ | Address Setup Time | (Note 4) | 5 | | 6 | | 10 | | ns |
| t$_{LXAX}$ | Address Hold Time | (Note 4) | 7 | | 8 | | 11 | | ns |
| t$_{AVWL}$ | Address Valid to Leading Edge of $\overline{WR}$ | (Notes 4 and 6) | 18 | | 20 | | 30 | | ns |
| t$_{SLWL}$ | $\overline{CS}$ Valid to Leading Edge or $\overline{WR}$ | (Note 6) | 22 | | 25 | | 35 | | ns |
| t$_{DVWH}$ | $\overline{WR}$ Data Setup Time | (Note 6) | 12 | | 15 | | 22 | | ns |
| t$_{WHDX}$ | $\overline{WR}$ Data Hold Time | (Note 6) | 5 | | 5 | | 5 | | ns |
| t$_{WLWH}$ | $\overline{WR}$ Pulse Width | (Note 6) | 18 | | 20 | | 28 | | ns |
| t$_{WHAX}$ | Trailing Edge of $\overline{WR}$ to Address Invalid | (Note 6) | 0 | | 0 | | 0 | | ns |
| t$_{WHPV}$ | Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register | (Note 6) | | 25 | | 30 | | 38 | ns |
| t$_{WHMV}$ | $\overline{WR}$ Valid to Port Output Valid Using Micro⇔Cell Register Preset/Clear | (Notes 6 and 6a) | | 25 | | 30 | | 38 | ns |
| t$_{DVMV}$ | Data Valid to Port Output Valid Using Micro⇔Cell Register Preset/Clear | (Notes 6 and 6b) | | 25 | | 30 | | 38 | ns |
| t$_{AVPV}$ | Address Input Valid to Address Output Delay | In 16-Bit Bus Mode (Note 5) | | 20 | | 30 | | 38 | ns |
| | | In 8-Bit Bus Mode (Note 5) | | 22 | | 32 | | 48 | ns |

**NOTE:** 6.  $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WRH}$ signals.
6a.  Assuming data is stable before active write signal.
6b.  Assuming write is active before data becomes valid.

## Microcontroller Interface – AC/DC Parameters
(5 V ± 10% Versions)

### Port A Peripheral Data Mode Read Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 | | -90 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVQV\,(PA)}$ | Address Valid to Data Valid | (Note 7) | | 45 | | 55 | | 62 | ns |
| $t_{SLQV\,(PA)}$ | $\overline{CS}$ Valid to Data Valid | | | 55 | | 55 | | 62 | ns |
| $t_{RLQV\,(PA)}$ | $\overline{RD}$ to Data Valid | (Notes 3, 8) | | 20 | | 32 | | 40 | ns |
| | $\overline{RD}$ to Data Valid 8031 Mode | | | 32 | | 38 | | 45 | ns |
| $t_{DVQV\,(PA)}$ | Data In to Data Out Valid | | | 22 | | 22 | | 26 | ns |
| $t_{QXRH\,(PA)}$ | $\overline{RD}$ Data Hold Time | (Note 3) | 0 | | 0 | | 0 | | ns |
| $t_{RLRH\,(PA)}$ | $\overline{RD}$ Pulse Width | (Note 3) | 30 | | 32 | | 38 | | ns |
| $t_{RHQZ\,(PA)}$ | $\overline{RD}$ to Data High-Z | (Note 3) | | 20 | | 25 | | 33 | ns |

### Port A Peripheral Data Mode Write Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 | | -90 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{WLQV\,(PA)}$ | $\overline{WR}$ to Data Propagation Delay | (Note 6) | | 25 | | 27 | | 35 | ns |
| $t_{DVQV\,(PA)}$ | Data to Port A Data Propagation Delay | (Note 9) | | 22 | | 22 | | 26 | ns |
| $t_{WHQZ\,(PA)}$ | $\overline{WR}$ Invalid to Port A Tri-State | (Note 6) | | 20 | | 25 | | 33 | ns |

**NOTES:** 7. Any input used to select Port A Data Peripheral Mode.
8. Data is already stable on Port A.
9. Data stable on ADIO pins to data on Port A.

*Microcontroller Interface – AC/DC Parameters*

(5 V ± 10% Versions)

*Power Down Timing* (5 V ± 10%)

| Symbol | Parameter | Conditions | -70 | | -90 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| t$_{LVDV}$ | ALE Access Time from Power Down | | | 100 | | 120 | | 150 | ns |
| t$_{LVDV1}$ | ALE or $\overline{CSI}$ Access Time from Sleep | | | 120 | | 150 | | 200 | ns |
| t$_{PD4}$ | GPLD and FPLD Propagation Delay in Sleep Mode | | | 600 | | 600 | | 600 | ns |
| t$_{PD5}$ | GPLD and FPLD Recovery Time After Sleep Mode | | | 250 | | 250 | | 250 | ns |
| t$_{CLWH}$ | Maximum Delay from APD Enable to Internal PDN Valid Signal | Using CLKIN Input | 15* t$_{CLCL}$ (µs) (Note 10) | | | | | | µs |
| | | Using WatchDog Clock | 15* t$_{WDCLK}$ (µs) | | | | | | µs |

**NOTES:** 10. tCLCL is the CLKIN clock period. See Figure 38.

## Microcontroller Interface – AC/DC Parameters
(5 V ± 10% Versions)

### WatchDog and Internal Oscillator Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PDGL}$ | Propagation Delay from GPLD Input to Clear Internal WDOG_ON | (Note 2a) | $t_{PD3}$ | | | ns |
| $t_{WDPW}$ | WatchDog Clear (CLR_WDOG) and Enable (EN_WDOG) Pulse Width | (Note 2a) | $t_{RLQV}$ | | | ns |
| $f_{OSC}$ | Internal Oscillator Frequency | | 1.2 | 2 | 2.8 | kHz |
| | WatchDog Clock and WCLK Signal Period – CLKIN Short Divisor (CLKIN/8K) | | | $2^{13} * t_{CLCL}$ | | µs |
| | WatchDog Clock and WCLK Signal Period – CLKIN Long Divisor (CLKIN/2M) | | | $2^{21} * t_{CLCL}$ | | µs |
| $t_{WDCLK}$ | WatchDog Clock and WCLK Signal Period – Internal OSC with No Divisor (2KHz) | | | 0.5 | | ms |
| | WatchDog Clock and WCLK Signal Period – Internal OSC with Divisor (2KHz/256) | | | 128 | | ms |
| $t_{WDTMO}$ | WatchDog Timeout Period | WD_TMO = 0,1,2......$2^9$–1 (Note 11) | | WD_TMO * $t_{WDCLK}$ (µs) | | µs |
| $t_{CHGH}$ | WatchDog Clock to Internal WDOG_ON High Delay | | 20 | | 1000 | ns |
| | Internal WDON_ON Active Time Using Internal Oscillator | Pulse Generator Clock = N = 0,1,2,3,4,5,6,7 (Note 11) | | $2^{N+3} * 2/f_{OSC}$ (kHz) | | ms |
| $t_{GHGL}$ | Internal WDON_ON Active Time Using External Clock (CLKIN) | Pulse Generator Clock = N = 0,1,2,3,4,5,6,7 (Note 11) | | $2^{N+3} * 16384 * t_{CLCL}$ | | µs |

**NOTES:** 11. Refer to PSDsoft Report on Timing Parameters $t_{WDTMO}$, $t_{GHGL}$ and $t_{NVNX}$.

## Microcontroller Interface – AC/DC Parameters
(5 V ± 10% Versions)

### $V_{CC}$ and Reset Timing (5 V ± 10%)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NLNH}$ | Reset Input Minimum Active Low Time with Debouncer Enabled — Using Internal Oscillator | | | $48/f_{OSC}$ (kHz) | | ms |
| | Reset Input Minimum Active Low Time with Debouncer Enabled — Using External Clock Input Pin (CLKin) | | | $393.2 * t_{CLCL}$ (µs) | | ms |
| | Reset Input Minimum Active Low Time with Debouncer Disabled | | 150 | | | ns |
| $t_{OPR}$ | Operational PSD after RESET Input Inactive | | | | 100 | ns |
| $t_{NVNX}$ | RST_OUT, RST_OUT Output Active Time Using Internal Oscillator | Pulse Generator Clock = $N = 0,1,2,3,4,5,6,7$ (Note 11) | | $2^{N+3} * 2/f_{OSC}$ (kHz) | | ms |
| | RST_OUT, RST_OUT Output Active Time Using External Clock (CLKIN) | Pulse Generaror Clock= $N = 0,1,2,3,4,5,6,7$ (Note 11) | | $2^{N+3} * 16384 * t_{CLCL}$ (Note 11) | | ms |
| $t_{NLNV}$ | Reset to RST_OUT, RST_OUT Output Valid with Debouncer Enabled | | | | 30 | ms |
| | Reset to RST_OUT, RST_OUT Output Valid with Debouncer Disabled | | | | 100 | ns |
| $t_{VXNV}$ | $V_{CC}$ Fall Detect to RST_OUT, RST_OUT Active with Digital Samplerr | | 40 | 100 | 175 | µs |
| | $V_{CC}$ Fall Detect to RST_OUT, RST_OUT Active without Digital Sampler | | 1 | | 2 | µs |
| $t_{VVNX}$ | $V_{CC}$ Valid to Internal Reset Active with Digital Sampler | | 40 | 100 | 150 | ms |
| | $V_{CC}$ Valid to Internal Reset Active without Digital Sampler | | 1 | | 2 | ns |

**NOTES:** 11. Refer to PSDsoft Report on Timing Parameters $t_{WDTMO}$, $t_{GHGL}$ and $t_{NVNX}$.

## Microcontroller Interface – AC/DC Parameters

(5 V ± 10% Versions)

### CEout Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NVCH}$ | From $V_{CC}$ Fall Detection ($V_{CC}$tp) to CEOUT High with Digital Sampler | Load of 1 µA | 40 | 100 | 175 | µs |
| | From $V_{CC}$ Fall Detection ($V_{CC}$tp) to CEOUT High without Digital Sampler | Load of 1 µA | 1 | | 2 | µs |
| $t_{NXCV}$ | CEout Recovery Time after Power Up Detection ($V_{CC} > V_{CC}$tp) with Digital Sampler | Load of 1 µA | 40 | 100 | 175 | µs |
| | CEout Recovery Time after Power Up Detection ($V_{CC} > V_{CC}$tp) without Digital Sampler | Load of 1 µA | 1 | | 2 | µs |

### Vstbyon Timing  (5 V ± 10%)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{BVBH}$ | Vstby Detection to Vstbyon Output High | | | 1.5 | 2 | µs |
| $t_{BXBL}$ | Vstby Off Detection to Vstbyon Output Low | | | 1.5 | 2 | µs |

## *Figure 34.  Read Timing*



*t_AVLX and t_LXAX are not required for 80C251 in Page Mode or 80C51XA in Burst Mode.
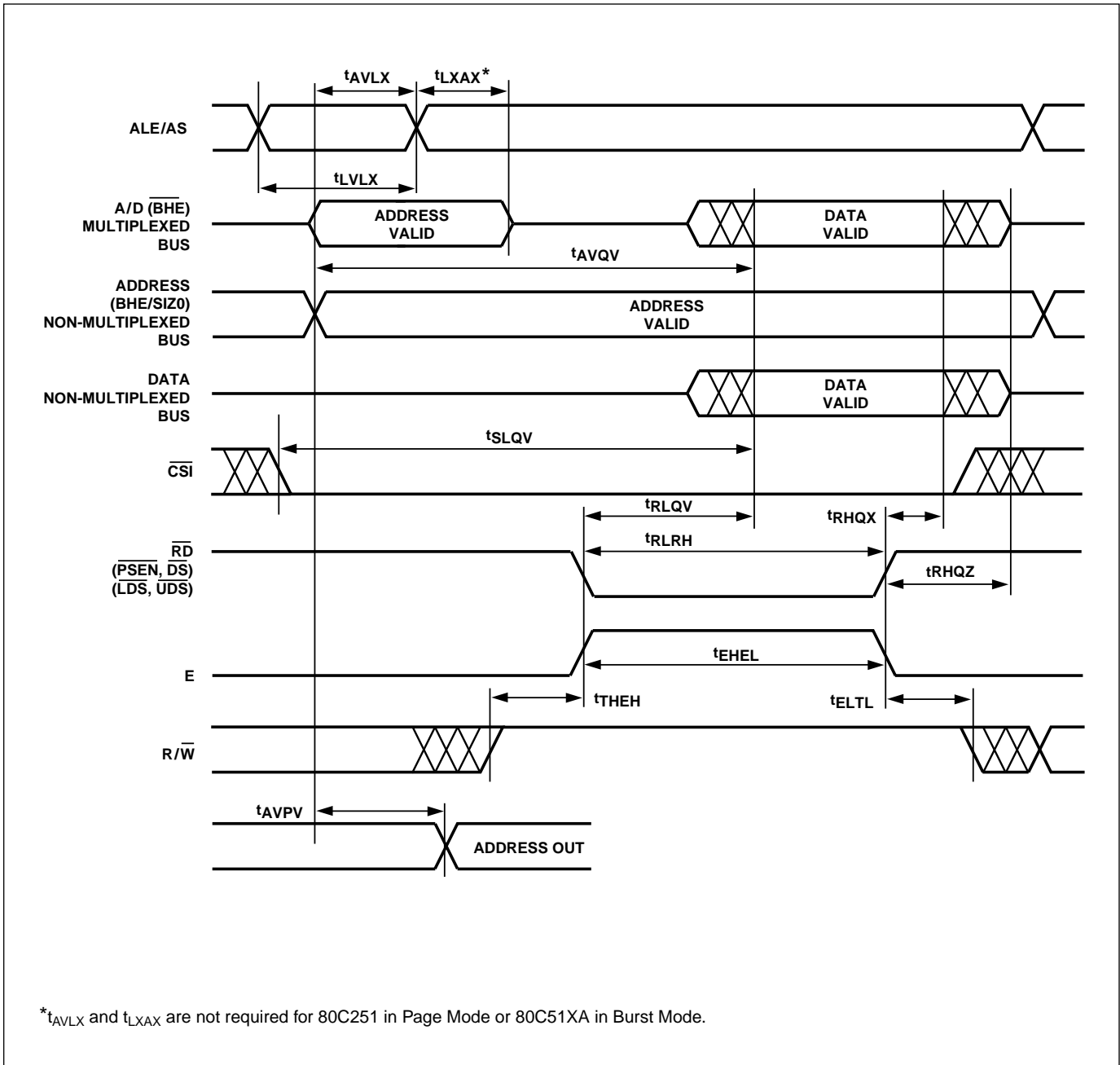
## Figure 35. Write Timing
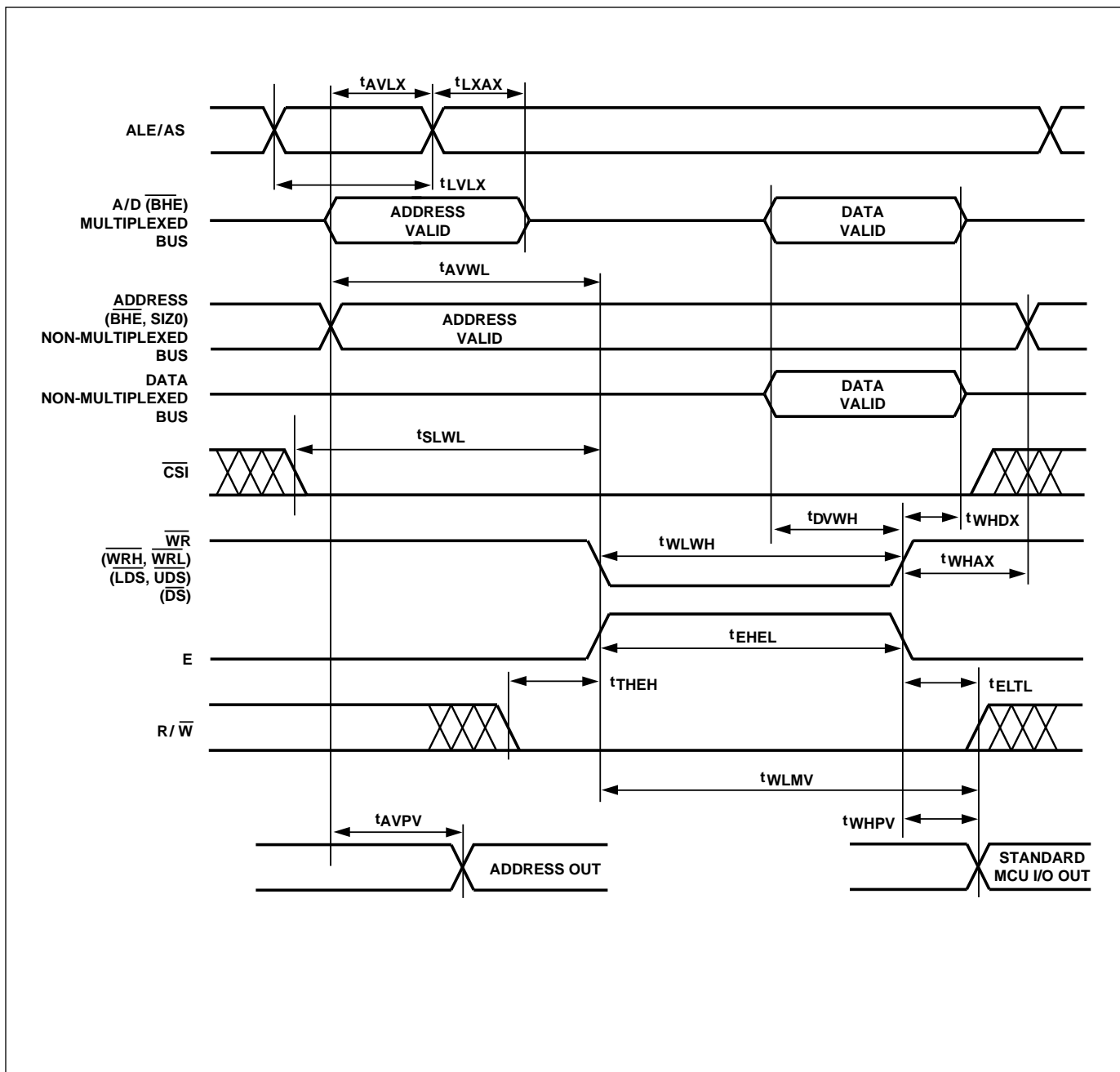
## Figure 36.  Peripheral I/O Read Timing
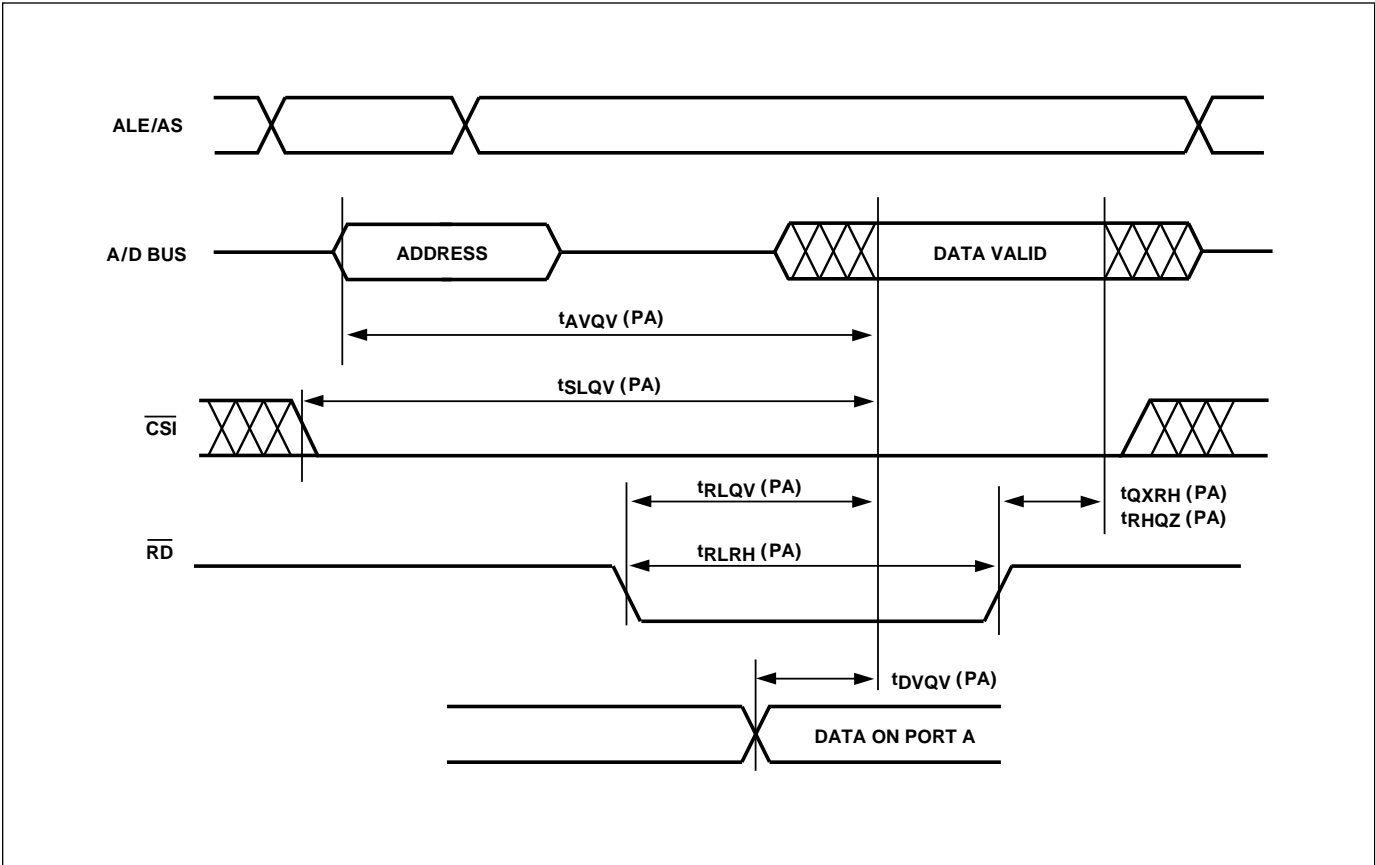


## Figure 37.  Peripheral I/O Write Timing
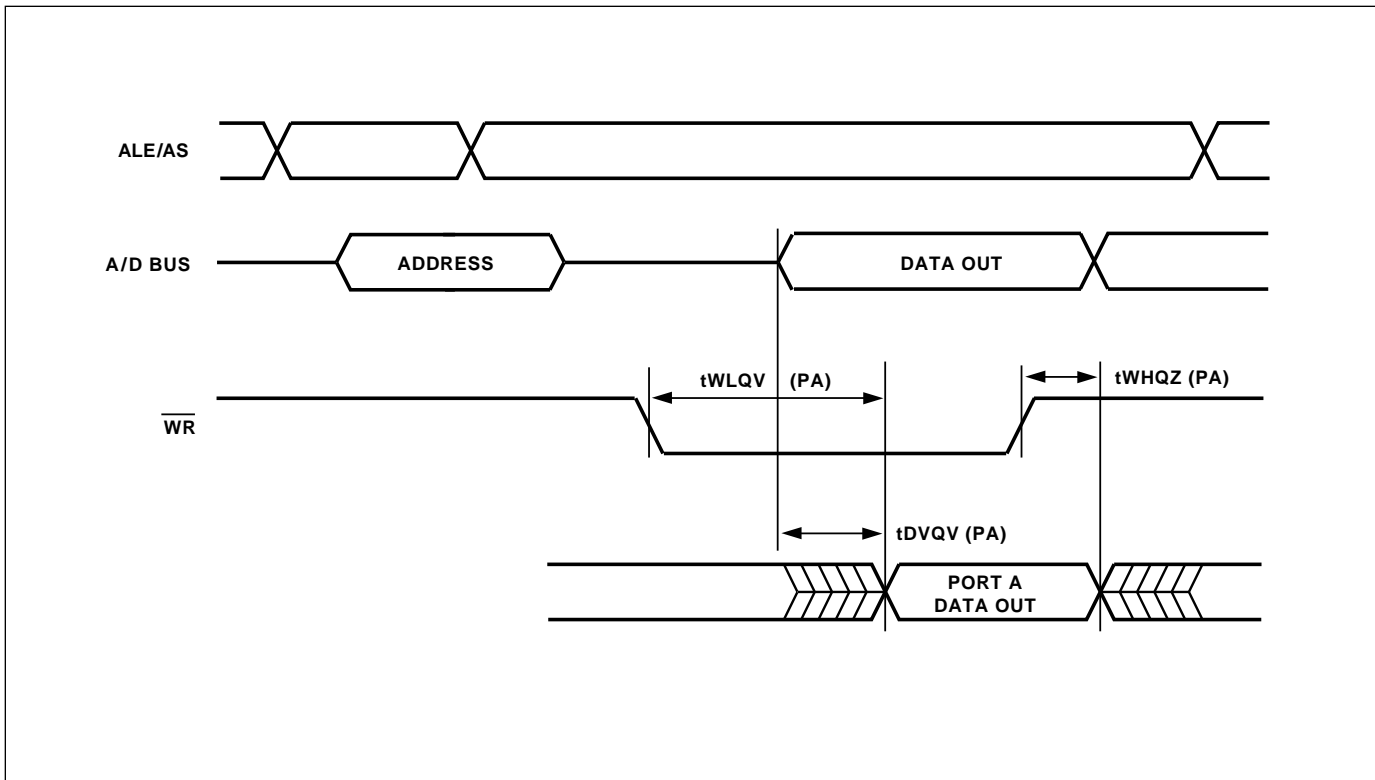
## *Figure 38. Combinatorial Timing – PLD*
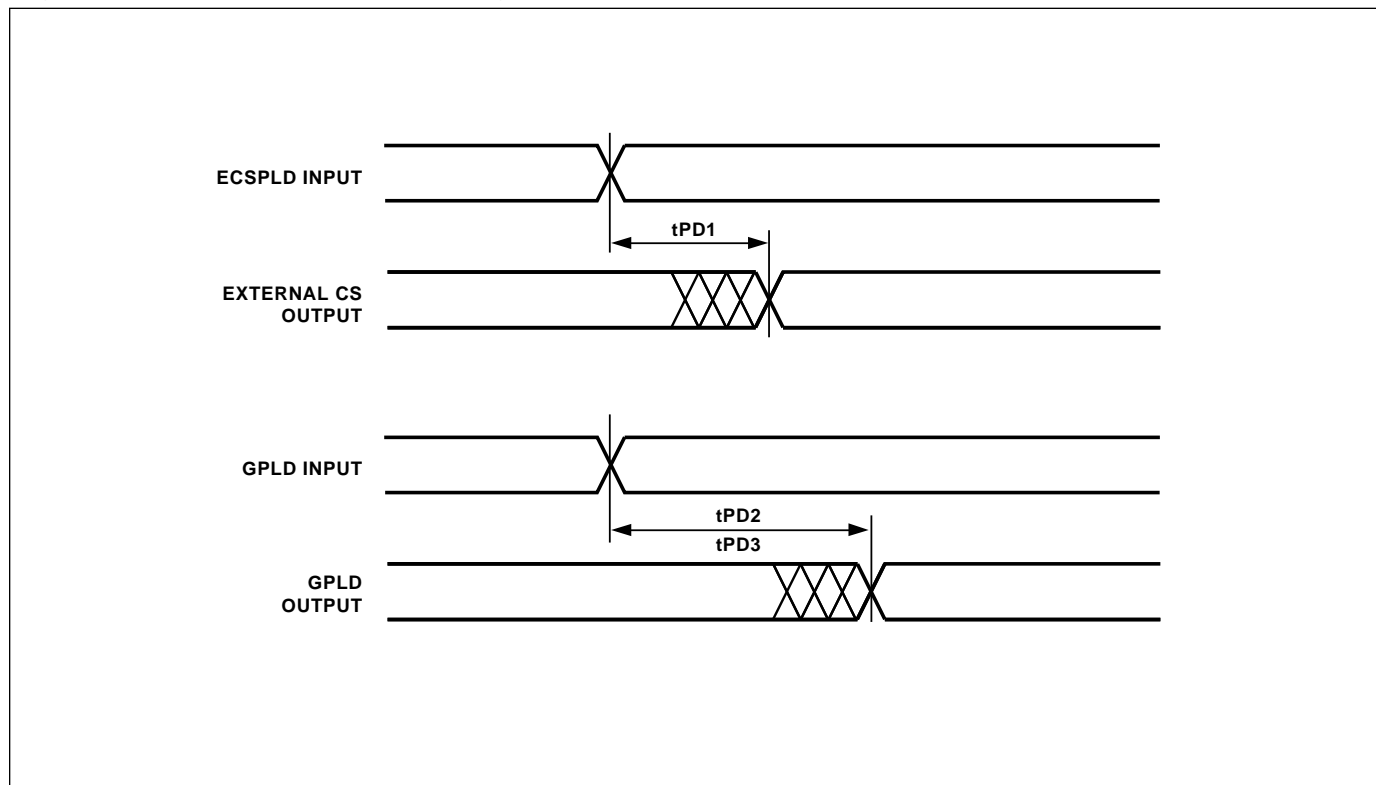


## *Figure 39. Synchronous Clock Mode Timing – PLD*
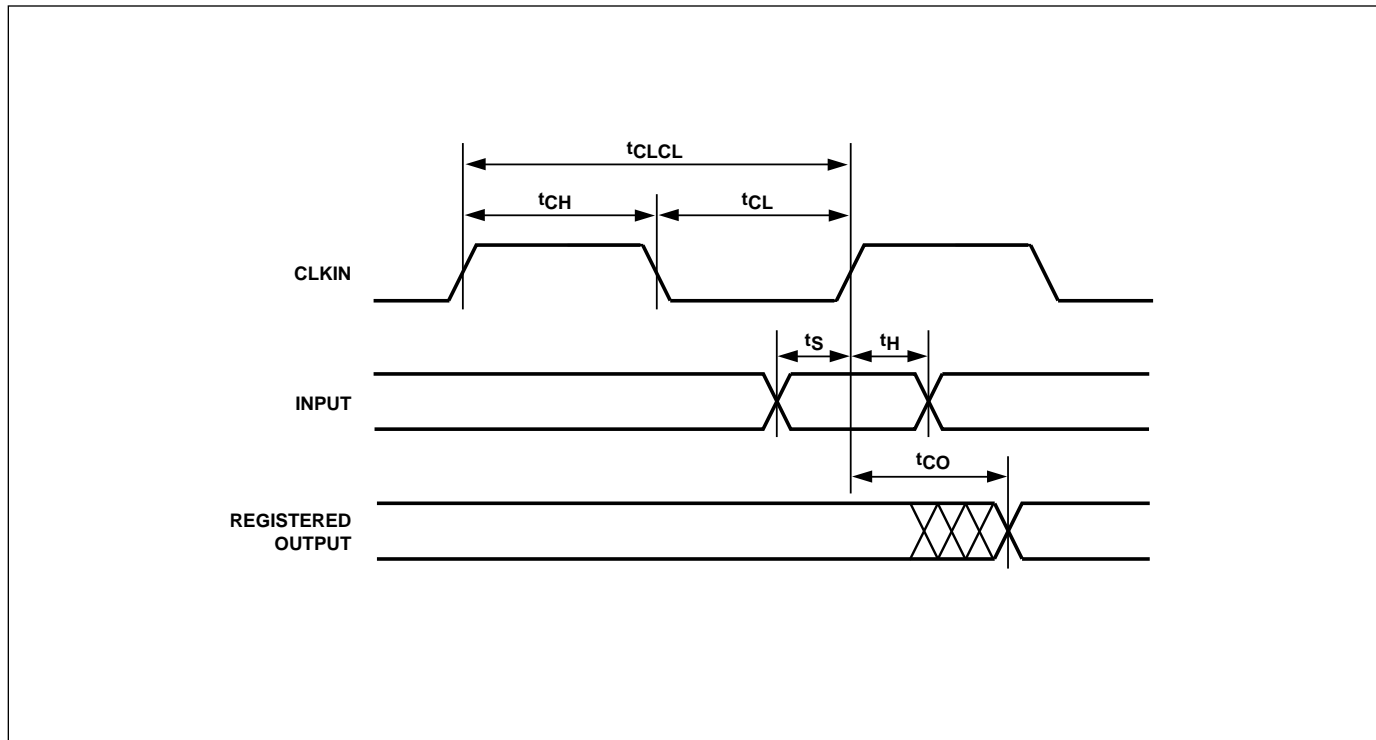
*Figure 40.  Asynchronous Clock Mode Timing (Product-Term Clock)*
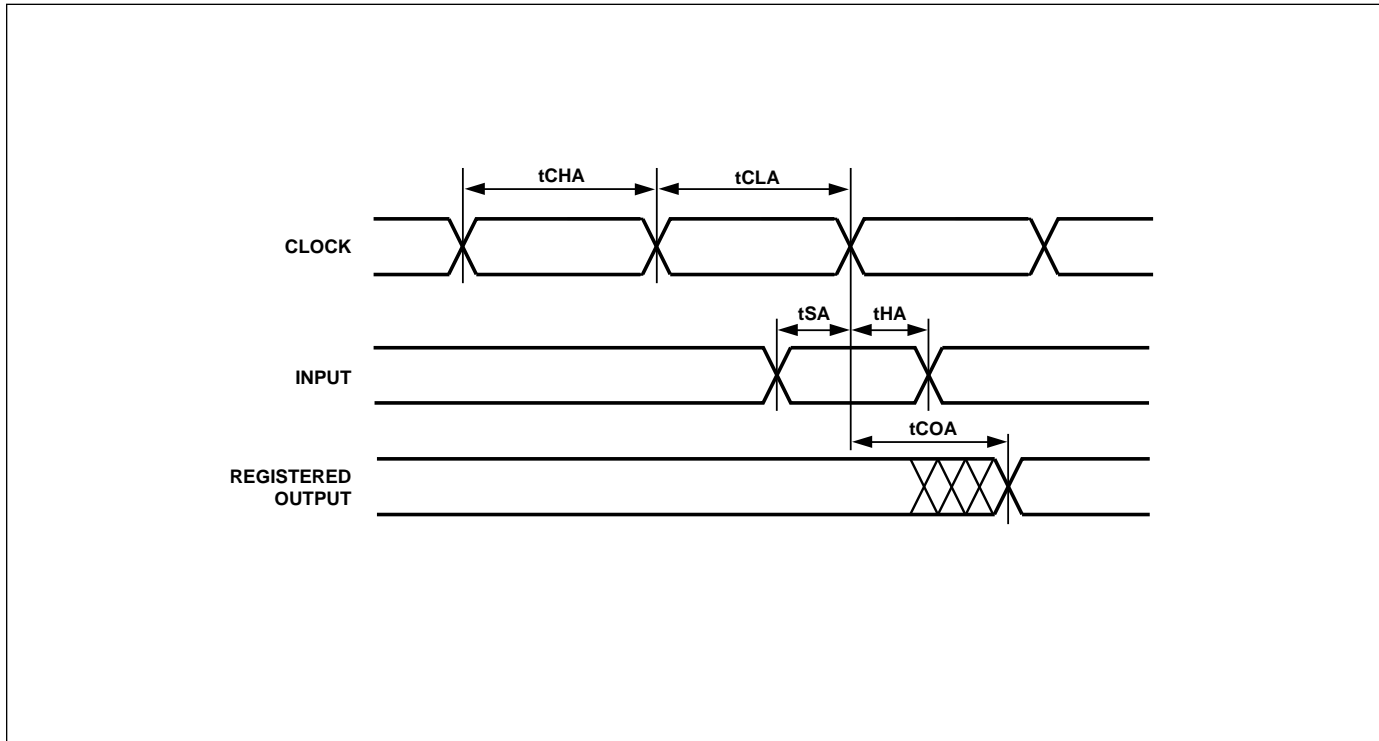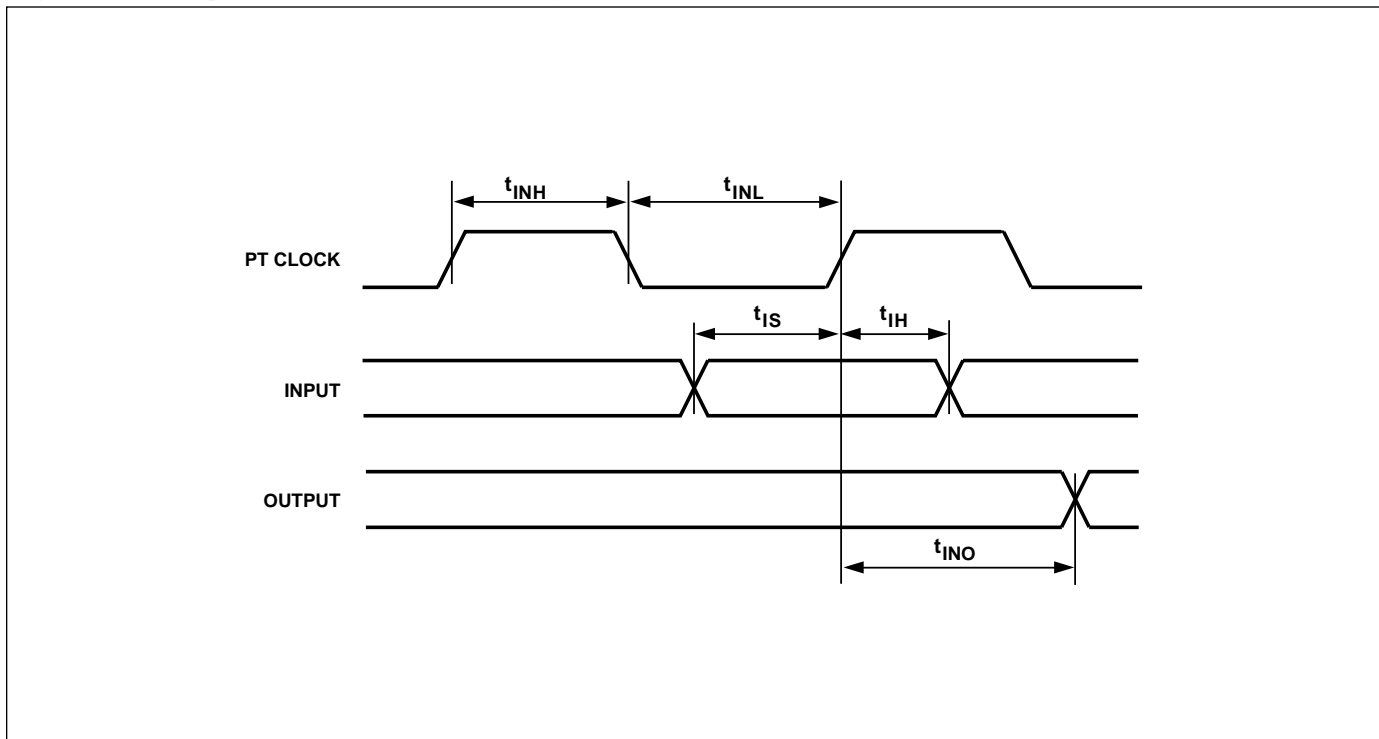
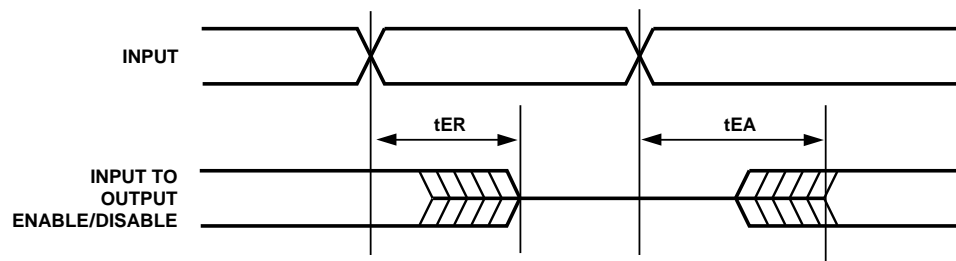

*Figure 41.  Input Micro⇔Cell Timing (Product-Term Clock)*

## *Figure 42.  Input to Output Disable/Enable*

INPUT

tER          tEA

INPUT TO
OUTPUT
ENABLE/DISABLE

## *Figure 43.  Asynchronous Reset/Preset*

tARPW

RESET/PRESET
INPUT

tARP

REGISTER
OUTPUT
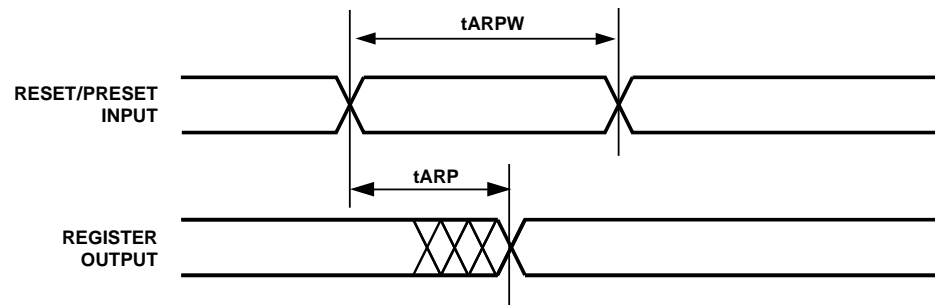
## Figure 44.  Power Up Timing
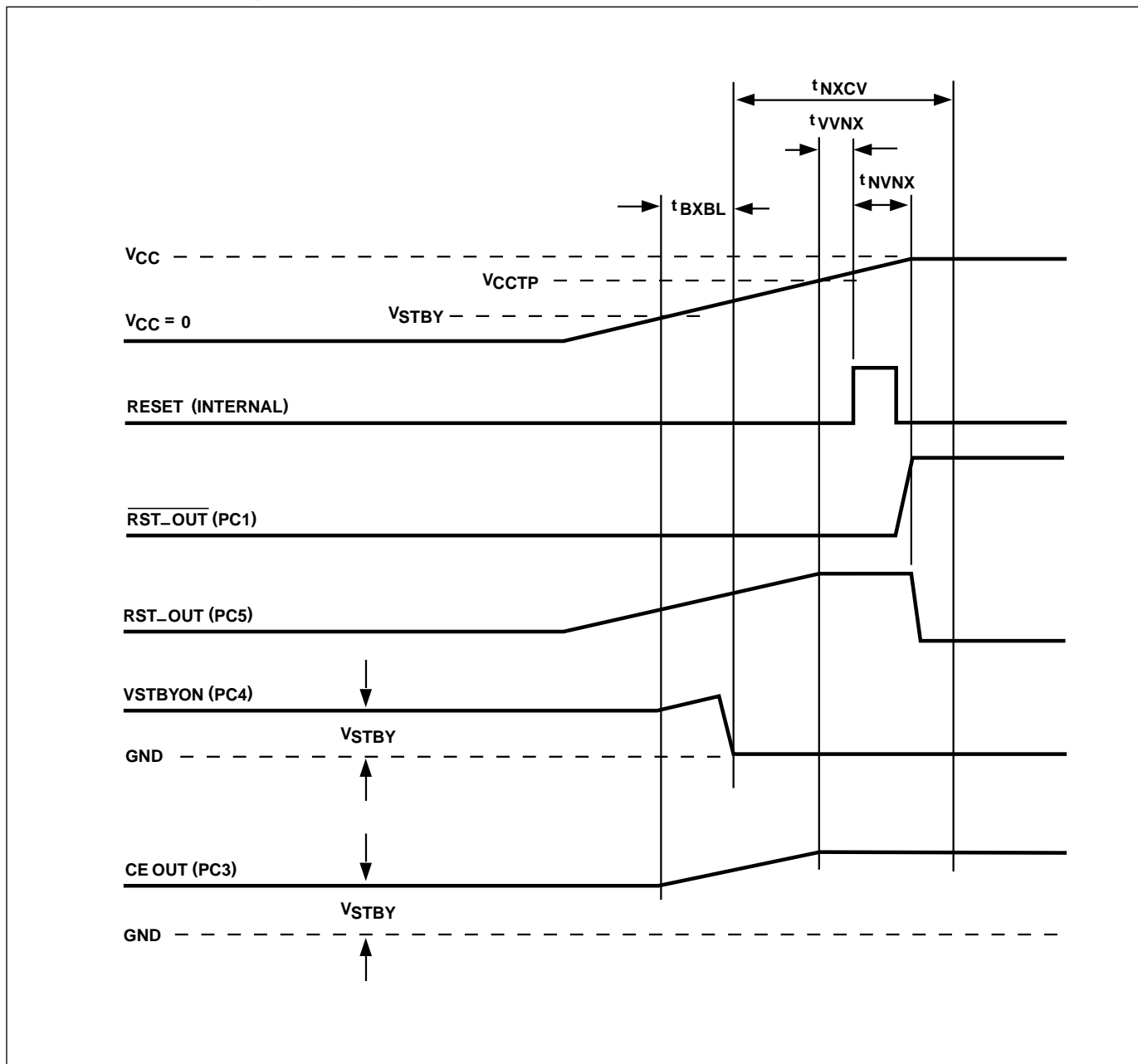
## *Figure 45.  Power Down Timing*
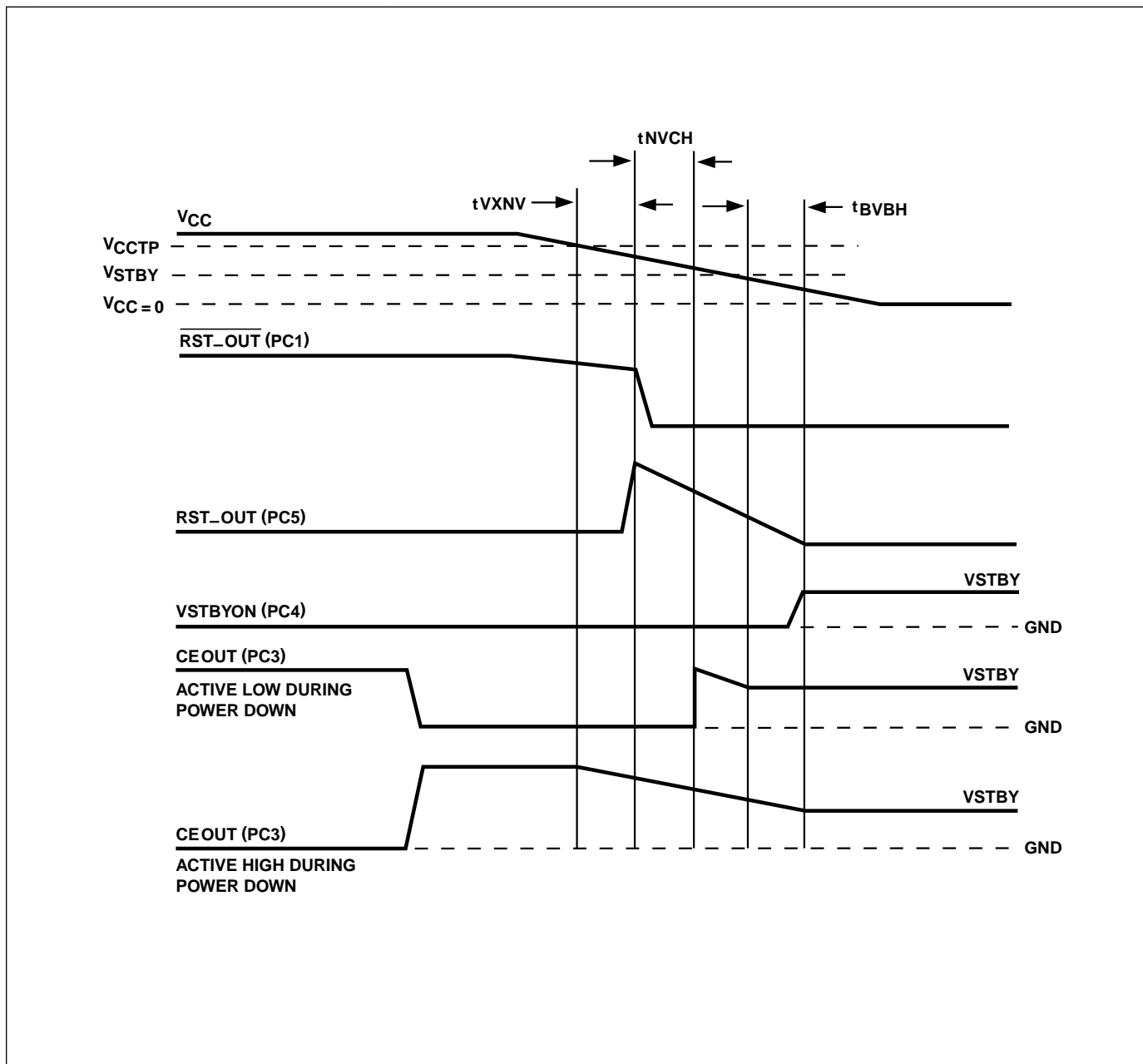
## *Figure 46.  Reset Input Timing*
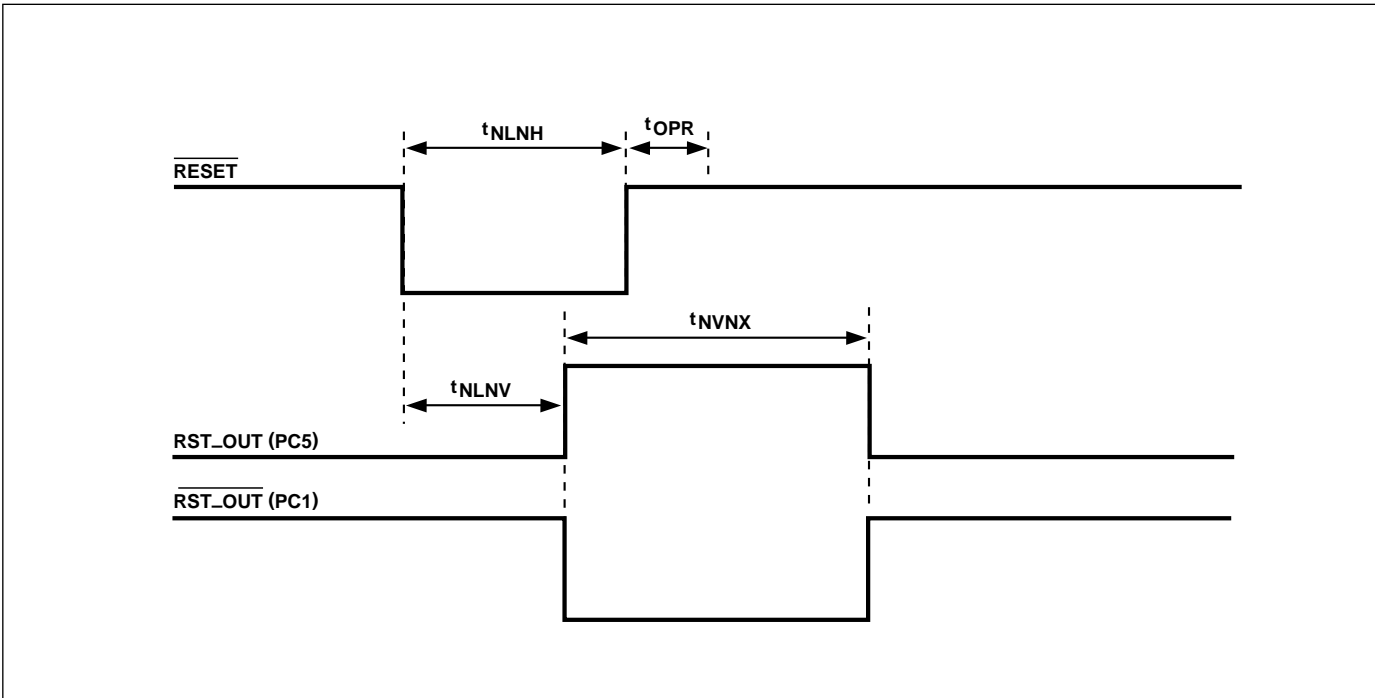


## *Figure 47.  Key to Switching Waveforms*

## *Pin Capacitance*

$T_A = 25 \ °C, \ f = 1 \ MHz$

| Symbol | Parameter[1] | Conditions | Typical[2] | Max | Unit |
|--------|-----------|------------|----------|-----|------|
| $C_{IN}$ | Capacitance (for input pins only) | $V_{IN} = 0$ V | 4 | 6 | pF |
| $C_{OUT}$ | Capacitance (for input/output pins) | $V_{OUT} = 0$ V | 8 | 12 | pF |
| $C_{VPP}$ | Capacitance (for WR/$V_{PP}$ or R/W/$V_{PP}$) | $V_{PP} = 0$ V | 18 | 25 | pF |

**NOTES:** 1. These parameters are only sampled and are not 100% tested.
2. Typical values are for $T_A$ = 25°C and nominal supply voltages.

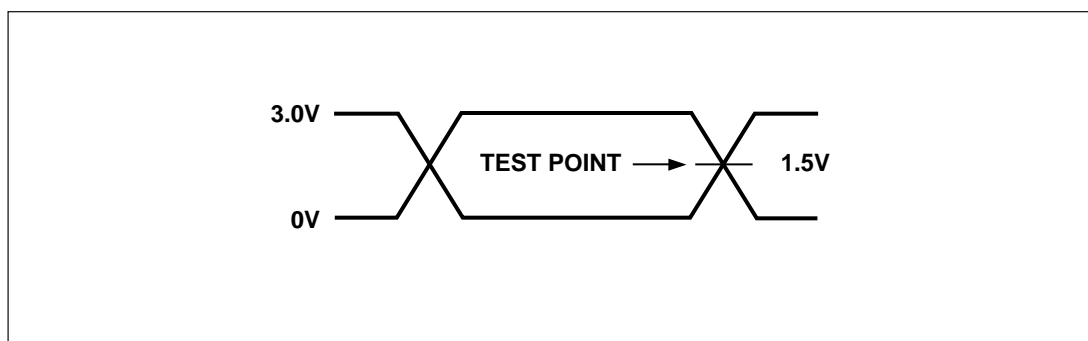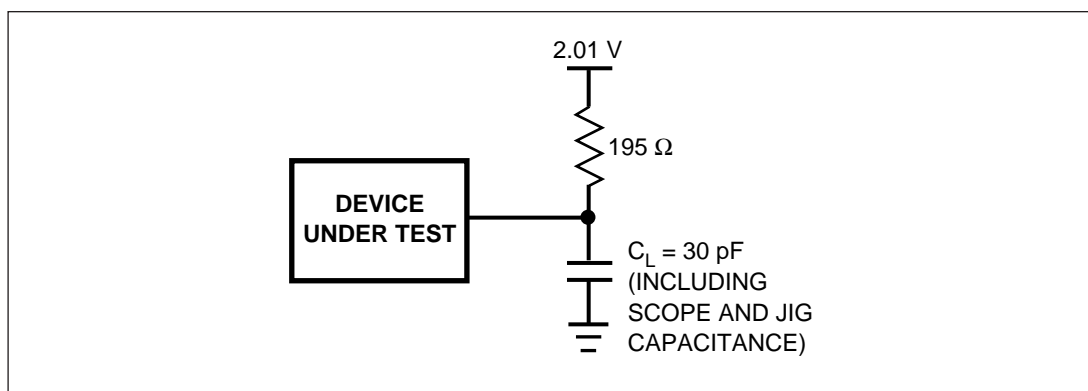## *Figure 48. AC Testing Input/Output Waveform*



## *Figure 49. AC Testing Load Circuit*



## *Erasure and Programming*

To clear all locations of their programmed contents, expose the window packaged device to an ultra-violet light source. A dosage of 30 W second/cm[2] is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm[2] for 40 to 45 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD7XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD7XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.
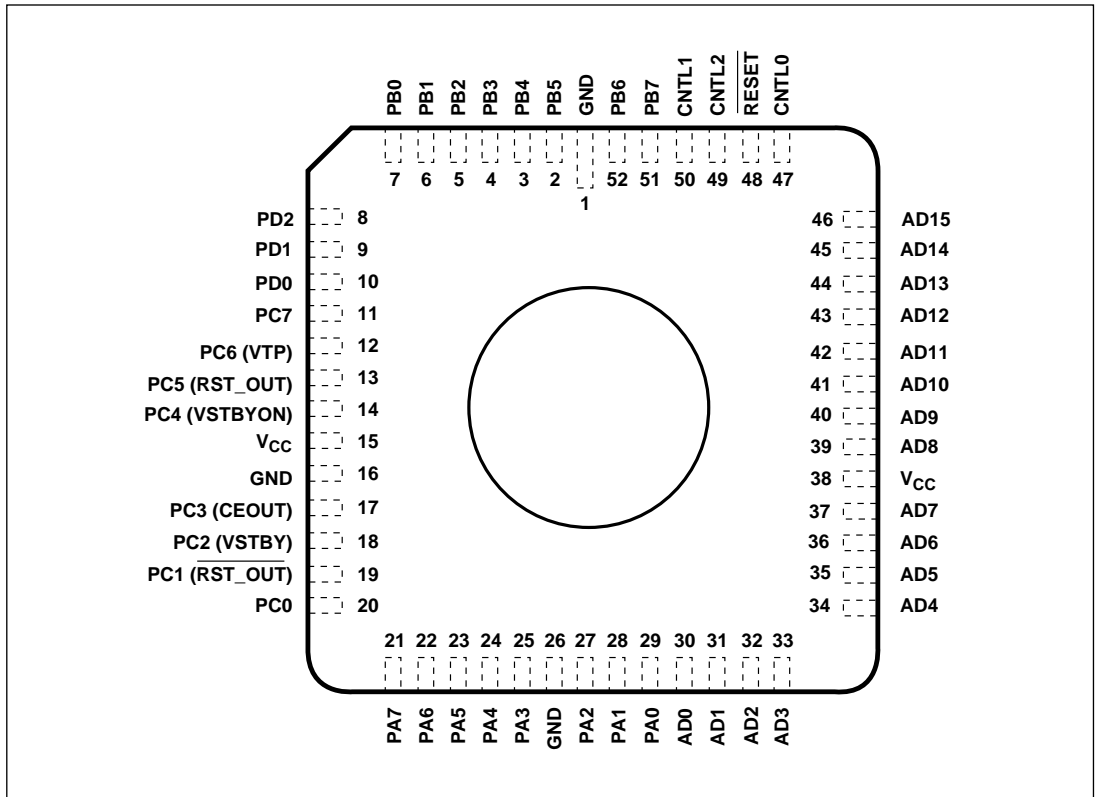
**PSD7XX
Pin
Assignments**

| Pin No. | Pin Assignments | Pin No. | Pin Assignments |
|---------|-----------------|---------|-----------------|
| 52-Pin PLDCC/ CLDCC | 52-Pin PLDCC/CLDCC | 52-Pin PLDCC/ CLDCC | 52-Pin PLDCC/CLDCC |
| 1 | GND | 27 | PA2 |
| 2 | PB5 | 28 | PA1 |
| 3 | PB4 | 29 | PA0 |
| 4 | PB3 | 30 | AD0 |
| 5 | PB2 | 31 | AD1 |
| 6 | PB1 | 32 | AD2 |
| 7 | PB0 | 33 | AD3 |
| 8 | PD2 | 34 | AD4 |
| 9 | PD1 | 35 | AD5 |
| 10 | PD0 | 36 | AD6 |
| 11 | PC7 | 37 | AD7 |
| 12 | PC6 (VTP) | 38 | $V_{CC}$ |
| 13 | PC5 (RST_OUT) | 39 | AD8 |
| 14 | PC4 (VSTBYON) | 40 | AD9 |
| 15 | $V_{CC}$ | 41 | AD10 |
| 16 | GND | 42 | AD11 |
| 17 | PC3 (CEOUT) | 43 | AD12 |
| 18 | PC2 (VSTBY) | 44 | AD13 |
| 19 | PC1 ($\overline{RST\_OUT}$) | 45 | AD14 |
| 20 | PC0 | 46 | AD15 |
| 21 | PA7 | 47 | CNTL0 |
| 22 | PA6 | 48 | RESET |
| 23 | PA5 | 49 | CNTL2 |
| 24 | PA4 | 50 | CNTL1 |
| 25 | PA3 | 51 | PB7 |
| 26 | GND | 52 | PB6 |

*PSD7XX
Package
Information*

**Figure 49. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC)
(Package Type J)**
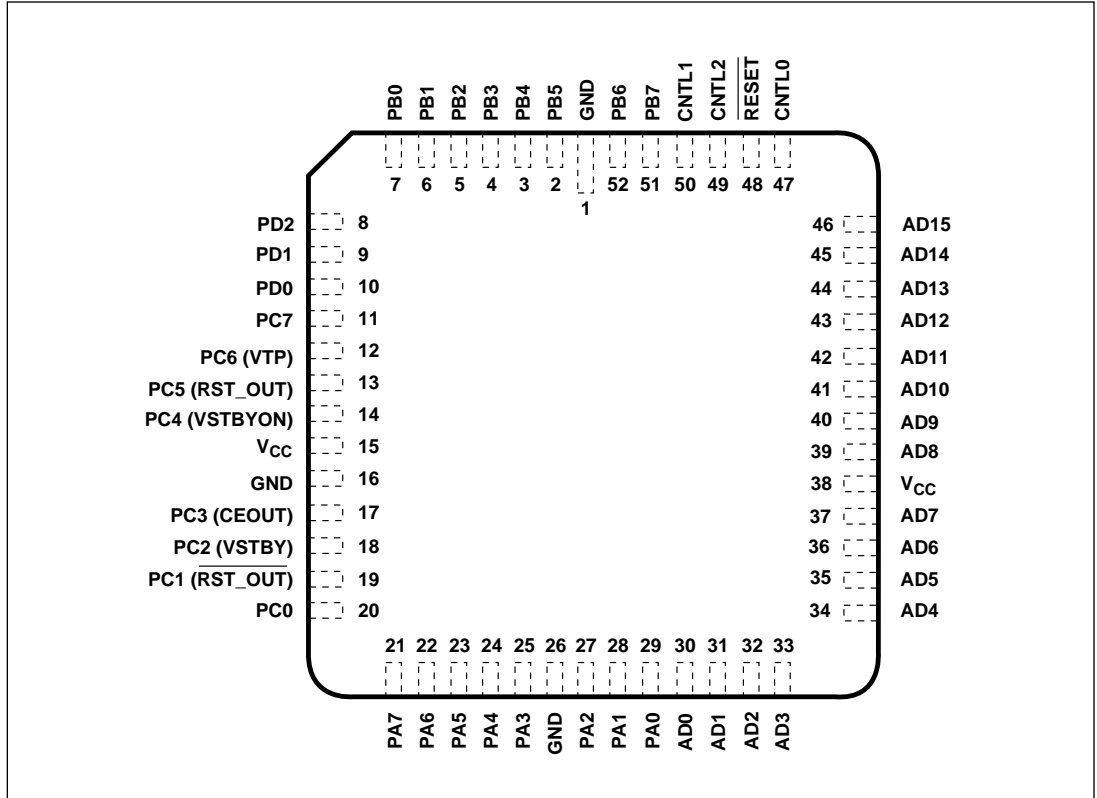


**Figure 50. Drawing L6 – 52-Pin Ceramic Leaded Chip Carrier (CLDCC)
with Window (Package Type L)**

**PSD7XX Product Errata**

Errata specifications for product shipping in the first half of 1997 are listed below. Product fully meeting specification (no errata parameters) is scheduled to ship in Q3 1997. Contact your WSI representative or check our web page at **www.wsipsd.com** for updated information.

### 5.0V ± 10% Only

| *PSD7XXS5-70* | *Specification* | *Errata Value* | *Unit* |
|---|---|---|---|
| $t_{AVLX}$ | 5 | 7 | nsec |
| $t_{LXAX}$ | 7 | 8 | nsec |
| $t_{RLQV}$ | 20 | 24 | nsec |
| $t_{WLMV}$ | 25 | 30 | nsec |
| $t_{WLQV\ (PA)}$ | 25 | 32 | nsec |
| $t_{WLQZ\ (PA)}$ | 20 | 26 | nsec |
| $t_{WHAX}$ | 0 | 18 | nsec |
| $t_{ARP}$ | 26 | 40 | nsec |
| $t_{HA}$ | 8 | 14 | nsec |
| $t_{LVDV}$ | 100 | 180 | nsec |
| *PSD7XXS5-90* | | | |
| $t_{AVLX}$ | 6 | 7 | nsec |
| $t_{WLQV\ (PA)}$ | 27 | 32 | nsec |
| $t_{WLQZ\ (PA)}$ | 25 | 26 | nsec |
| $t_{WHAX}$ | 0 | 18 | nsec |
| $t_{ARP}$ | 29 | 40 | nsec |
| $t_{HA}$ | 8 | 14 | nsec |
| $t_{LVDV}$ | 120 | 180 | nsec |
| *PSD7XXS5-15* | | | |
| $t_{WHAX}$ | 0 | 18 | nsec |
| $t_{ARP}$ | 31 | 40 | nsec |
| $t_{HA}$ | 8 | 14 | nsec |
| $t_{LVDV}$ | 140 | 180 | nsec |

**Product Revisions**

| *Product Revisions* | *Data Sheet Changes* |
|---|---|
| Original PSD7XX (7/97) | – |
| 10/97 | $t_{VXNV}$, $t_{NVCH}$, and $t_{NXCV}$ on pgs. 90 and 91 corrected from ns to µs |