MHS

MATRA M H S

September 1990

DATA SHEET

HM 65789

16 K x 4 HIGH SPEED CMOS SRAM WITH OUTPUT ENABLE

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FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 25*/35/45/55 ns
  COMMERCIAL : 15*/20/25/35/45 ns
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **OUTPUT ENABLE**

DESCRIPTION

The HM 65789 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65789 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

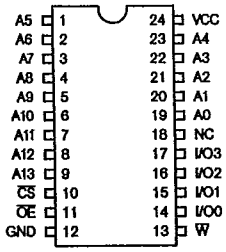
Easy memory expansion is provided by an active low chip select (CS), an active low output enable (OE) and three state drivers.
All inputs and outputs of the HM 65789 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65789 is processed following the test methods of MIL STD 883C.

PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
Tape and Reel Service.

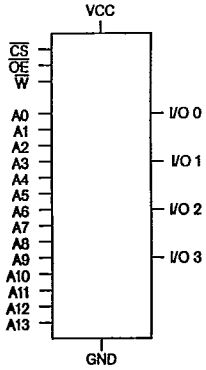
SOIC & SOJ 300 mils, 24 pins.

Pinout DIL 24 pins (top view)

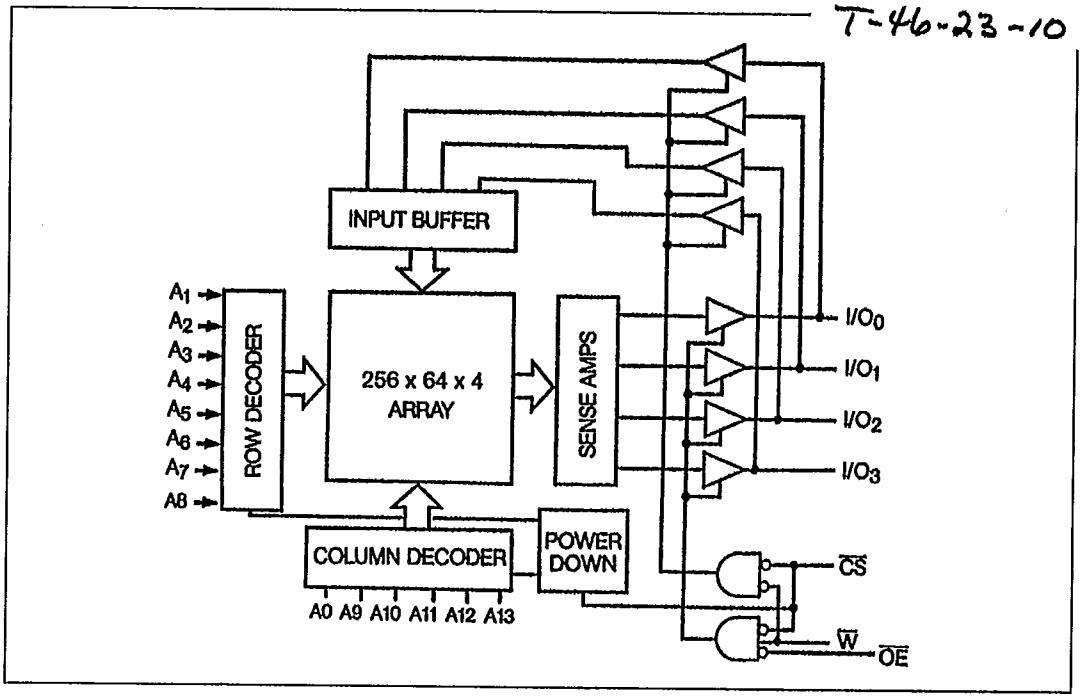


* preliminary

LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13	: Address inputs	$\overline{CS}$	: Chip-select
I/O0-I/O3	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	X	L	Valid	Z	Write

L = low - H = high - X = H or L-Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

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OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

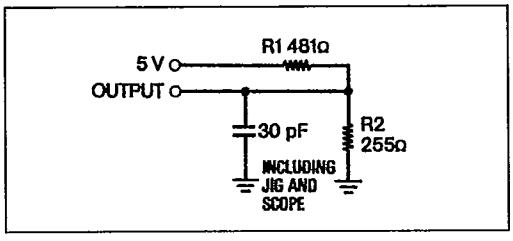


Fig. 1a.

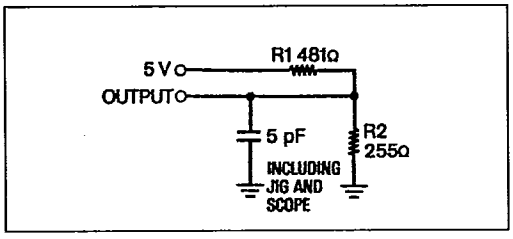
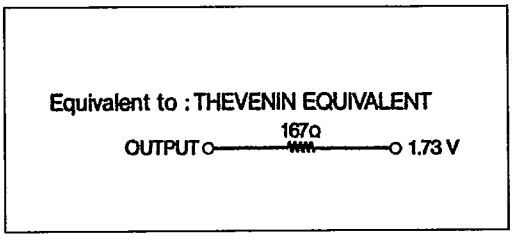


Fig. 1b.



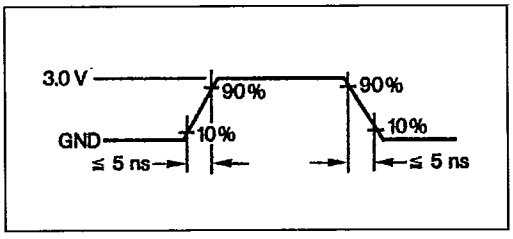


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	−10.0	–	10.0	µA
IOZ	(3)	Output leakage current	−10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	−350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

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Consumption for Commercial specification :

SYMBOL	PARAMETER	65789 E*-5	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	40	40	30	30	30	mA	max
ICCSB1 (7)	Standby supply current	20	20	20	20	20	mA	max
ICCOP (8)	Dynamic operating current	115	100	100	100	100	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65789 H-9/-2	65789 K-9/-2	65789 M-9/2	65789 N-9/-2	UNIT	VALUE
ICCSB (6)	Standby supply current	40	30	30	30	mA	max
ICCSB1 (7)	Standby supply current	20	20	20	20	mA	max
ICCOP (8)	Dynamic operating current	100	100	100	100	mA	max

Notes : 6. $\overline{CS}$ ≥ VIH, min duty cycle = 100 %. A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. $\overline{CS}$ = Vcc − 0.3 V Iout = 0 mA.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : + 30 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65789 E-5*	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
TAVAV	Write cycle time	15	20	20	25	40	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	12	15	20	25	30	ns	min
TDVWH	Data set-up time	10	10	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	12	15	20	25	30	ns	min
TWLQZ	Write low to high Z	7	7	7	10	15	ns	max
TWLWH	Write pulse width	12	15	15	20	20	ns	min
TWHAX	Address hold from end of write	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	5	5	5	5	5	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65789 H-9/-2	65789 K-9/-2	65789 M-9/-2	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	ns	min
TDVWH	Data set-up time	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	20	25	30	ns	min
TWLQZ (8)	Write low to high Z	7	10	15	ns	max
TWLWH	Write pulse width	15	20	25	ns	min
TWHAX	Address hold from end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (8)	Write high to low Z	5	5	5	ns	min

Note : 9. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
* Preliminary.

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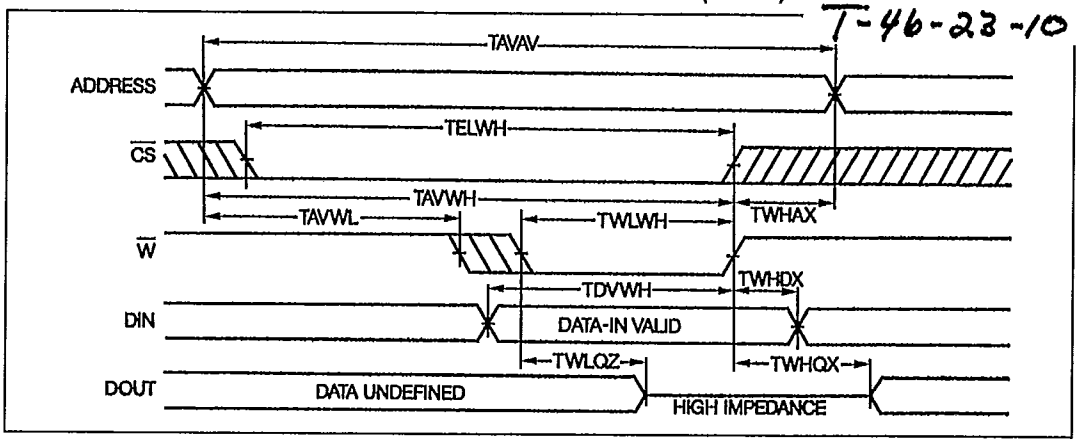
WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 9)



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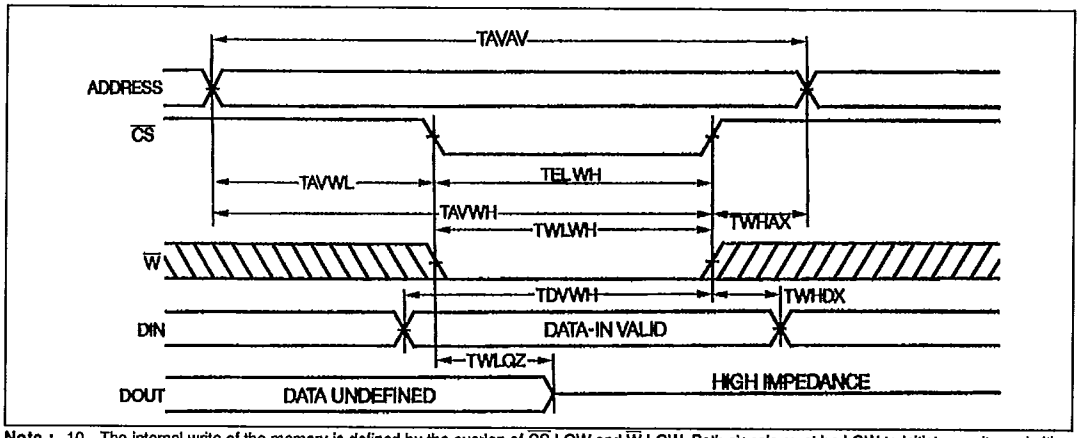
WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 9)



Note : 10. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a writee by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out will be high impedance if $\overline{OE}$ = VIH.

READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65789 E-5*	65789 F-5	65789 H-5	65789 K-5	65789 M-5	UNIT	VALUE
TAVAV	Read cycle time	15	20	25	35	45	ns	min
TAVQV	Address access time	15	20	25	35	45	ns	max
TAVQX	Address valid to low Z	3	3	3	3	3	ns	min
TELQV	Chip-select access time	15	20	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	8	8	10	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	15	20	25	35	45	ns	max
TGLQV	Output enable access time	10	10	12	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	8	8	10	12	15	ns	max

READ CYCLE : Military specification

SYMBOL	PARAMETER	65789 H-9/2	65789 K9/2	65789 M9/2	65789 N-9/2	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	35	45	55	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	15	ns	max

* Preliminary.

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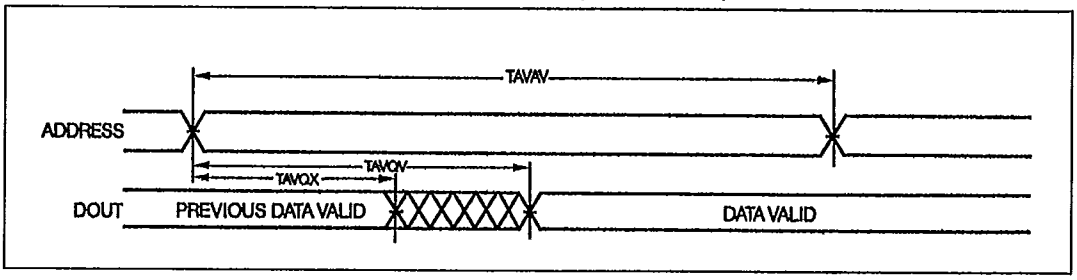
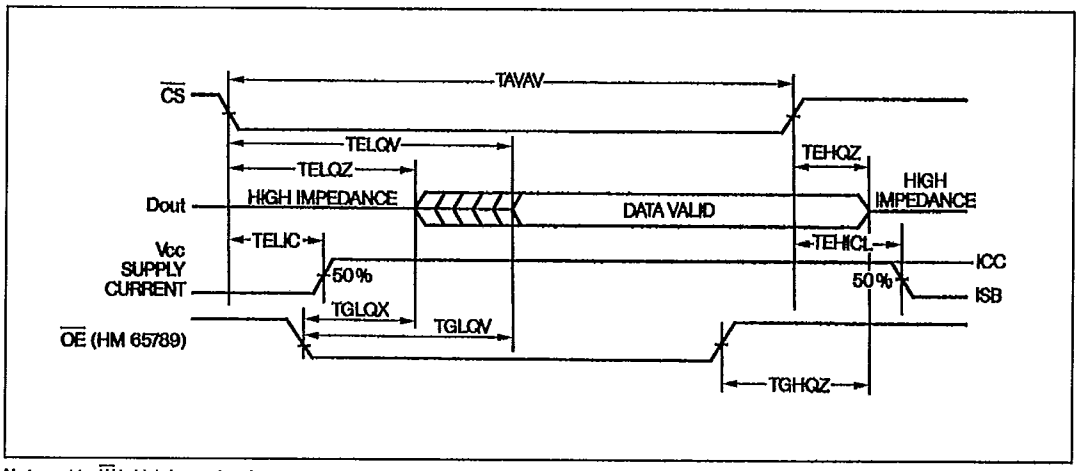
READ CYCLE nb 1 : (notes 10, 11)



READ CYCLE nb 2 : (notes 10, 12)



Notes : 11. $\overline{W}$ is high for read cycle.
12. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
13. Address valid prior or coincident with $\overline{CS}$ transition low.

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ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65767	F	–5 : R

- Package: 0 - Chip form; 1 - Ceramic 24 pins; 3 - Plastic 24 pins; T - SOIC 24 pins 300 mils; U - SOJ 24 pins 300 mils
- Device type: 16 k x 4 high speed static RAM with output enable
- Grade: E* = 15 ns; F = 20 ns; H = 25 ns; K = 35 ns; M = 45 ns; N = 55 ns
- Level: –5 : Commercial; –9 : Industrial; –2 : Military; –8 : Military with B.I. (B.I. = Burn-In)
- R: Tape and Reel Service

* Preliminary

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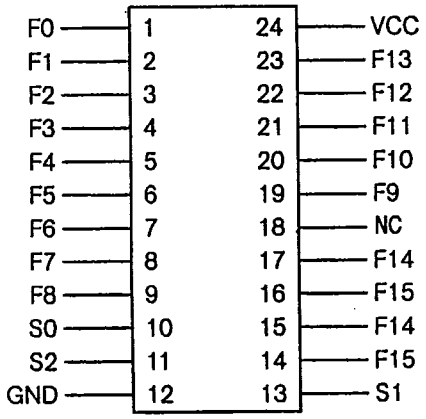
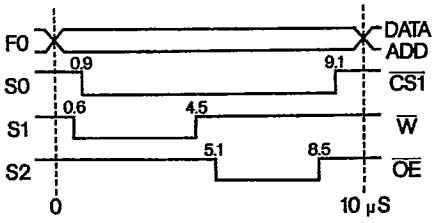
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins
SOIC DIL, 300 mils, 24 pins
Ceramic, 300 mils, 24 pins
LCC rectangular, 28 pins

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
FO = 50 KHz ± – 20 %
Fn = 1/2 Fn – 1
S0 to S2 = programmable signals for write/read cycles
NC = Non connected