MOTOROLA

MC1444
MC1544

HIGH-SPEED, LOW THRESHOLD SENSE AMPLIFIERS

The MC1444 and MC1544 are high-speed quad sense amplifiers for use with plated wire, thin film or other memory systems requiring very low threshold sensitivity and narrow pulse widths. Both devices feature internal capacitive coupling to reduce the effects of voltage offsets.

- Threshold Level – 1.5 mV (Typ), 100 ns Rectangular Pulse
- Decoded Input Channel Selection
- Output Strobe Capability
- DC Level Restore Gate on Internal Capacitors Eliminates Repetition Rate Limitations

AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

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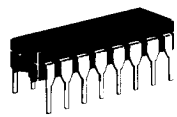


L SUFFIX
CASE 620

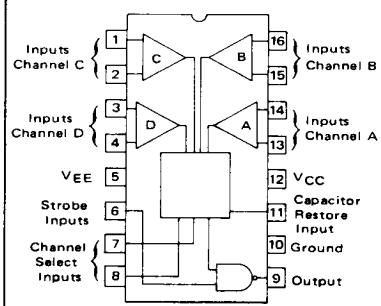
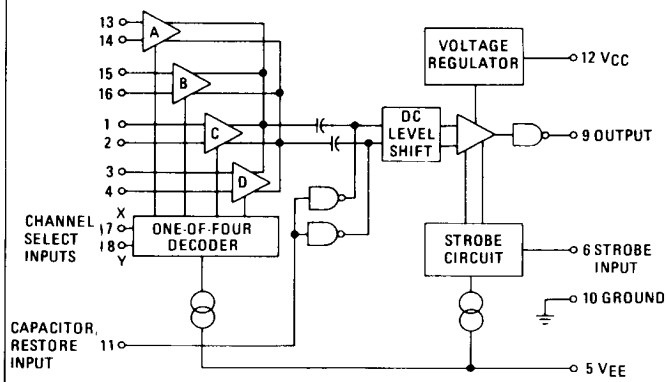


FIGURE 1 – BLOCK DIAGRAM



TRUTH TABLES

Channel Select		
Pin 7(X)	Pin 8(Y)	Channel Selected
H	H	A
L	H	B
H	L	C
L	L	D

H = high level (steady state, $V_I \geq V_{IH(min)}$ or $V_{ID} > V_{th}$
L = low level (steady state), $V_I \leq V_{IL(max)}$ or $V_{ID} < V_{th}$
X = irrelevant (any input, including transitions)
⎍ = transition from low level to high level
⎍ = low-level output pulse

Inputs					Output
Strobe	Capacitor Restore	Differential Input *Channel A	Channel Selects		
L	X	X	X	X	H
X	H	X	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	L	H	H	⎍	⎍
H	L	H	⎍	H	⎍
⎍	L	H	H	H	⎍

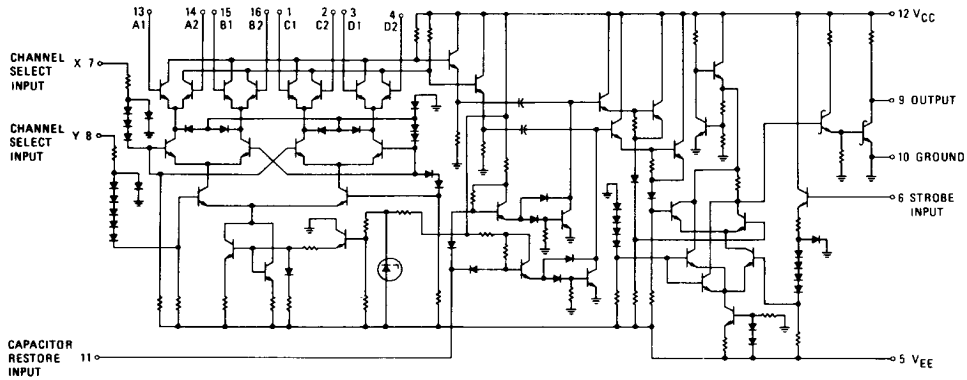
*Channel A used as an example, other channels function similarly. See channel select table.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating		Symbol	Value	Unit
Power Supply Voltages(1)		V_{CC} V_{EE}	+7.0 -8.0	Vdc
Input Common-Mode Voltage Range		V_{ICR}	+5.0, -6.0	Vdc
Input Differential-Mode Voltage Range(2)		V_{IDR}	+5.0, -6.0	Vdc
Input Capacitor Restore, Channel Select, and Strobe Voltage		$V_{I(CR)}$ $V_{I(CS)}$ $V_{I(S)}$	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = 25°C		P_D	1.0 6.7	Watt mW/°C
Operating Ambient Temperature Range	MC1444 MC1544	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Operating Junction Temperature		T_J	+175	°C

(1) All voltage values, except differential voltages, are with respect to the network ground terminal.
(2) Differential input voltages are at A1 with respect to A2, and similarly B1 to B2, C1 to C2, and D1 to D2.

FIGURE 2 – EQUIVALENT CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	4.75 -5.7	5.0 -6.0	5.25 -6.30	V

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 V ≤ V_{CC} ≤ 5.25 V, -5.7 V ≥ V_{EE} ≥ -6.3 V, T_A = 25°C.)

Characteristic	Symbol	MC1444			MC1544			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Threshold Voltage (Figure 4) (V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = T_{high} to T_{low}) (1)	V_{th}	0.3	1.0	2.3	0.5	1.0	1.5	mV
Input Bias Current (Selected Channel)	I_{IB}	–	20	50	–	20	50	μA
Input Offset Current (Selected Channel)	I_{IO}	–	1.0	10	–	1.0	10	μA
Channel Select Input Current-High Logic State, ($V_{IH(CS)}$ = 3.5 V)	$I_{IH(CS)}$	–	–	2.6	–	–	2.6	mA
Channel Select Input Current - Low Logic State, ($V_{IL(CS)}$ = 0 V)	$I_{IL(CS)}$	–	–	1.0	–	–	1.0	mA
Capacitor Restore Input Current - High Logic State, ($V_{IH(CR)}$ = 3.5 V)	$I_{IH(CR)}$	–	–	10	–	–	10	μA
Capacitor Restore Input Current-Low Logic State, ($V_{IL(CR)}$ = 0 V)	$I_{IL(CR)}$	–	–	-3.5	–	–	-3.5	mA
Strobe Input Current-High Logic State, ($V_{IH(S)}$ = 3.5 V)	$I_{IH(S)}$	–	–	200	–	–	200	μA
Strobe Input Current-Low Logic State ($V_{IL(S)}$ = 0 V)	$I_{IL(S)}$	–	–	200	–	–	200	μA
Channel Select Input Voltage-Low Logic State	$V_{IL(CS)}$	–	–	0.7	–	–	0.7	V
Channel Select Input Voltage-High Logic State	$V_{IH(CS)}$	2.1	–	–	2.1	–	–	V
Capacitor Restore Input Voltage-Low Logic State	$V_{IL(CR)}$	–	–	0.8	–	–	0.8	V
Capacitor Restore Input Voltage-High Logic State	$V_{IH(CR)}$	2.0	–	–	2.0	–	–	V
Strobe Input Voltage-Low Logic State	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage-High Logic State	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Input Common-Mode Voltage Range	V_{ICR+} V_{ICR-}	– –	4.7 -6.0	– –	– –	4.7 -6.0	– –	V
Input Differential Voltage Range	V_{IDR}	–	±3.7	–	–	±3.7	–	V
Output Voltage-Low Logic State (I_{OL} = 10 mA)	V_{OL}	–	0.4	0.5	–	0.4	0.5	V
Output Voltage-High Logic State (I_{OH} = -400 μA)	V_{OH}	2.4	–	–	2.4	–	–	V
Positive Power Supply Current	I_{CC}	–	–	30	–	–	30	mA
Negative Power Supply Current	I_{EE}	–	–	30	–	–	30	mA

SWITCHING CHARACTERISTICS (unless otherwise noted, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = -6.0 V)

Characteristic	Symbol	MC1444			MC1544			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time Differential Inputs to High Logic State Output	$t_{PLH(D)}$	–	40	–	–	40	–	ns
Propagation Delay Time Differential Input to Low Logic State Output	$t_{PHL(D)}$	–	18	25	–	18	25	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	30	–	–	30	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	18	25	–	18	25	ns
Lead Time from Channel Select Input to Application of Differential Input Voltage	$t_{L(CS)}$	–	45	–	–	45	–	ns
Lead Time from Application of a 50 mV Offset Signal to Application of the Capacitor Restore Signal	$t_{L(CRO)}$	–	15	–	–	15	–	ns
Lead Time from Application of Strobe Input to Application of Differential Input Signal	$t_{L(S)}$	–	10	–	–	10	–	ns
Lead Time from Application of Capacitor Restore Signal to Application of Differential Input Signal	$t_{L(CR)}$	–	10	–	–	10	–	ns
Common-Mode Recovery Time (e_{in1} = +2.0 V) (e_{in1} = -2.0 V)	t_{CMR+} t_{CMR-}	– –	50 50	– –	– –	50 50	– –	ns
Differential-Mode Recovery Time (e_{in1} = +1.0 V) (e_{in1} = -1.0 V)	t_{DMR+} t_{DMR-}	– –	65 65	– –	– –	65 65	– –	ns

(1) T_{high} = 75°C for MC1444, 125°C for MC1544.
T_{low} = 0°C for MC1444, -55°C for MC1544.

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FIGURE 3 – THRESHOLD VOLTAGE TEST CIRCUIT

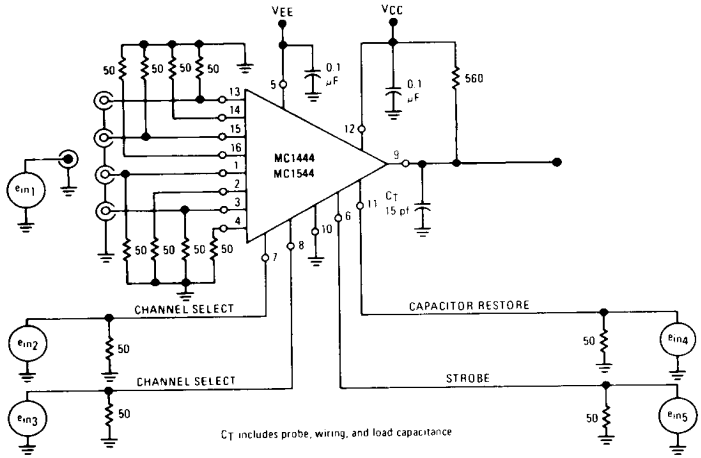


FIGURE 4 – SWITCHING CHARACTERISTICS TEST CIRCUIT

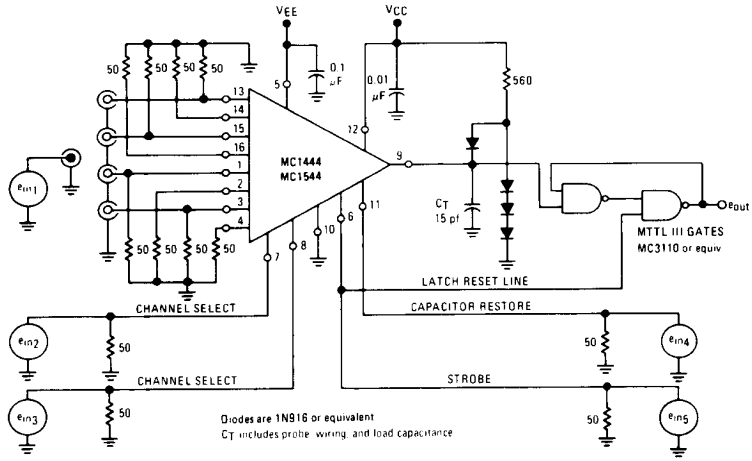
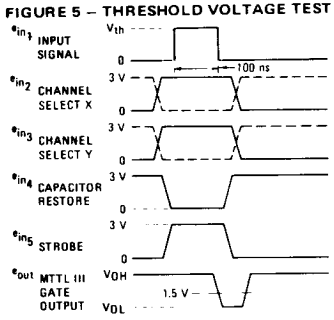
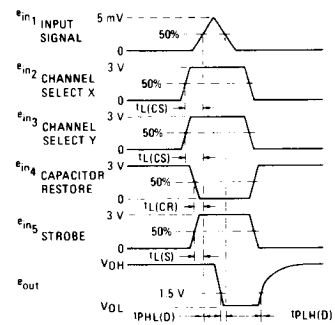


FIGURE 5 – THRESHOLD VOLTAGE TEST



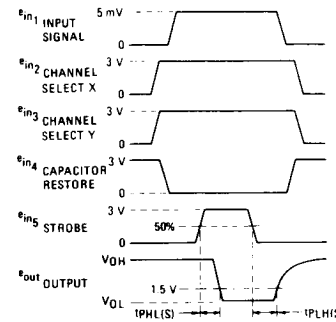
NOTE: e_{in_2} and e_{in_3} to be normal or inverted (dotted line) as necessary to select desired channel. For e_{in_1} – e_{in_5} t_{TLH}, t_{THL} ≤ 10 ns

FIGURE 6 – $t_{L(CS)}$, $t_{L(CR)}$, $t_{L(S)}$, $t_{PLH(D)}$



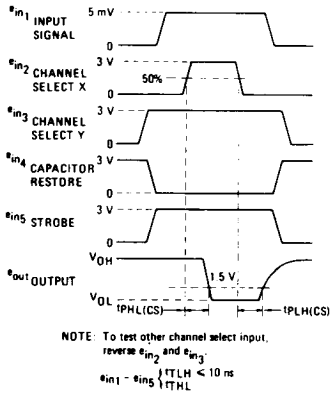
NOTE: e_{in_2} – e_{in_5} t_{TLH}, t_{THL} ≤ 10 ns

FIGURE 7 – $t_{PLH(S)}$, $t_{PHL(S)}$



NOTE: e_{in_1} – e_{in_2} t_{TLH}, t_{THL} ≤ 10 ns

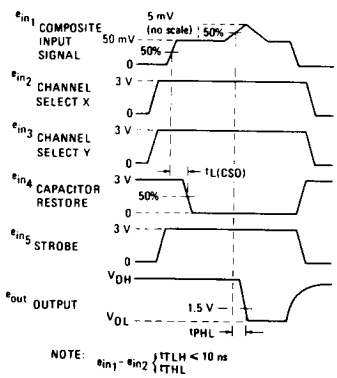
FIGURE 8 – $t_{PLH(CS)}$, $t_{PHL(CS)}$



NOTE: To test other channel select input, reverse e_{in_2} and e_{in_3}.

$e_{in_1} - e_{in_5}$ $\begin{cases} t_{TLH} \leq 10\ ns \\ t_{THL} \end{cases}$

FIGURE 9 – $t_{L(CRO)}$



NOTE: $e_{in_1} - e_{in_2}$ $\begin{cases} t_{TLH} \leq 10\ ns \\ t_{THL} \end{cases}$

DEFINITIONS

V_{OH}	Output Voltage – High Logic State
V_{OL}	Output Voltage – Low Logic State
$V_{IH(S)}$	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
$V_{IL(S)}$	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal (e_{in_1}) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 5
V_{ICM+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{ICM-}	The minimum common-mode input voltage that will not break down the amplifier
$V_{IH(CR)}$	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
$V_{IL(CR)}$	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
$V_{IH(CS)}$	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
$V_{IL(CS)}$	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{ID}	The maximum differential-mode input voltage that will not saturate the amplifier
I_{OH}	Output Source Current – High Logic State
I_{OL}	Output Sink Current - Low Logic State
$I_{IH(S)}$	The current into the strobe input when the input is at a high-level of 3.5 volts
$I_{IL(S)}$	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or – 2 volt common-mode signal (t_{TLH}, $t_{THL} \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
$t_{L(CRO)}$	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 9
$t_{L(CR)}$	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{L(CS)}$	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{PLH(CS)}$	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{PHL(CS)}$	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or – 1 volt differential-mode signal (t_{TLH}, $t_{THL} \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 23
$t_{PLH(D)}$	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 6
$t_{PHL(D)}$	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 6
$t_{L(S)}$	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 6
$t_{PLH(S)}$	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the High Logic Level as shown in Figure 7
$t_{PHL(S)}$	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the High Logic Level as shown in Figure 7
$I_{IH(CS)}$	The current into the channel select input when the input is at a high-level of 3.5 volts
$I_{IH(CR)}$	The current out of the capacitor restore input when the input is at a low-level of 0 volts
$I_{IL(CS)}$	The input current to a channel select input when that input is at a high-level of 3.5 volts
$I_{IL(CR)}$	The current into a channel select input when the input is at a low-level of 0 volts

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 10 – THRESHOLD VOLTAGE versus TEMPERATURE

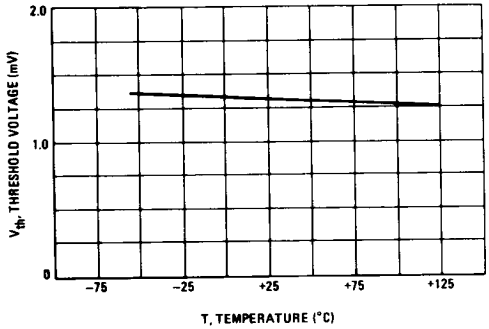


FIGURE 11 – THRESHOLD VOLTAGE versus POWER SUPPLIES

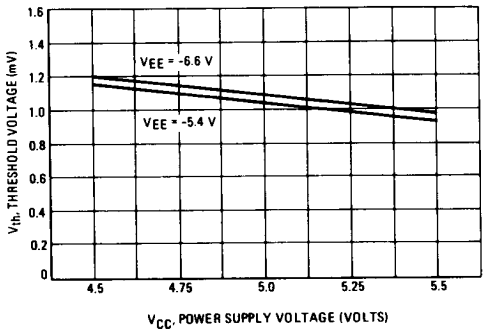


FIGURE 12 – THRESHOLD versus INPUT OFFSET VOLTAGE

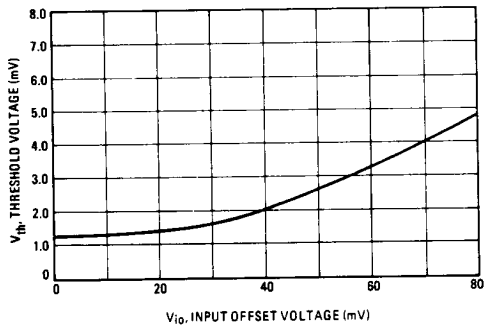


FIGURE 13 – THRESHOLD VOLTAGE versus PULSE WIDTH

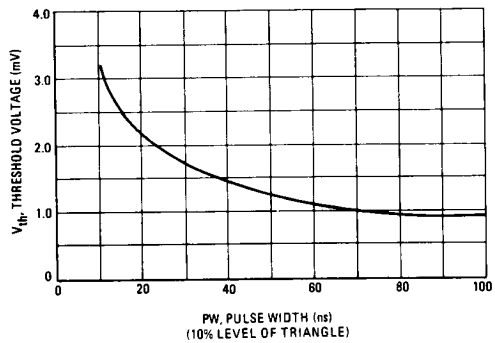


FIGURE 14 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

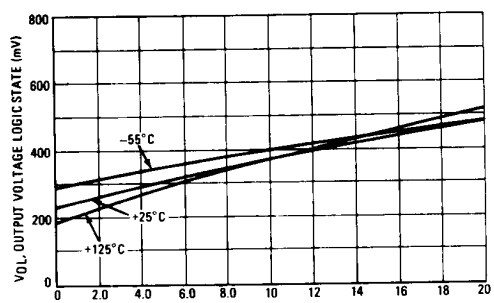
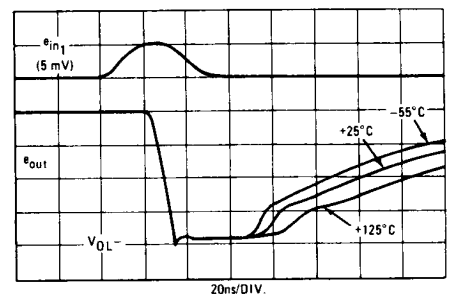


FIGURE 15 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figure 3 and 6)



TYPICAL CHARACTERISTICS (continued)

FIGURE 16 – INPUT IMPEDANCE versus FREQUENCY

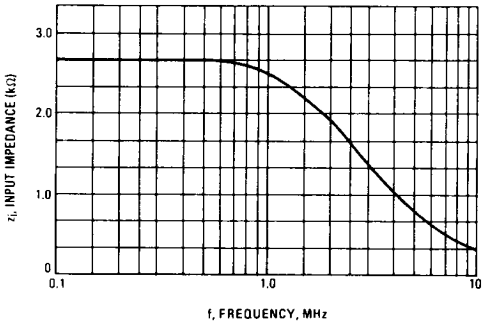


FIGURE 17 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

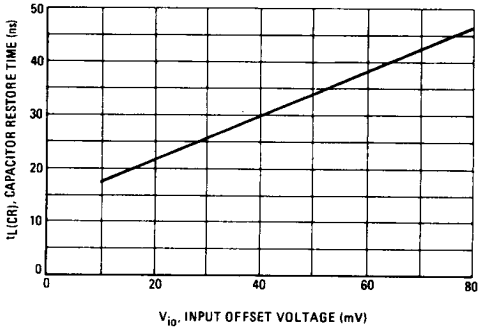


FIGURE 18 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

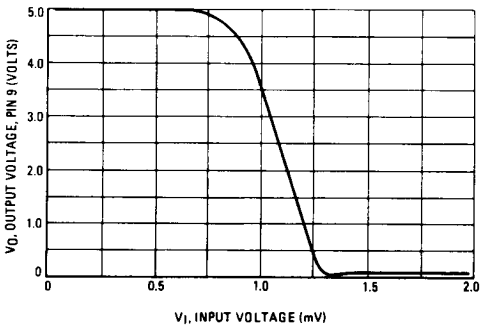


FIGURE 19 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

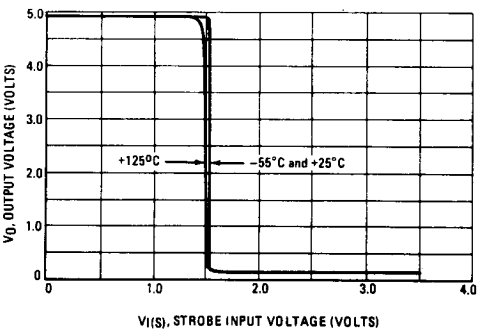


FIGURE 20 – CHANNEL SELECT X to OUTPUT TRANSFER CHARACTERISTICS

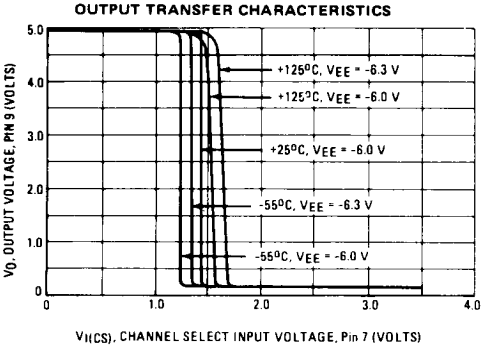


FIGURE 21 – CHANNEL SELECT Y to OUTPUT TRANSFER CHARACTERISTICS

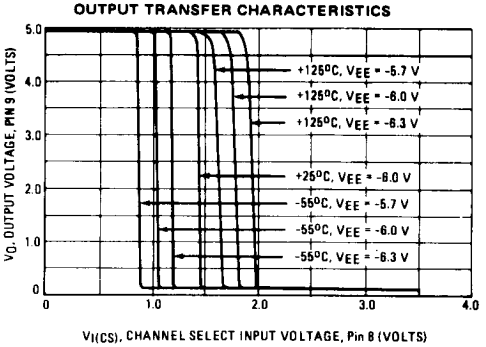


FIGURE 22 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.

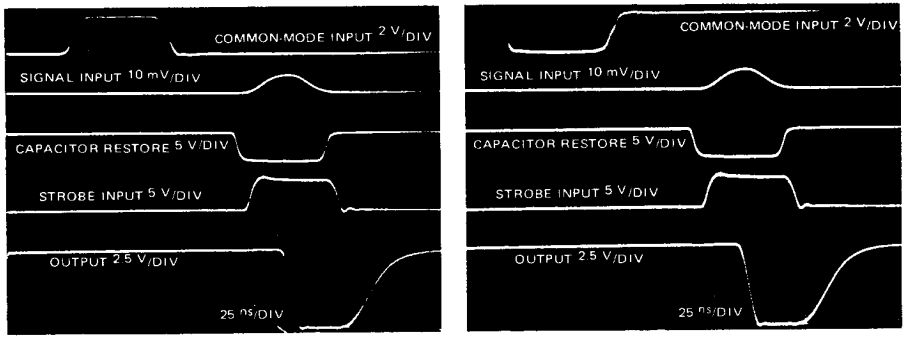


FIGURE 23 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential input and is shown separately for reference only.