



RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 50 watt RF power LDMOS transistors are designed for cellular base station applications covering the frequency range of 2110 to 2170 MHz.

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1500$ mA, $P_{out} = 50$ Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	16.7	30.5	7.2	-35.7	-19
2140 MHz	17.0	31.0	7.1	-35.4	-20
2170 MHz	17.2	31.8	7.0	-34.8	-15

AFT21S230SR3
AFT21S232SR3

2110-2170 MHz, 50 W AVG., 28 V

Features

- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- NI-780S-6: R3 Suffix = 250 Units, 44 mm Tape Width, 13 inch Reel.
- NI-780S-2: R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel.
 For R5 Tape and Reel options, see p. 18.

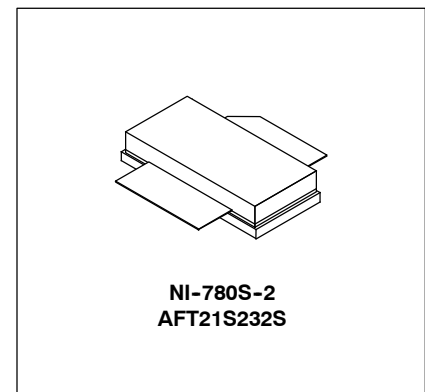
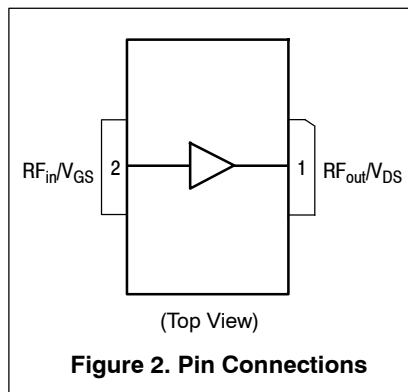
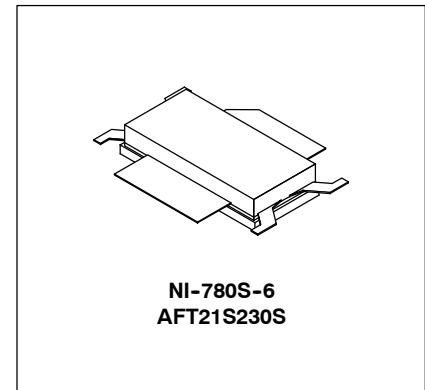
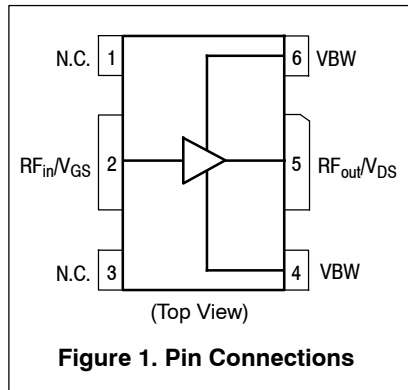


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	163 0.79	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 50 W CW, 28 Vdc, $I_{DQ} = 1500\text{ mA}$, 2110 MHz Case Temperature 86°C , 140 W CW(4), 28 Vdc, $I_{DQ} = 1500\text{ mA}$, 2110 MHz	$R_{\theta JC}$	0.43 0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 291\ \mu\text{Adc}$)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1500\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.7\text{ Adc}$)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Functional Tests (5) (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1500\text{ mA}$, $P_{out} = 50\text{ W Avg.}$, $f = 2110\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Power Gain	G_{ps}	16.0	16.7	19.0	dB
Drain Efficiency	η_D	29.0	30.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.7	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-35.7	-34.0	dBc
Input Return Loss	IRL	—	-19	-10	dB

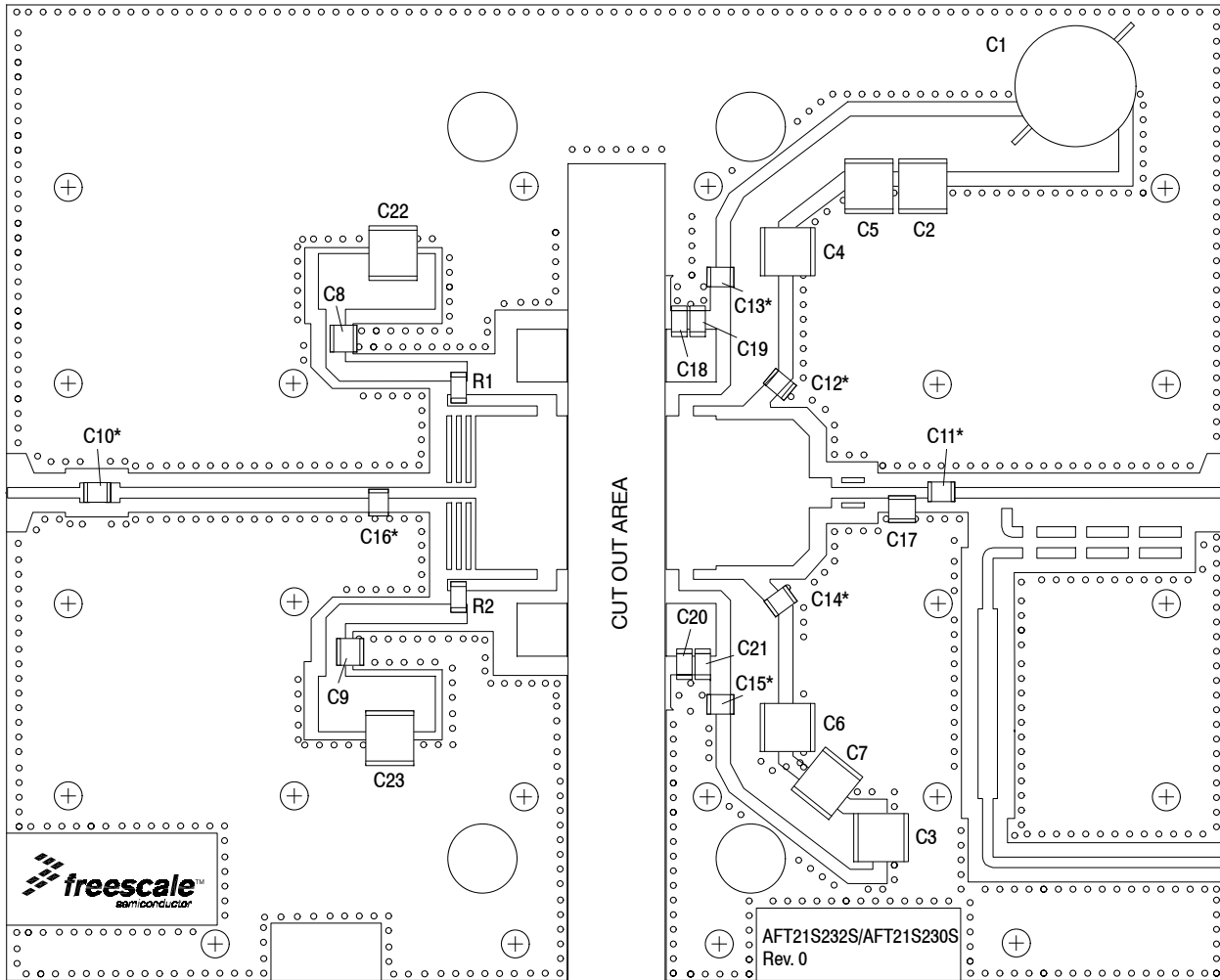
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 1500\text{ mA}$, $f = 2140\text{ MHz}$					
VSWR 10:1 at 32 Vdc, 269 W CW Output Power (3 dB Input Overdrive from 182 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1500\text{ mA}$, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	182 (1)	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	-19.3	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) AFT21S230S AFT21S232S	VBW _{res}	—	95 60	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 50\text{ W Avg.}$	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) (1)	$\Delta P1dB$	—	0.007	—	dB/°C

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C10, C11, C12, C13, C14, C15 and C16 are mounted vertically.

Figure 3. AFT21S230SR3(232SR3) Test Circuit Component Layout

Table 5. AFT21S230SR3(232SR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	470 μ F, 63 V Electrolytic Capacitor	B41694A5477Q7	EPCOS
C2, C3, C4, C5, C6, C7, C22, C23	10 μ F, 100 V Chip Capacitors	C5750X7S2A106M	TDK
C8, C9, C10, C11, C12, C13, C14, C15	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C16	0.6 pF Chip Capacitor	ATC100B0R6BT500XT	ATC
C17	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C18, C19, C20, C21	1 μ F, 50 V Chip Capacitors	CDR34BX104AKWS	AVX
R1, R2	8.2 Ω , 1/4 W Chip Resistors	RC1206FR-108R2L	Yageo
PCB	0.020", $\epsilon_r = 3.5$	RO4350B	Rogers

TYPICAL CHARACTERISTICS

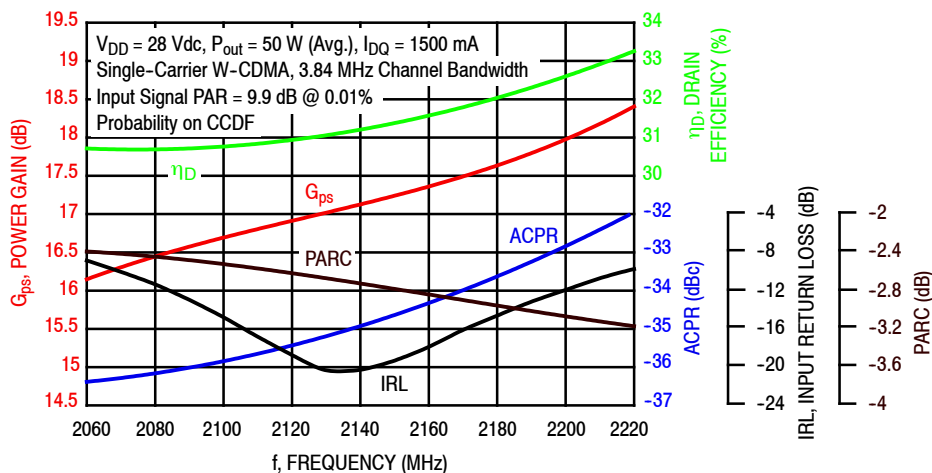


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 50$ Watts Avg.

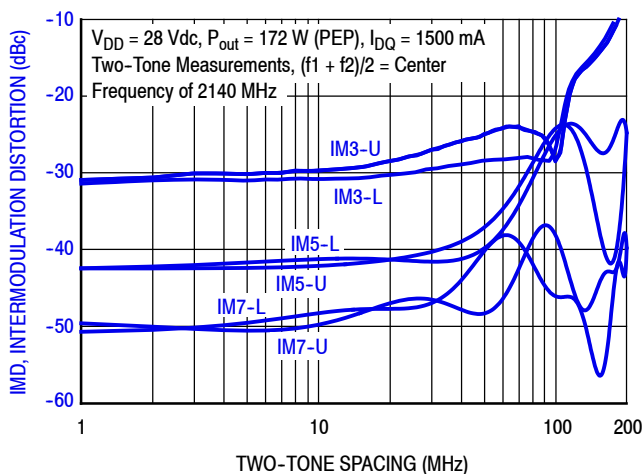


Figure 5a. Intermodulation Distortion Products versus Two-Tone Spacing — AFT21S230S

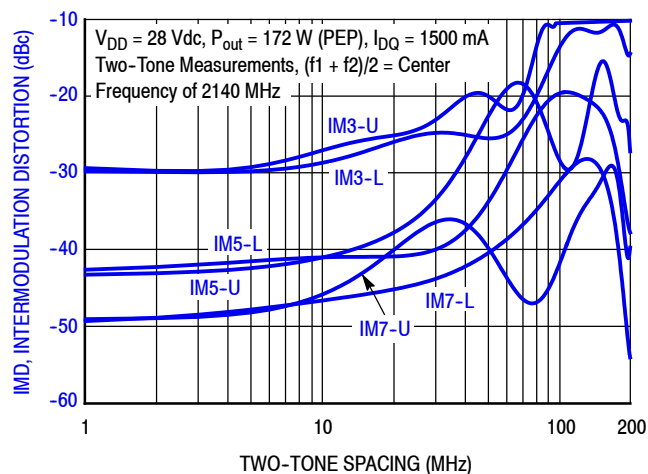


Figure 5b. Intermodulation Distortion Products versus Two-Tone Spacing — AFT21S232S

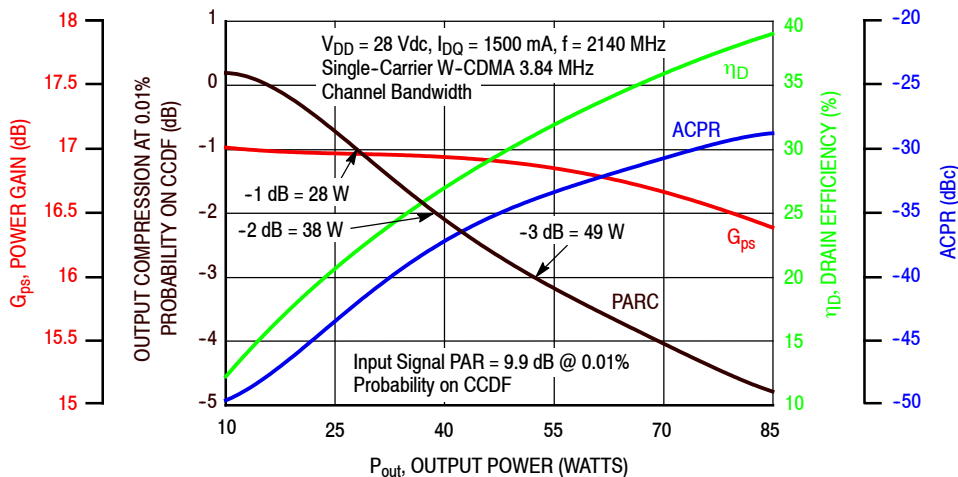


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

AFT21S230SR3 AFT21S232SR3

TYPICAL CHARACTERISTICS

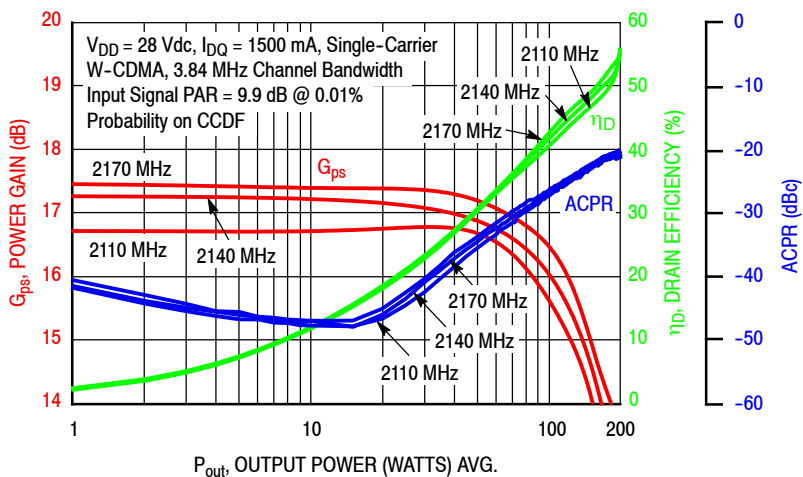


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

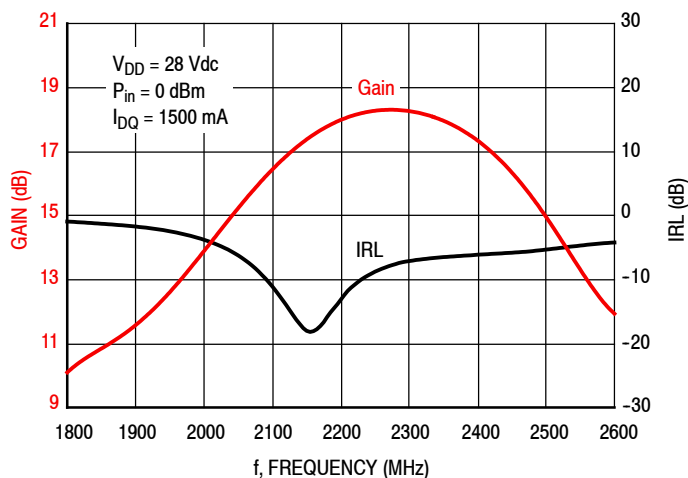


Figure 8. Broadband Frequency Response

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1500 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(on)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	$Z_{\text{load}}^{(1)} (\Omega)$	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.20 - j6.00	1.20 + j5.90	1.50 - j3.90	17.7	54.3	269	55.4	11	55.2	331	57.0	16
2140	1.70 - j6.40	1.50 + j6.30	1.60 - j4.00	17.7	54.3	269	55.1	10	55.2	331	56.0	15
2170	1.70 - j6.80	1.75 + j6.70	1.50 - j4.00	17.8	54.3	269	54.7	11	55.2	331	56.0	16

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

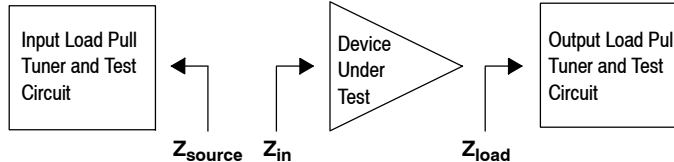


Figure 9. Load Pull Performance — Maximum P1dB Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1500 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(on)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	$Z_{\text{load}}^{(1)} (\Omega)$	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.20 - j6.00	1.20 + j5.93	2.10 - j2.41	20.0	52.7	186	64.9	16	54.3	269	66.2	20
2140	1.70 - j6.40	1.40 + j6.30	1.80 - j2.60	19.8	52.8	191	64.2	16	53.4	219	65.4	24
2170	1.70 - j6.80	1.80 + j6.80	1.70 - j2.60	20.0	52.8	191	64.2	17	54.2	263	65.5	22

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

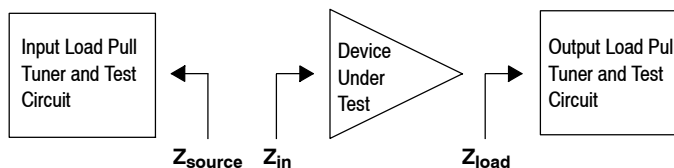


Figure 10. Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

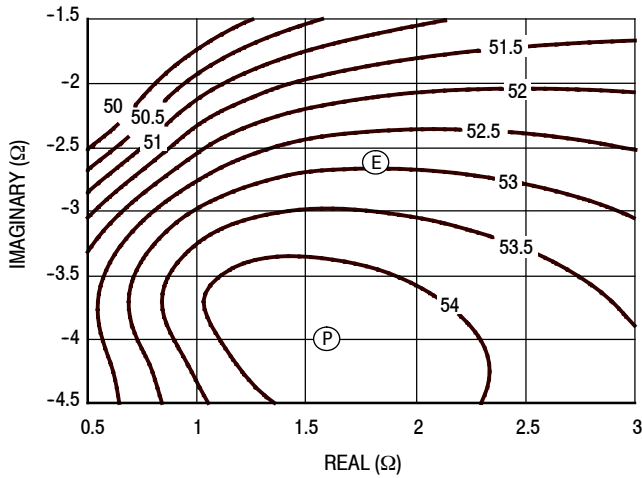


Figure 11. P1dB Load Pull Output Power Contours (dBm)

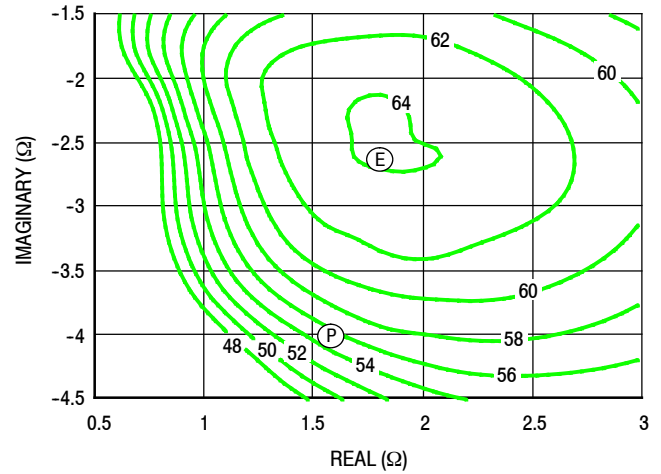


Figure 12. P1dB Load Pull Efficiency Contours (%)

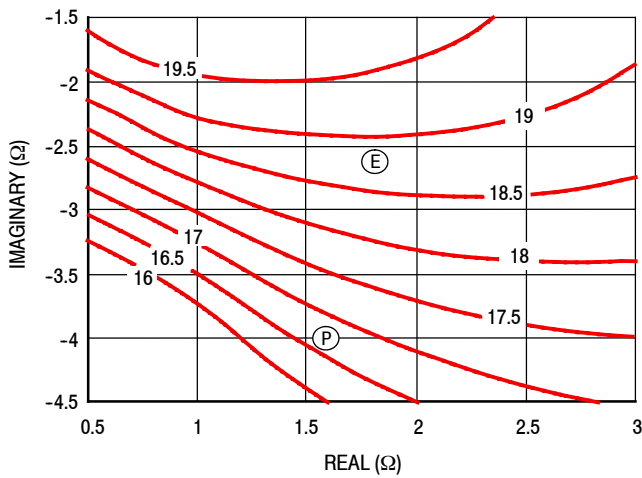


Figure 13. P1dB Load Pull Gain Contours (dB)

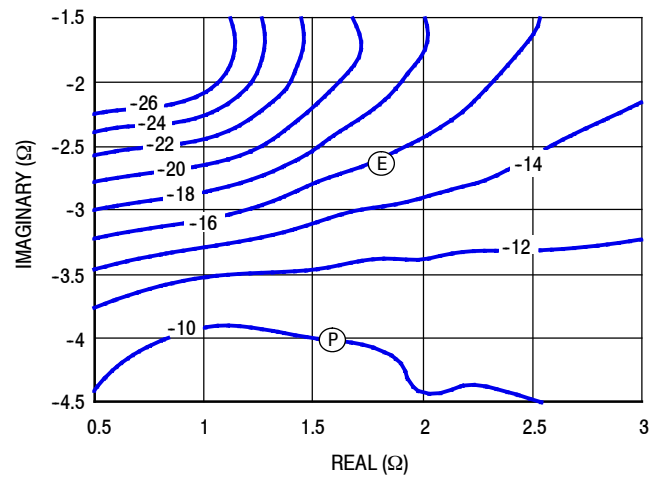


Figure 14. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Power Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

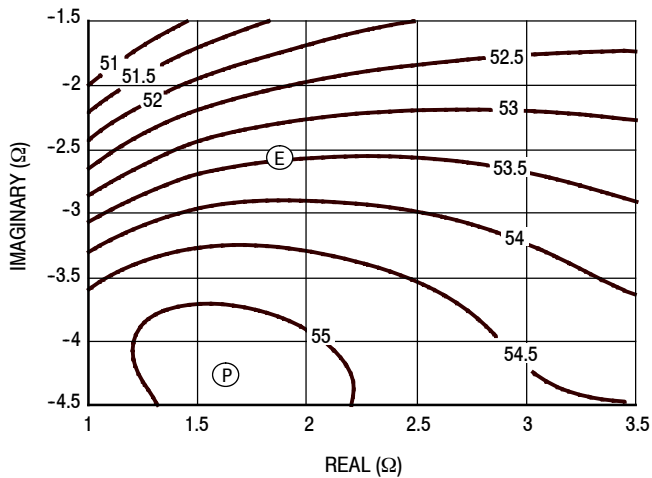


Figure 15. P3dB Load Pull Output Power Contours (dBm)

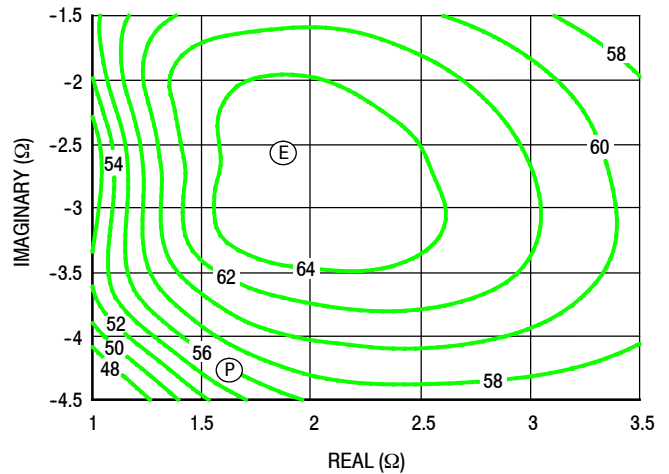


Figure 16. P3dB Load Pull Efficiency Contours (%)

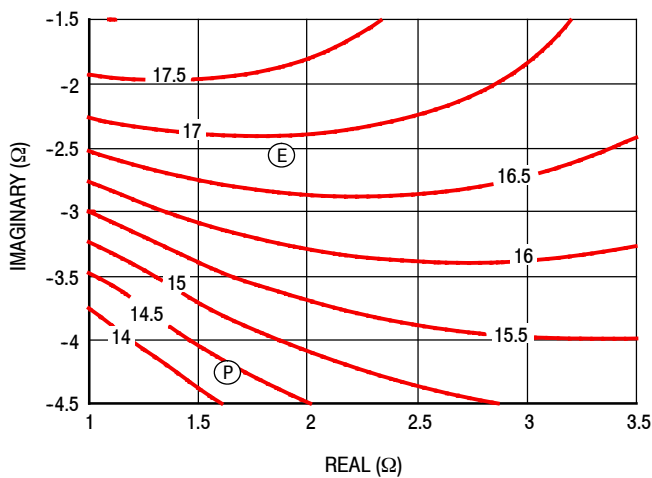


Figure 17. P3dB Load Pull Gain Contours (dB)

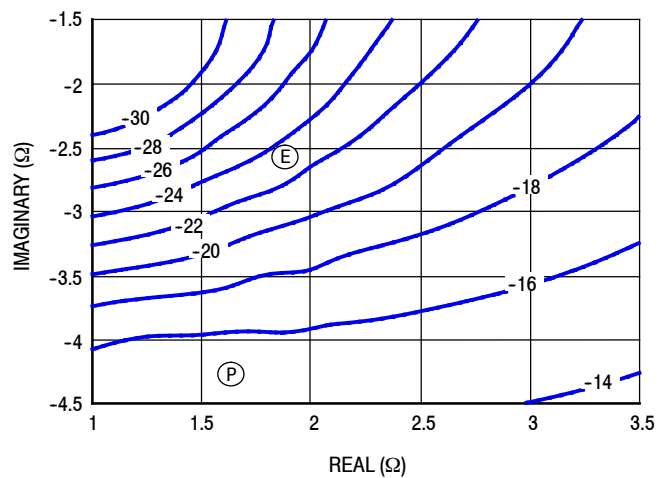
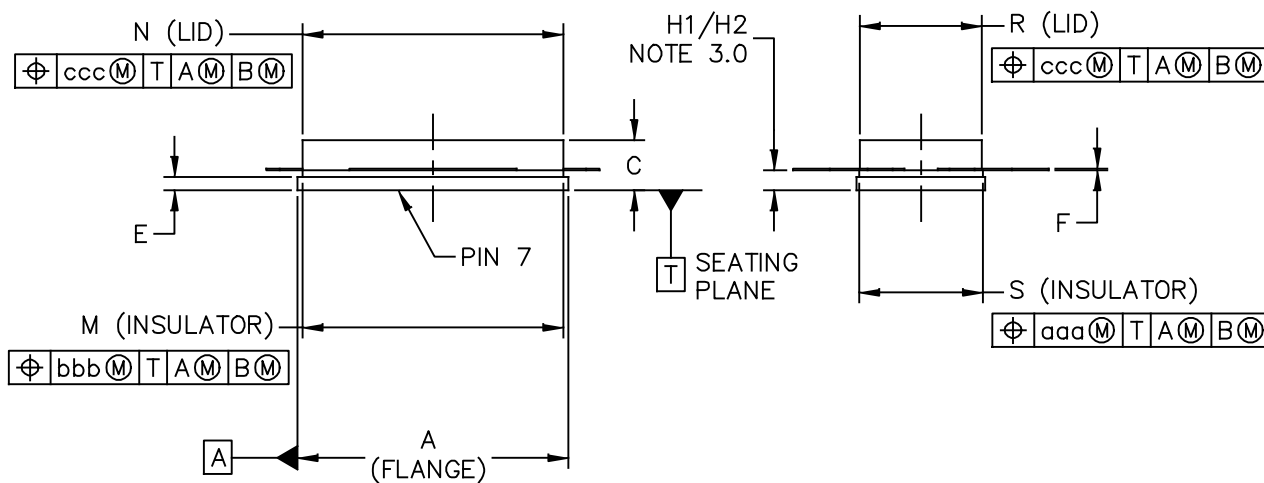
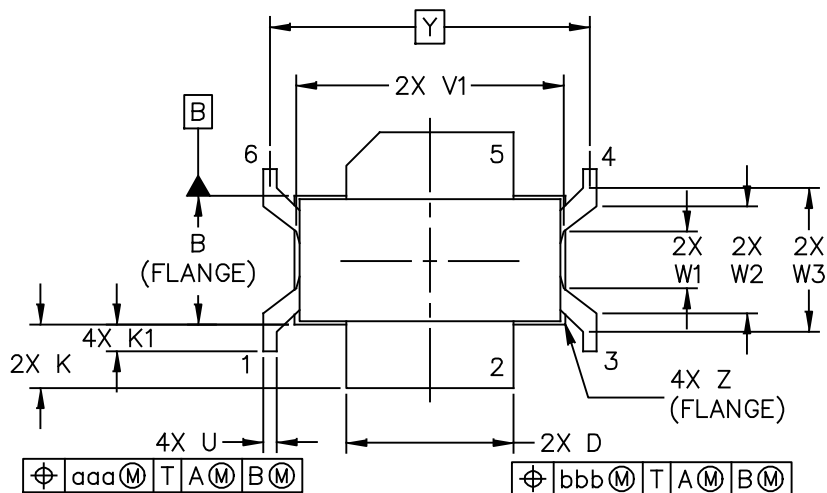


Figure 18. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Power Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: NI-780S-6		DOCUMENT NO: 98ASA00443D		REV: A	
		CASE NUMBER: 2268-02		24 MAY 2012	
		STANDARD: NON-JEDEC			

NOTES:

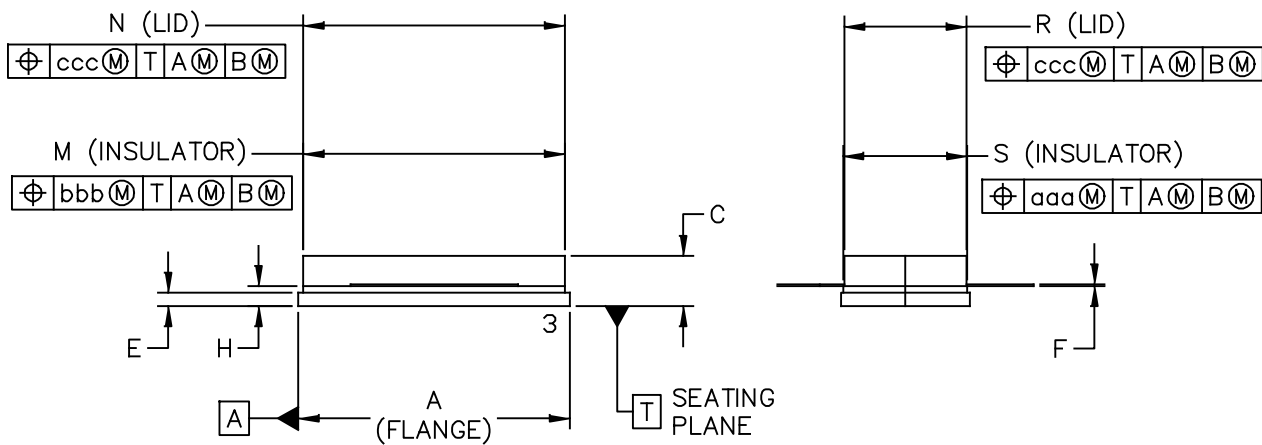
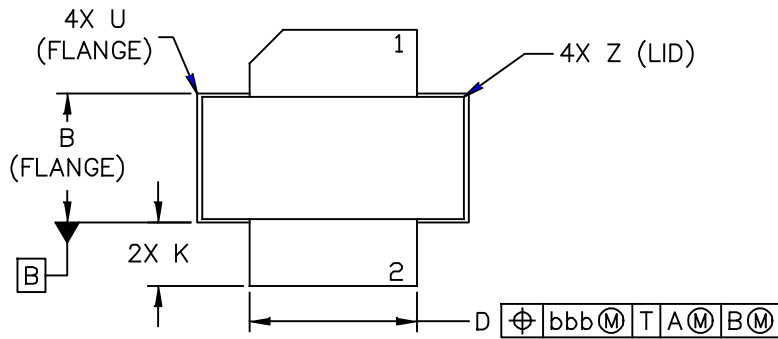
1.0 CONTROLLING DIMENSION: INCH.

2.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3.0 DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2 & 5. H2 APPLIES TO PINS 1, 3, 4 & 6.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	– .815	20.45	– 20.70	R	.365	– .375	9.27	– 9.53
B	.380	– .390	9.65	– 9.91	S	.365	– .375	9.27	– 9.53
C	.125	– .170	3.18	– 4.32	U	.035	– .045	0.89	– 1.14
D	.495	– .505	12.57	– 12.83	V1	.795	– .805	20.19	– 20.45
E	.035	– .045	0.89	– 1.14	W1	.165	– .175	4.19	– 4.45
F	.004	– .007	0.10	– 0.18	W2	.315	– .325	8.00	– 8.26
H1	.057	– .067	1.45	– 1.70	W3	.425	– .435	10.80	– 11.05
H2	.054	– .070	1.37	– 1.78	Y	.956 BSC		24.28 BSC	
K	.170	– .210	4.32	– 5.33	Z	R.000 – R.040		R.00 – R1.02	
K1	.070	– .090	1.78	– 2.29	aaa	– .005	–	–	0.127 –
M	.774	– .786	19.66	– 19.96	bbb	– .010	–	–	0.254 –
N	.772	– .788	19.61	– 20.02	ccc	– .015	–	–	0.381 –

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: NI-780S-6			DOCUMENT NO: 98ASA00443D		REV: A
			CASE NUMBER: 2268-02		24 MAY 2012
			STANDARD: NON-JEDEC		



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-780S	DOCUMENT NO: 98ASB16718C	REV: H
	CASE NUMBER: 465A-06	31 MAR 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	-.815	20.45	20.7	U	-.040			1.02
B	.380	-.390	9.65	9.91	Z	-.030			0.76
C	.125	-.170	3.18	4.32	aaa	-.005		0.127	
D	.495	-.505	12.57	12.83	bbb	-.010		0.254	
E	.035	-.045	0.89	1.14	ccc	-.015		0.381	
F	.003	-.006	0.08	0.15	-				
H	.057	-.067	1.45	1.7	-				
K	.170	-.210	4.32	5.33	-				
M	.774	-.786	19.61	20.02	-				
N	.772	-.788	19.61	20.02	-				
R	.365	-.375	9.27	9.53	-				
S	.365	-.375	9.27	9.52	-				
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI-780S					DOCUMENT NO: 98ASB16718C			REV: H	
					CASE NUMBER: 465A-06			31 MAR 2005	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

NI-780S-6: R5 Suffix = 50 Units, 44 mm Tape Width, 13 inch Reel.

NI-780S-2: R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for AFT21S230S and AFT21S232S parts will be available for 2 years after release of AFT21S230S and AFT21S232S. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased this device in the R5 tape and reel option will be offered AFT21S230S and AFT21S232S in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2012	• Initial Release of Data Sheet
1	Nov. 2012	• Corrected Tape and Reel tape width from 32 mm to 44 mm, p. 1, 14

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo, Altivec, C-5, CodeTest, CodeWarrior, ColdFire, C-Ware, Energy Efficient Solutions logo, Kinetis, mobileGT, PowerQUICC, Processor Expert, QorIQ, Qorivva, StarCore, Symphony, and VortiQa are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast, BeeKit, BeeStack, ColdFire+, CoreNet, Flexis, MagniV, MXC, Platform in a Package, QorIQ Qonverge, QUICC Engine, Ready Play, SafeAssure, SMARTMOS, TurboLink, Vybrid, and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2012 Freescale Semiconductor, Inc.