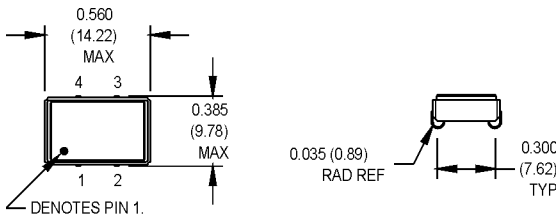
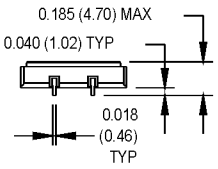
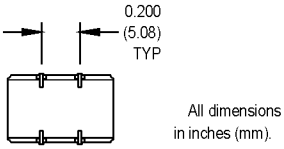
M5R Series

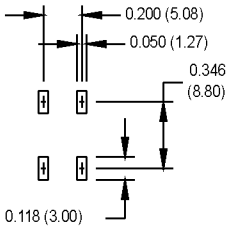
9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator

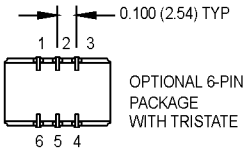


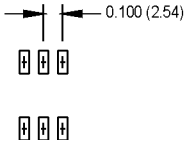




SUGGESTED SOLDER PAD LAYOUT







Pin Connections

FUNCTION	4 Pin	6 Pin
N/C or Output $\overline{Q}$	1	1
Enable		2
Ground/Cover	2	3
Output Q	3	4
N/C		5
+Vcc	4	6

Ordering Information

M5R 1 8 Z Q J -R 00.0000 MHz

Product Series

Temperature Range
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C
- **7:** -0°C to +85°C
- **8:** 0°C to +50°C

Stability
- **3:** ±100 ppm
- **4:** ±50 ppm
- **5:** ±35 ppm
- **6:** ±25 ppm
- **8:** ±20 ppm

Output Type
- **R:** Complementary Enable
- **T:** Single Enable
- **Z:** Complementary w/o Enable
- **X:** Single w/o Enable

Symmetry/Output Logic Type
- **L:** 45/55% LVDS
- **P:** 45/55% PECL
- **H:** 40/60% LVDS
- **Q:** 40/60% PECL

Package/Lead Configurations
- **J:** J-lead

RoHS Compliance
- **Blank:** non-RoHS compliant part
- **-R:** RoHS compliant part

Frequency (customer specified)

1. Calibration, deviation over temperature, shock, vibration, and aging.
2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	T_A	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year			±2	ppm		
Thereafter (per year)			±1	ppm		
Input Voltage	Vcc	3.135	3.3	3.465	V	
PECL Input Current	Icc			60	mA	0.75 to 24 MHz
				95	mA	24 to 96 MHz
				105	mA	96 to 800 MHz
LVDS Input Current	Icc			30	mA	0.75 to 24 MHz
				60	mA	24 to 800 MHz
Output Type						PECL/LVDS
Load		50 Ohms to Vcc -2 VDC 100 Ohm differential load				See Note 2 PECL Waveform LVDS Waveform
Symmetry (Duty Cycle)		(See Ordering Information)				@ Vcc-1.3 VDC (LVPECL) @ 50% of waveform (LVDS)
Output Skew				200	ps	PECL
Differential Voltage		250	340	450	mV	LVDS
Logic "1" Level	Voh	Vcc-1.02			V	PECL
Logic "0" Level	Vol			Vcc-1.63	V	PECL
Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		80% Vcc min. Or N/C: output active 20% Vcc max.: output disables to high-Z				"R" & "T" output types
Start up Time			5		ms	
Phase Jitter	ϕJ					Integrated 12 kHz - 20 MHz
≥20 MHz			3	5	ps RMS	

1. Calibration, deviation over temperature, shock, vibration, and aging.
2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.