

CMOS Ripple-Carry Binary Counter/Dividers

December 1992

Features

- High Voltage Types (20V Rating)
- Medium Speed Operation
- Fully Static Operation
- Buffered Inputs and Outputs
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- Common Reset
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of $1\mu\text{A}$ at 18V Over Full Package-Temperature Range;
 - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications For Description Of 'B' Series CMOS Devices"

Applications

- Control Counters
- Timers
- Frequency Dividers
- Time-Delay Circuits

Description

CD4020BMS - 14 Stage

CD4024BMS - 7 Stage

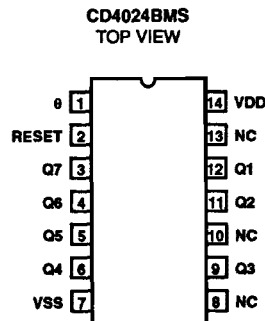
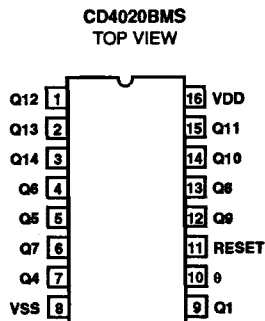
CD4040BMS - 12 Stage

CD4020BMS, CD4024BMS, and CD4040BMS are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

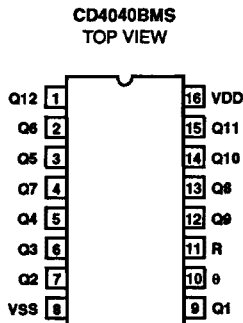
The CD4020BMS, CD4024BMS and the CD4040BMS is supplied in these 14 lead outline packages:

	CD4020B	CD4024B	CD4040B
Braze Seal DIP	H4W	H4Q	H4X
Frit Seal DIP	H1F	H1B	H1F
Ceramic Flatpack	H6W	H3W	H6W

Pinouts



NC = NO CONNECTION



7

LOGIC

Specifications CD4020BMS, CD4024BMS, CD4040BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) (Voltage Referenced to VSS Terminals)	-0.5V to +20V
Input Voltage Range, All Inputs	-0.5V to VDD +0.5V
DC Input Current, Any One Input	±10mA
Operating Temperature Range	-55°C to +125°C
Package Types D, F, K, H	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (During Soldering)	+265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum	

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W
Maximum Package Power Dissipation (PD) at +125°C		
For TA = -55°C to +100°C (Package Type D, F, K)	500mW	
For TA = +100°C to +125°C (Package Type D, F, K)	Derate	
	Linearity at 12mW/°C to 200mW	
Device Dissipation per Output Transistor	100mW	
For TA = Full Package Temperature Range (All Package Types)		
Junction Temperature	+175°C	

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

- NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
2. Go/No Go test with limits applied to inputs

Specifications CD4020BMS, CD4024BMS, CD4040BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay 0 To Q1	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	360	ns
				+125°C, -55°C	-	486	ns
Propagation Delay Qn To Qn + 1	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	330	ns
				+125°C, -55°C	-	446	ns
Propagation Delay Reset To Q	TPLH3 TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
				+125°C, -55°C	-	378	ns
Transition Time Q1	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
				+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
				+125°C, -55°C	2.22	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

Specifications CD4020BMS, CD4024BMS, CD4040BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH15	VDD = 15V, VO _{UT} = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VO _H > 9V, VO _L < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VO _H > 9V, VO _L < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Input To Q1	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay QN To QN + 1	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Propagation Delay Reset To Q	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	2, 3	+25°C	-	100	ns
		VDD = 15V	2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Reset Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Input Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

- All voltages referenced to device GND.
- The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
- CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VO _H > VDD/2	VO _L < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

Specifications CD4020BMS, CD4024BMS, CD4040BMS

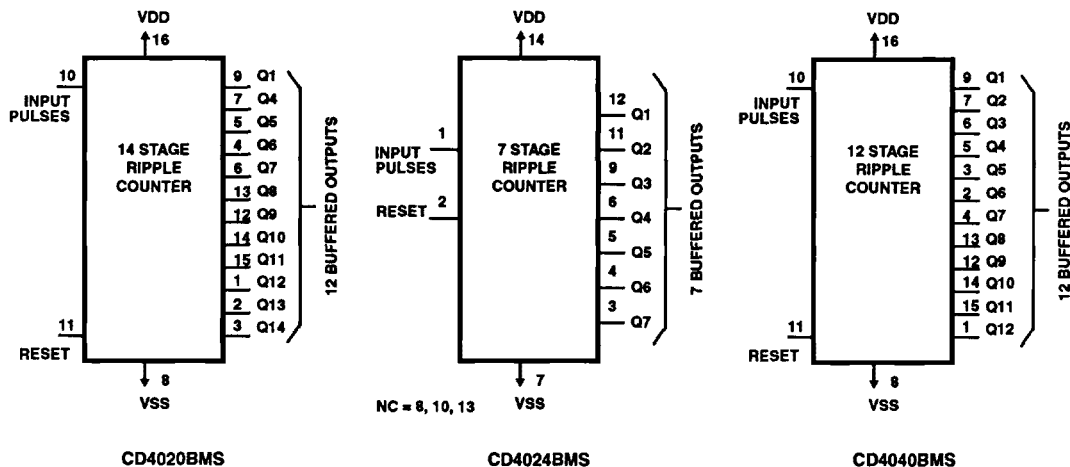
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4024BMS						
Static Burn-In 1 Note 1	3 - 6, 8 - 13	1, 2, 7	14			
Static Burn-In 2 Note 1	3 - 6, 8 - 13	7	1, 2, 14			
Dynamic Burn-In Note 1	8, 10, 13	2, 7	14	3 - 6, 9, 11, 12	1	
Irradiation Note 2	3 - 6, 8 - 13	7	1, 2, 14			
PART NUMBER CD4040BMS						
Static Burn-In 1 Note 1	1 - 7, 9, 12 - 15	8, 10, 11	16			
Static Burn-In 2 Note 1	1 - 7, 9, 12 - 15	8	10, 11, 16			
Dynamic Burn-In Note 1	-	8, 11	16	1 - 7, 9, 12 - 15	10	
Irradiation Note 2	1 - 7, 9, 12 - 15	8	10, 11, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$; VDD = $18V \pm 0.5V$
2. Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = $10V \pm 0.5V$

Functional Diagrams



Logic Diagrams

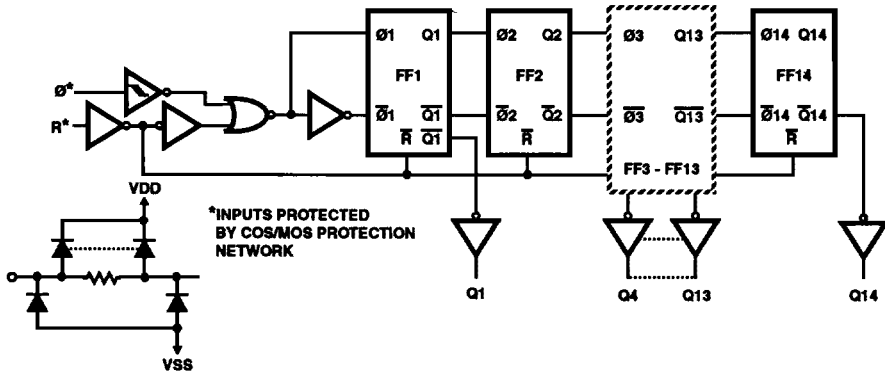


FIGURE 1. LOGIC DIAGRAM FOR CD4020BMS

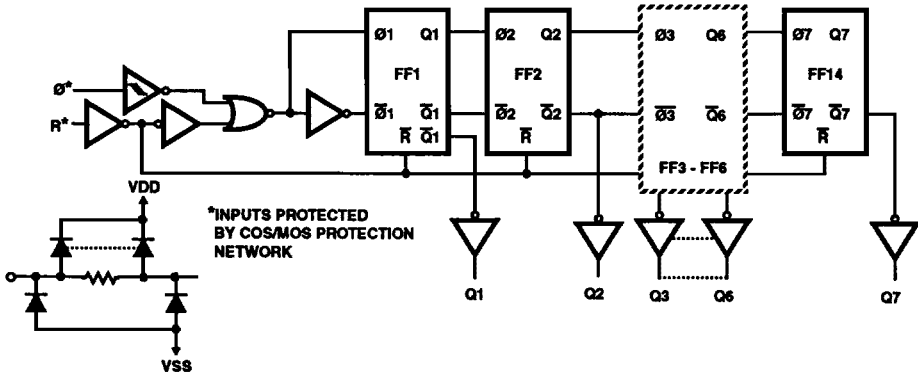


FIGURE 2. LOGIC DIAGRAM FOR CD4024BMS

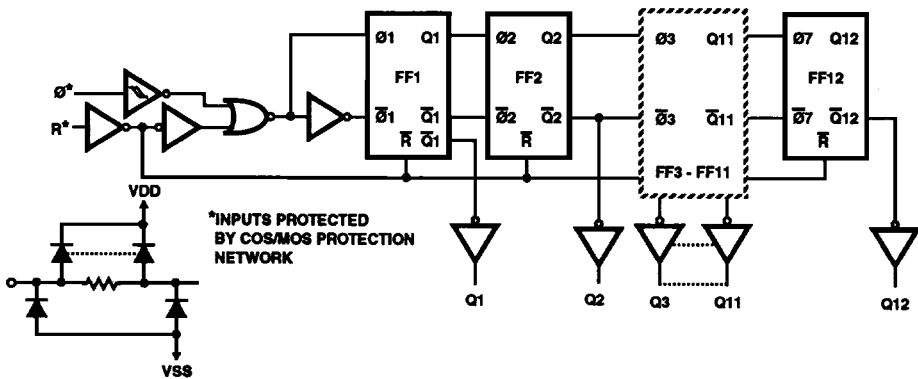


FIGURE 3. LOGIC DIAGRAM FOR CD4040BMS

Typical Performance Characteristics

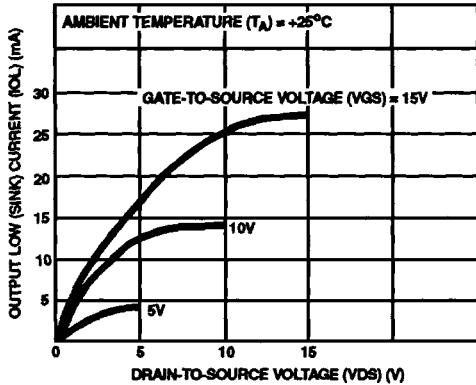


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

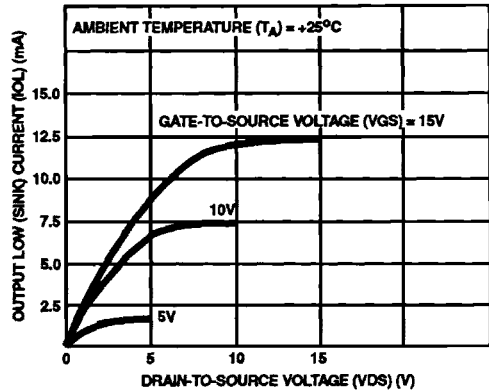


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

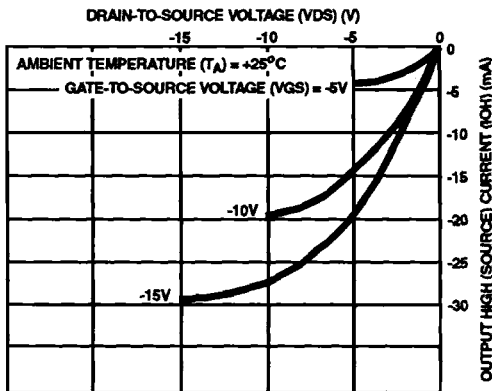


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

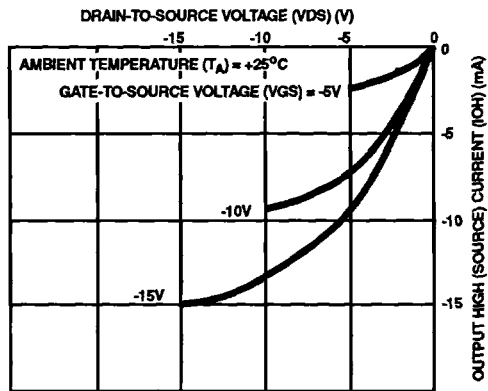


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

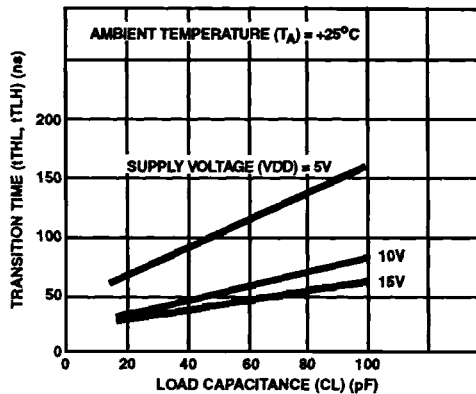


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

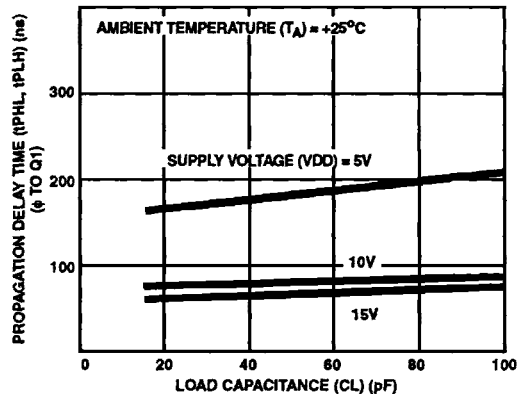


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (ϕ TO Q1)

Typical Performance Characteristics (Continued)

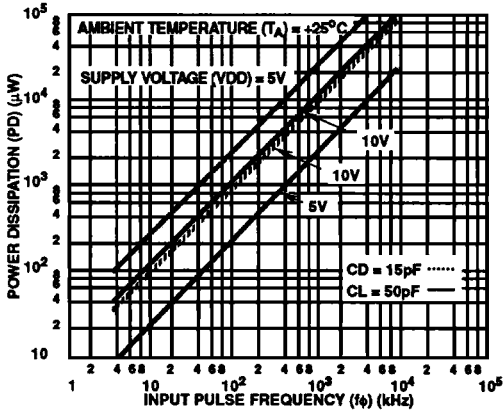
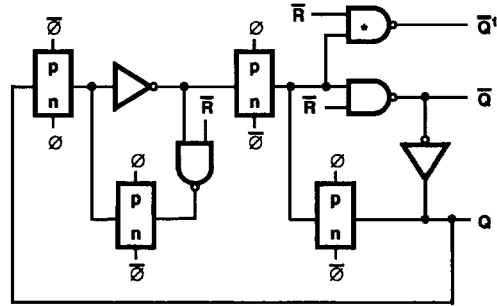


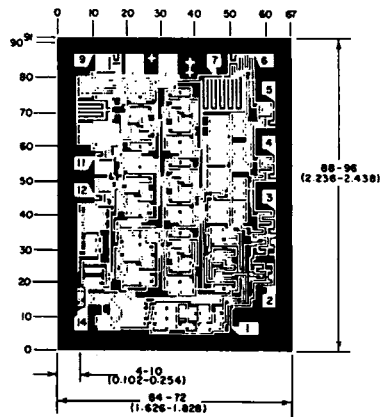
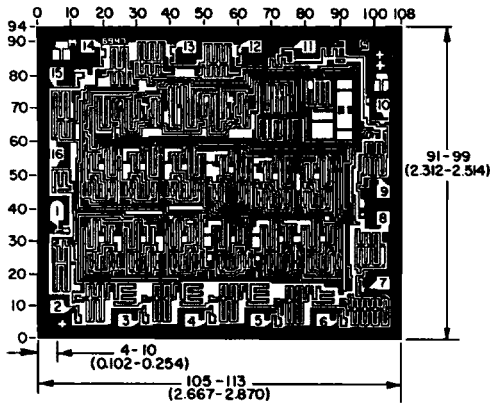
FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT PULSE FREQUENCY FOR CD4020BMS



* ON FIRST STAGE ONLY

FIGURE 11. DETAIL OF TYPICAL FLIP-FLOP STAGES

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

DIMENSIONS AND PAD LAYOUT FOR CD4020BMS. DIMENSIONS AND PAD LAYOUT FOR CD4040BMS ARE IDENTICAL

DIMENSIONS AND PAD LAYOUT FOR CD4024BMSH

- METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.
- PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane
- BOND PADS: 0.004 inches X 0.004 inches MIN
- DIE THICKNESS: 0.0198 inches - 0.0218 inches