

ADG819/ADG820**FEATURES**

Low On Resistance 0.8 Ω Max at 125°C
0.25 Ω Max On Resistance Flatness
1.8 V to 5.5 V Single Supply
200 mA Current Carrying Capability
Automotive Temperature Range: -40°C to +125°C
Rail-to-Rail Operation
6-Lead SOT-23 Package, 8-Lead μ SOIC Package, and
6-Bump MicroCSP (Micro Chip Scale Package) ADG819
Fast Switching Times
Typical Power Consumption (<0.01 μ W)
TTL-/CMOS-Compatible Inputs
Pin Compatible with the ADG719 (ADG819)

APPLICATIONS

Power Routing
Battery-Powered Systems
Communication Systems
Data Acquisition Systems
Cellular Phones
Modems
PCMCIA Cards
Hard Drives
Relay Replacement

GENERAL DESCRIPTION

The ADG819 and the ADG820 are monolithic, CMOS, SPDT (single-pole, double-throw) switches. These switches are designed on a submicron process that provides low power dissipation yet gives high switching speed, low On resistance, and low leakage currents.

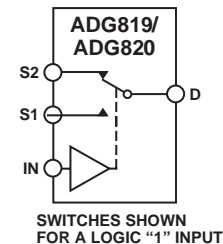
Low power consumption and an operating supply range of 1.8 V to 5.5 V make the ADG819 and ADG820 ideal for battery-powered, portable instruments.

Each switch of the ADG819 and the ADG820 conducts equally well in both directions when on. The ADG819 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG820 exhibits make-before-break action.

The ADG819 and the ADG820 are available in a 6-lead SOT-23 package and an 8-lead μ SOIC package. The ADG819 is also available in a 2 \times 3 bump 1.14 mm \times 2.18 mm MicroCSP package. This chip occupies only a 1.14 mm \times 2.18 mm area, making it the ideal candidate for space-constrained applications.

REV. 0

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FUNCTIONAL BLOCK DIAGRAM**PRODUCT HIGHLIGHTS**

1. Very low ON resistance, 0.5 Ω typical
2. 1.8 V to 5.5 V single-supply operation
3. High current carrying capability
4. Tiny 6-lead SOT-23 package, 8-lead μ SOIC package, and 2 \times 3 bump 1.14 mm \times 2.18 mm MicroCSP package (ADG819 only)

ADG819/ADG820—SPECIFICATIONS¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C ²	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
ON Resistance (R_{ON})	0.5			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$; Test Circuit 1
	0.6	0.7	0.8	Ω max	
ON Resistance Match Between Channels (ΔR_{ON})	0.06			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
	0.08	0.1	0.12	Ω max	
ON Resistance Flatness ($R_{FLAT(ON)}$)	0.1			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
	0.17	0.2	0.25	Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$; Test Circuit 2
	± 0.25	± 3	± 10	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01			nA typ	$V_S = V_D = 1\text{ V}$, or $V_S = V_D = 4.5\text{ V}$; Test Circuit 3
	± 0.25	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS³					
ADG819					
t_{ON}	35			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; Test Circuit 4
	45	50	55	ns max	
t_{OFF}	10			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; Test Circuit 4
	16	18	21	ns max	
Break-Before-Make Time Delay, t_{BBM}	5			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; Test Circuit 5
			1	ns min	
ADG820					
t_{ON}	10			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; Test Circuit 4
	18	20	22	ns max	
t_{OFF}	26			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; Test Circuit 4
	40	45	50	ns max	
Make-Before-Break Time Delay, t_{MBB}	15			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 0\text{ V}$; Test Circuit 6
			1	ns min	
Charge Injection	20			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 7
Off Isolation	-71			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 8
Channel-to-Channel Crosstalk	-72			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 10
Bandwidth -3 dB	17			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	80			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	300			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	2.0	μA max	

NOTES

¹Temperature range is as follows: -40°C to +125°C.

²ON resistance parameters tested with $I_S = 10\text{ mA}$.

³Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to }3.6\text{ V, GND} = 0\text{ V.}$)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C ²	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
ON Resistance (R_{ON})	0.7			Ω typ Ω max	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$; Test Circuit 1
ON Resistance Match Between Channels (ΔR_{ON})	0.06	1.5	1.6	Ω typ Ω max	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$
ON Resistance Flatness ($R_{FLAT(ON)}$)	0.25	0.13	0.13	Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.25	± 3	± 10	nA typ nA max	$V_{DD} = 3.6\text{ V}$ $V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$; Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.25	± 3	± 25	nA typ nA max	$V_S = V_D = 1\text{ V}$, or $V_S = V_D = 3.3\text{ V}$; Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS³					
ADG819					
t_{ON}	40			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$; Test Circuit 4
	60	65	70	ns max	
t_{OFF}	10			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$; Test Circuit
	16	18	21	ns max	
Break-Before-Make Time Delay, t_{BBM}	40			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 1.5\text{ V}$; Test Circuit 5
			1	ns min	
ADG820					
t_{ON}	20			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$; Test Circuit 4
	35	40	45	ns max	
t_{OFF}	30			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$; Test Circuit 4
	45	50	55	ns max	
Make-Before-Break Time Delay, t_{MBB}	10			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$; Test Circuit 6
			1	ns min	
Charge Injection	10			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 7
Off Isolation	-71			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 8
Channel-to-Channel Crosstalk	-72			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 10
Bandwidth -3 dB	17			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	80			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	300			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ μA max	$V_{DD} = 3.6\text{ V}$ Digital Inputs = 0 V or 3.6 V
		1.0	2.0		

NOTES

¹Temperature range is as follows: -40°C to +125°C.²ON resistance parameters tested with $I_S = 10\text{ mA}$.³Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG819/ADG820

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to GND	-0.3 V to +7 V
Analog Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	400 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	200 mA
Operating Temperature Range	
Industrial	-40°C to +85°C
Automotive	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
μSOIC Package	
θ _{JA} Thermal Impedance	206°C/W
θ _{JC} Thermal Impedance	44°C/W
SOT-23 Package (4-Layer Board)	
θ _{JA} Thermal Impedance	119°C/W

MicroCSP Package

θ _{JA} Thermal Impedance	TBD
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

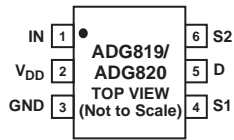
²Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table for the ADG819/ADG820

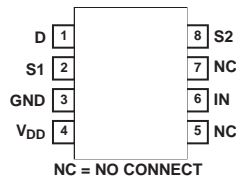
IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

PIN CONFIGURATIONS

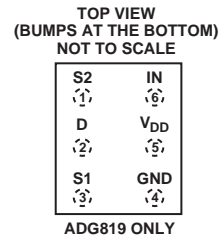
6-Lead SOT-23 (RJ-6)



8-Lead μSOIC (RM-8)



2 × 3 MicroCSP



ORDERING GUIDE

Model Option	Temperature Range	Brand ¹	Package Description	Package
ADG819BRM	-40°C to +125°C	SNB	μSOIC (MicroSmall Outline IC)	RM-8
ADG819BRT	-40°C to +125°C	SNB	SOT-23 (Plastic Surface-Mount)	RJ-6 ²
ADG819BCB	-40°C to +85°C	SNB	MicroCSP (Micro Chip Scale Package)	CB-6 ²
ADG820BRM	-40°C to +125°C	SPB	μSOIC (MicroSmall Outline IC)	RM-8
ADG820BRT	-40°C to +125°C	SPB	SOT-23 (Plastic Surface-Mount)	RJ-6 ²

NOTES

¹Branding on these packages is limited to three characters due to space constraints.

²Contact factory for availability.

TERMINOLOGY

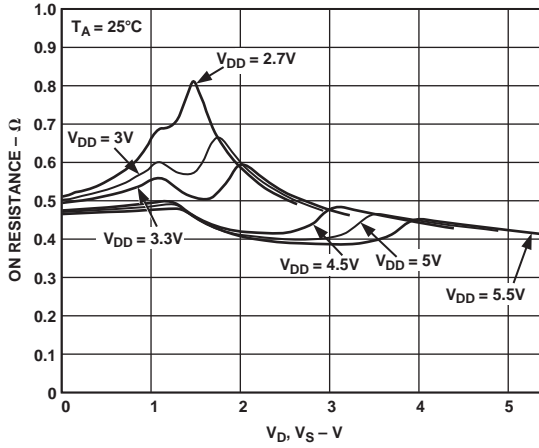
V_{DD}	Most Positive Power Supply Potential
GND	Ground (0 V) Reference
I_{DD}	Positive Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	ON Resistance Match between Any Two Channels, i.e., $R_{ON\ max} - R_{ON\ min}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of ON resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch OFF
I_D, I_S (ON)	Channel Leakage Current with the Switch ON
V_D (V_S)	Analog Voltage on Terminals D, S
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
I_{INL} (I_{INH})	Input Current of the Digital Input
C_S (OFF)	OFF Switch Source Capacitance
C_D, C_S (ON)	ON Switch Capacitance
t_{ON}	Delay between applying the digital control input and the output switching ON.
t_{OFF}	Delay between applying the digital control input and the output switching OFF.
t_{BBM}	OFF time or ON time measured between the 90% points of both switches when switching from one address state to another.
t_{MBB}	ON time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.
OFF Isolation	A measure of unwanted signal coupling through an OFF switch.
Bandwidth	Frequency at which the output is attenuated by -3 dB.
ON Response	Frequency Response of the ON Switch
Insertion Loss	Loss due to the ON Resistance of the Switch

CAUTION

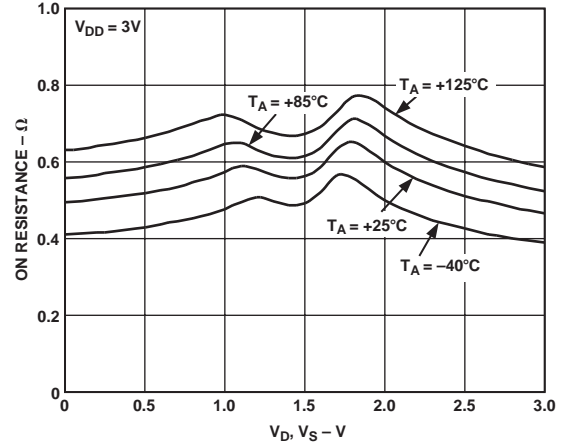
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG819/ADG820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



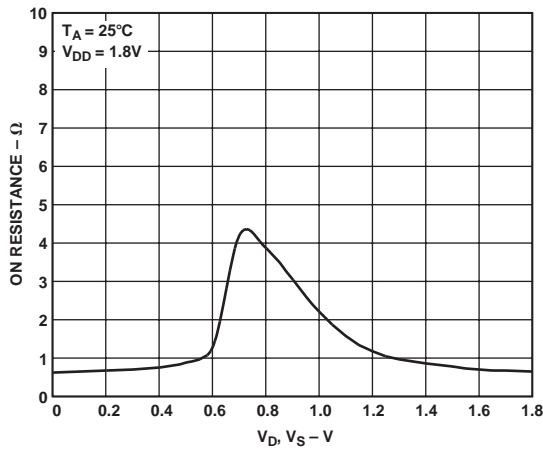
ADG819/ADG820 – Typical Performance Characteristics



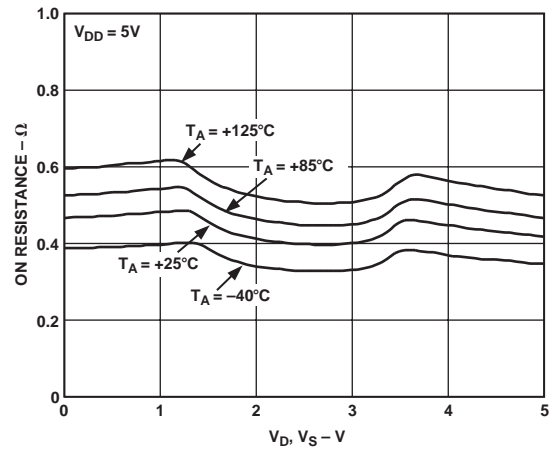
TPC 1. ON Resistance vs. V_D (V_S)



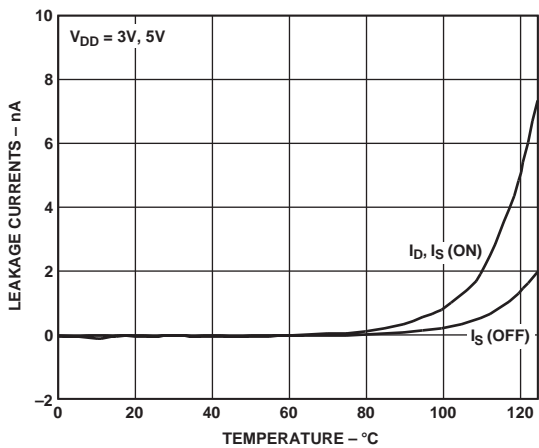
TPC 4. ON Resistance vs. V_D (V_S) for Different Temperatures



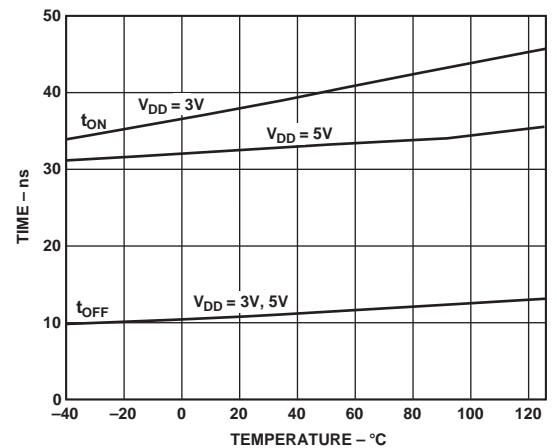
TPC 2. ON Resistance vs. V_D (V_S)



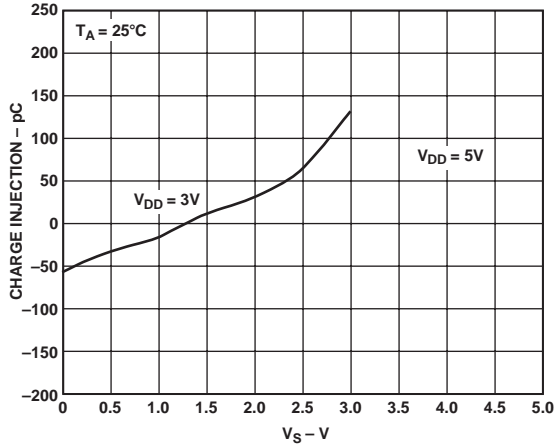
TPC 5. ON Resistance vs. V_D (V_S) for Different Temperatures



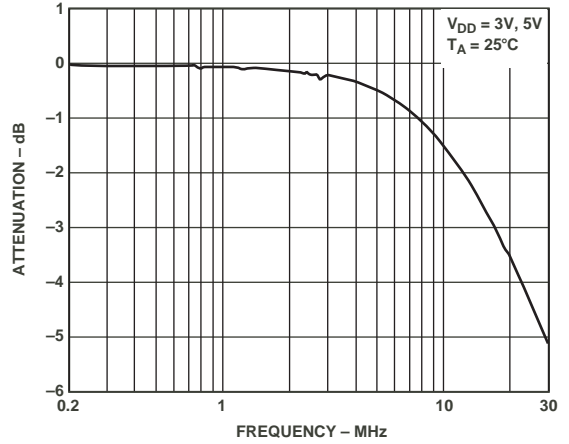
TPC 3. Leakage Currents vs. Temperatures



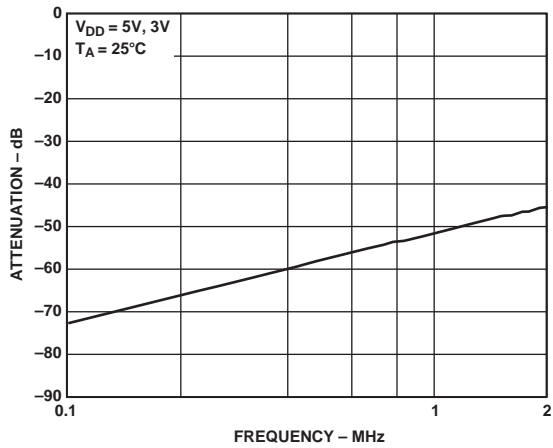
TPC 6. t_{ON}/t_{OFF} Times vs. Temperature (ADG819)



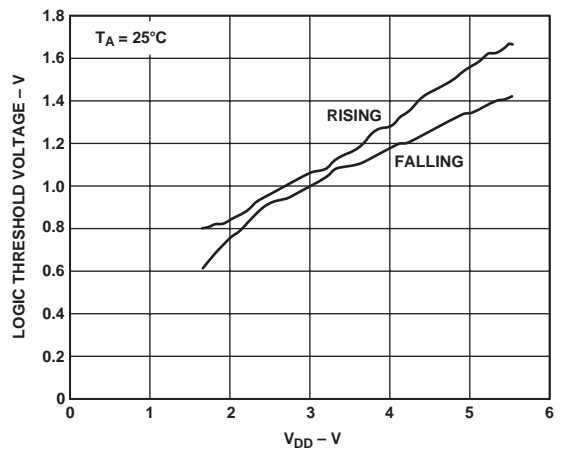
TPC 7. Charge Injection vs. Source Voltage



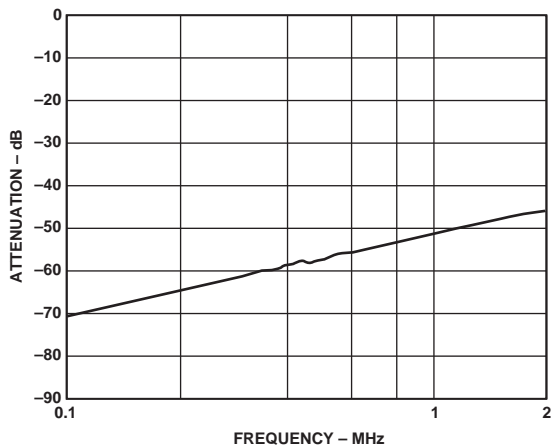
TPC 10. ON Response vs. Frequency



TPC 8. OFF Isolation vs. Frequency



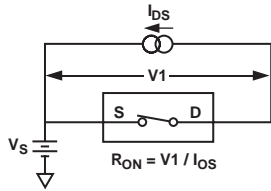
TPC 11. Logic Threshold vs. Supply Voltage



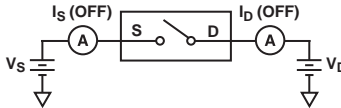
TPC 9. Crosstalk vs. Frequency

ADG819/ADG820

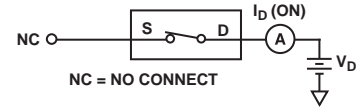
Test Circuits



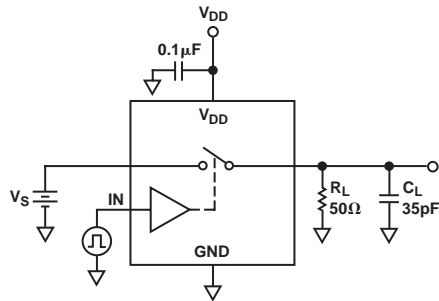
Test Circuit 1. ON Resistance



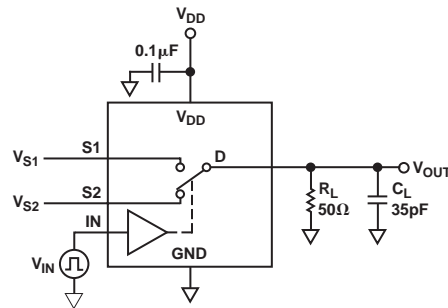
Test Circuit 2. OFF Leakage



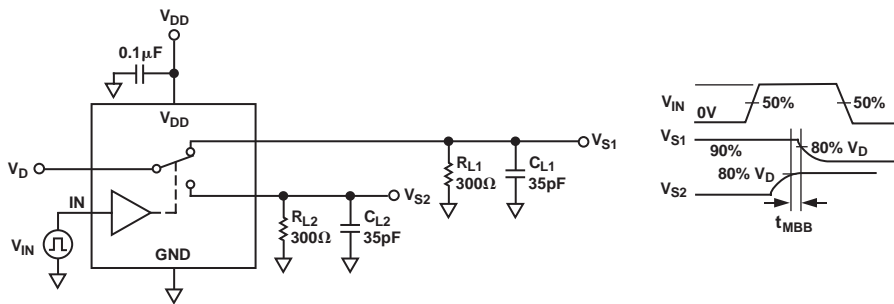
Test Circuit 3. ON Leakage



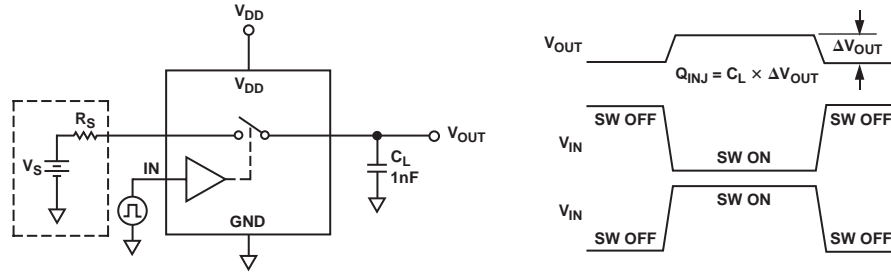
Test Circuit 4. Switching Times



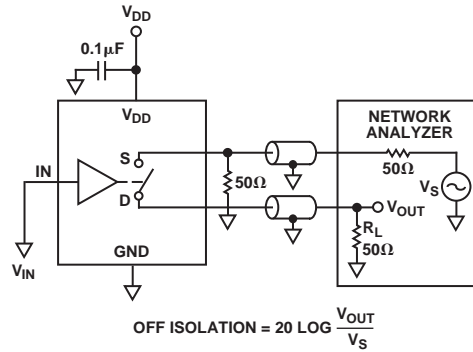
Test Circuit 5. Break-Before-Make Time Delay, t_{BBM} (ADG819 Only)



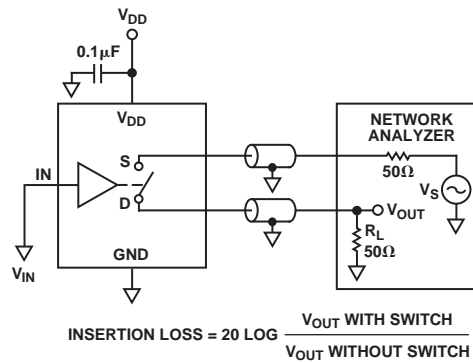
Test Circuit 6. Make-Before-Break Time Delay, t_{MBB} (ADG820 Only)



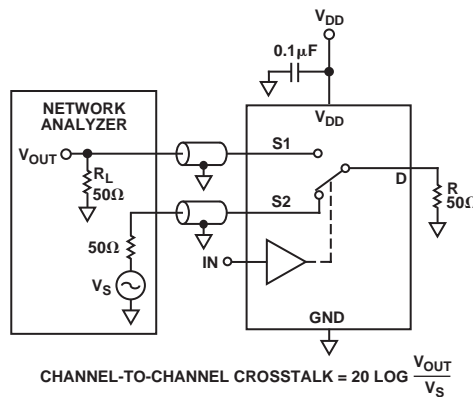
Test Circuit 7. Charge Injection



Test Circuit 8. OFF Isolation



Test Circuit 9. Bandwidth

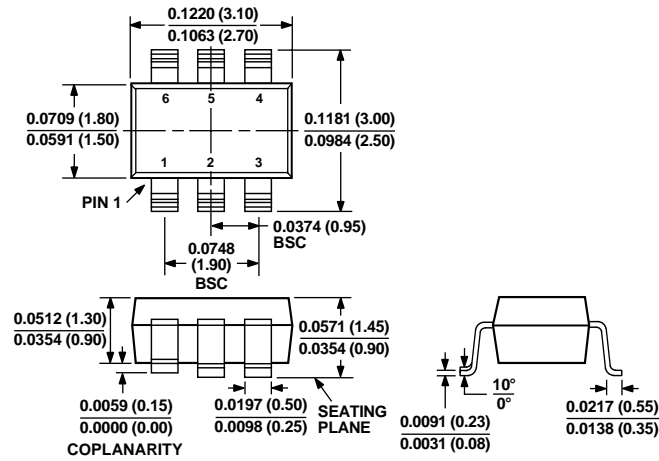


Test Circuit 10. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

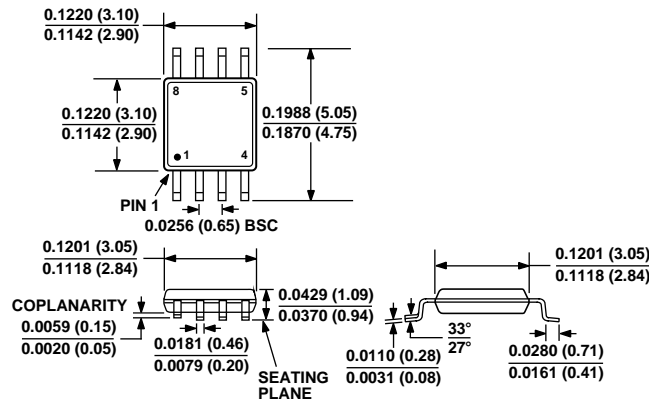
6-Lead Plastic Surface-Mount Package (RJ-6)

Dimensions shown in inches and (mm)



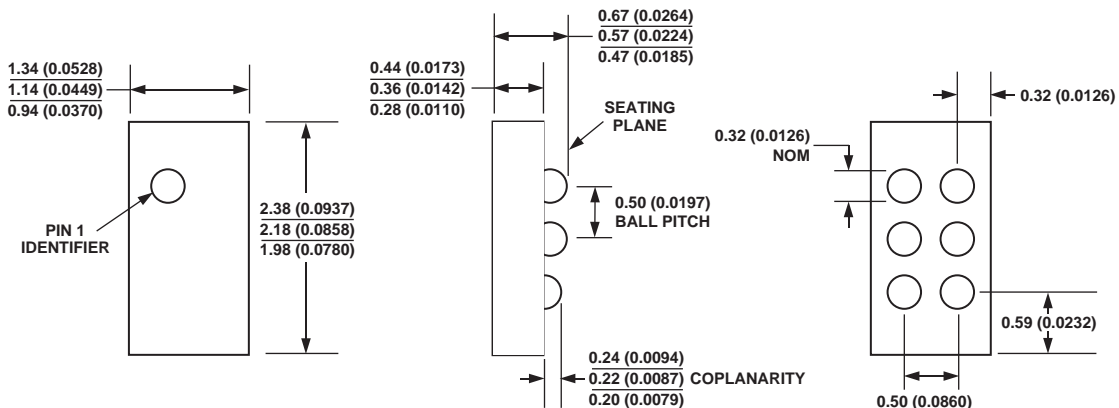
8-Lead μ SOIC Package (RM-8)

Dimensions shown in inches and (mm)



2 × 3 Array for MicroCSP (CB-6)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

