Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT 49C460
IDT 49C460A
IDT 49C460B
IDT 49C460C

T-45-17

FEATURES:

- Fast

	Detect	Correct
– IDT49C460C	16ns (max.)	24ns (max.)
– IDT49C460B	25ns (max.)	30ns (max.)
– IDT49C460A	30ns (max.)	36ns (max.)
– IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - – Commercial: 95mA (max.)
  - – Military: 125mA (max.)
- Improves system memory reliability
  - – Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - – Data words up to 64-bits
- Built-in diagnostics
  - – Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - – Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, PPGA, LCC, PLCC and Ceramic Quad Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, both ceramic and plastic, LCC (25 mil and 50 mil centers), PLCC and Ceramic Quad Flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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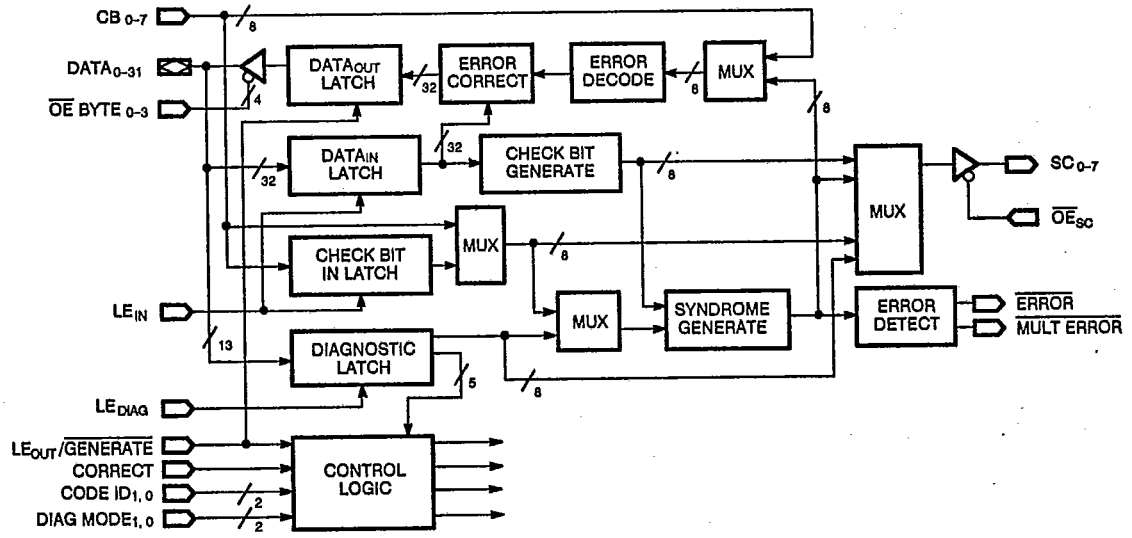
FUNCTIONAL BLOCK DIAGRAM



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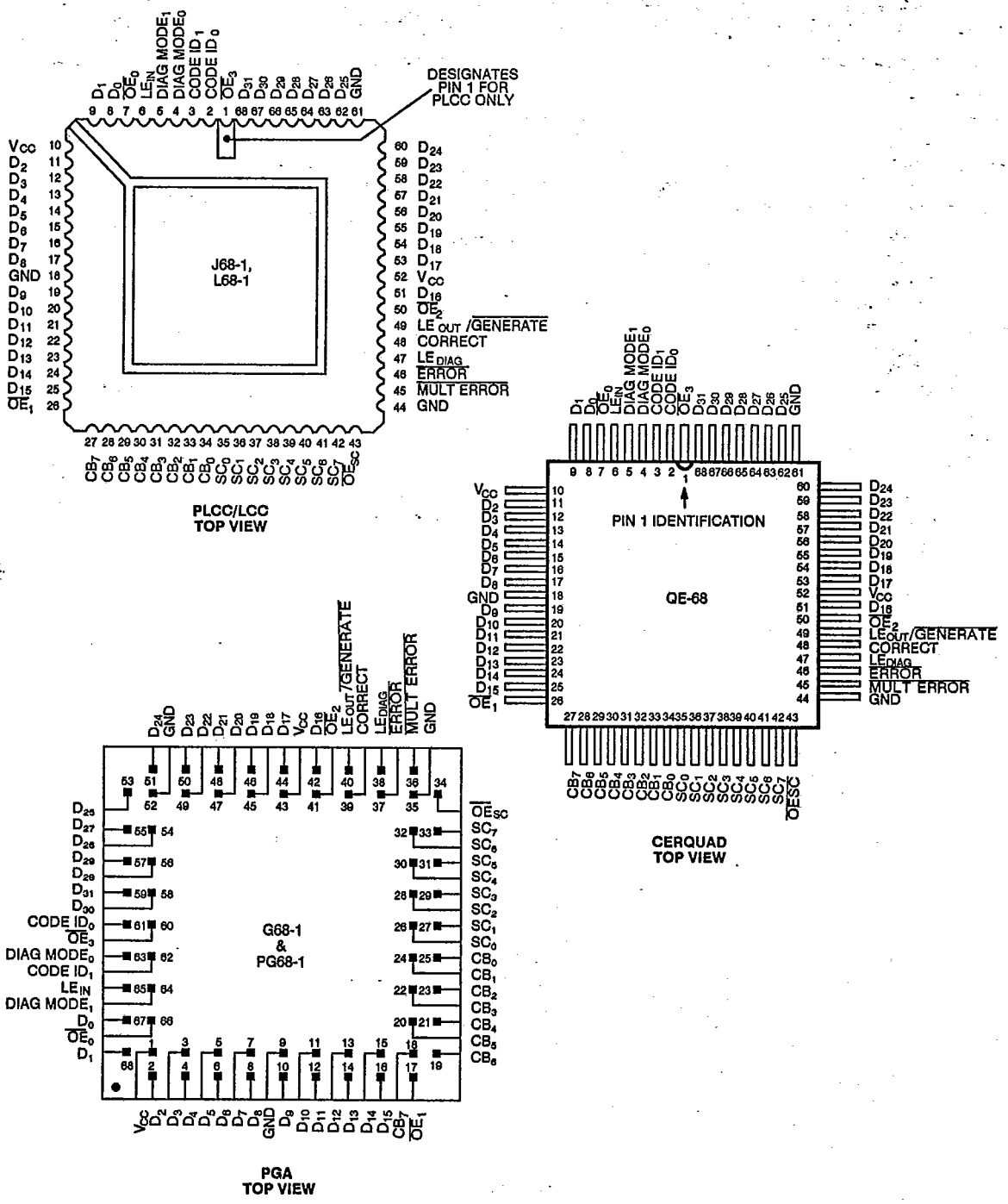
PIN CONFIGURATION



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PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-31}$	I/O	32 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines. Used to input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
$\overline{LE_{OUT}}$/ $\overline{GENERATE}$	I	A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE_{SC}}$	I	Output Enable – Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT\ ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}$ $BYTE_{0-3}$	I	Output Enable – Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
DIAG $MODE_{1,0}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
CODE $ID_{1,0}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE $ID_{1,0}$ input 01 is also used to instruct the EDC that the signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT.

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EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH:

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in another byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT INPUT LATCH:

Eight check bits are loaded under control of LE_{IN}. Check bits are used in the Error Detection and Error Correction modes.

CHECK BIT GENERATION LOGIC:

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC:

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits means the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC:

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs are HIGH. $\overline{\text{ERROR}}$ will go low if one error is detected. $\overline{\text{MULT ERROR}}$ and $\overline{\text{ERROR}}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC:

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS:

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch in the PASSTHRU mode. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH:

The diagnostic latch is loadable, under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC:

Specifies what mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{\text{GENERATE}}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

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DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

WORD SIZE SELECTION:

The 2 code identification pins, CODE $ID_{1,0}$ are used to determine the data word size that is 32 or 64 bits. Table 5 defines all possible slice identification codes. They also select the Internal Control Mode.

CHECK AND SYNDROME BITS:

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

C_0 C_1, C_2, C_3, C_4, C_5, C_6 for the 32-bit configuration
C_0 C_1, C_2, C_3, C_4, C_5, C_6, C_7 for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

TABLE 2.
DIAGNOSTIC MODE CONTROL

CORRECT	DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

TABLE 3.
IDT49C460 OPERATING MODES

OPERATING MODE	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	DATA OUT LATCH	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW(1)	Check Bits Generated from Data In Latch	High
Detect	0 0	0 1	1	0	Data In Latch	Syndrome Bits Data In/ Check Bit Latch	Error Dep(2)
Correct	0 0	0 1	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	Data In Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	–	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	Data In Latch	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	1	1	Data In Latch set to 0000	–	–
Internal Mode	CODE $ID_{1,0}$ = 01 (Control Signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$, and CORRECT are taken from Diagnostic Latch.)						

NOTES:
1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the Data Out Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate), does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

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OPERATING MODE SELECTION:

Tables 2 and 3 describe the 9 operating modes of the IDT49C460s. The Diagnostic Mode pins—DIAG $MODE_{0,1}$—define four basic areas of operation. GENERATE and CORRECT further divide operation into 8 functions, with CODE $ID_{1,0}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC_{0-7}. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs ERROR and MULT ERROR. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-7}. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG $MODE_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even CODE $ID_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

TABLE 5. SLICE IDENTIFICATION

CODE ID_1	CODE ID_0	SLICE SELECTED
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0-31)
1	1	64-Bit, Upper 32-Bit (32-63)

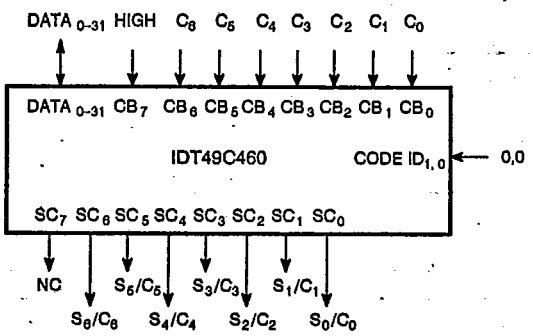

Figure 1. 32-Bit Configuration

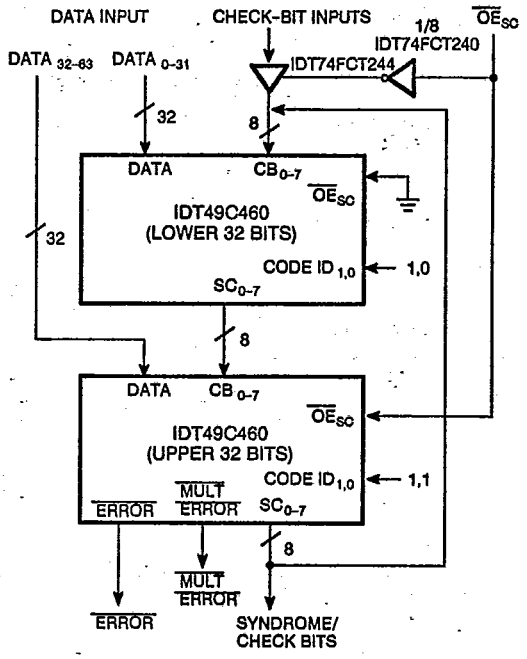

Figure 2. 64-Bit Configuration

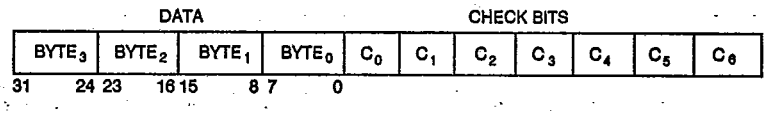

Figure 3. 32-Bit Data Format

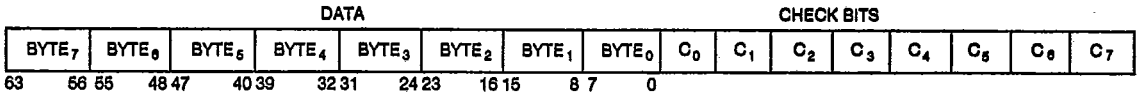

Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION:

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the Pass Thru or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 4 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

TABLE 4. 32-BIT DIAGNOSTIC LATCH CODING FORMAT

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13-31	DON'T CARE

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TABLE 6. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR (32-BIT)

					HEX	0	1	2	3	4	5	6	7
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

64-BIT DATA WORD CONFIGURATION:

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error correction and double bit error detection of a 64-bit data field. Table 5 gives the CODE $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE $ID_{1,0}$ = 11. Control signals not indicated are connected to both units in parallel. The EDC with the CODE $ID_{1,0}$ = 10 has the $\overline{OE}_{SC}$ grounded. The $\overline{OE}_{SC}$ selects the syndrome bits from the EDC with CODE $ID_{1,0}$ = 11 and also controls the check bit buffers from memory.

Data in bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE $ID_{1,0}$ = 10, while Data in bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE $ID_{1,0}$ = 11.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE $ID_{1,0}$ = 10 through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the upper EDC unit to the lower EDC unit. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

TABLE 8A.
64-BIT DIAGNOSTIC LATCH-CODING FORMAT (DIAGNOSTIC DETECT AND CORRECT MODE)

BIT	INTERNAL FUNCTION
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32-39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

TABLE 8B.
64-BIT DIAGNOSTIC LATCH—CODING FORMAT (DIAGNOSTIC GENERATE MODE)

BIT	INTERNAL FUNCTION
0-7	DON'T CARE
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

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TABLE 9. SYNDROME DECODE TO BIT-IN-ERROR (64-BIT CONFIGURATION)

					HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				SYNDROME BITS	S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

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TABLE 10.
KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FOR IDT49C460 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected DATA Out	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

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TABLE 11. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODING

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

SC OUTPUTS

The tables below indicate how the SC_{0-7} outputs are generated in each control mode for various CODE IDs (Internal Control Mode not applicable).

GENERATE	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0	PH1	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA	PA	PA ⊕ CB_1
$SC_2 \leftarrow$	PB	PB	PB ⊕ CB_2
$SC_3 \leftarrow$	PC	PC	PC ⊕ CB_3
$SC_4 \leftarrow$	PD	PD	PD ⊕ CB_4
$SC_5 \leftarrow$	PE	PE	PE ⊕ CB_5
$SC_6 \leftarrow$	PF	PF	PF ⊕ CB_6
$SC_7 \leftarrow$	–	PF	PG ⊕ CB_7
	FINAL CHECK BITS	PARTIAL CHECK BITS	FINAL CHECK BITS

CORRECT/ DETECT	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0 ⊕ C0	PH1 ⊕ C0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ C1	PA ⊕ C1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ C2	PB ⊕ C2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ C3	PC ⊕ C3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ C4	PD ⊕ C4	PC ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ C5	PE ⊕ C5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ C6	PF ⊕ C6	PF ⊕ CB_6
$SC_7 \leftarrow$	–	PF ⊕ C7	PG ⊕ CB_7
	FINAL SYNDROME	PARTIAL SYNDROME	FINAL SYNDROME

DIAGNOSTIC GENERATE	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	DL0	DL0	DL32
$SC_1 \leftarrow$	DL1	DL1	DL33
$SC_2 \leftarrow$	DL2	DL2	DL34
$SC_3 \leftarrow$	DL3	DL3	DL35
$SC_4 \leftarrow$	DL4	DL4	DL36
$SC_5 \leftarrow$	DL5	DL5	DL37
$SC_6 \leftarrow$	DL6	DL6	DL38
$SC_7 \leftarrow$	–	DL7	DL39
	FINAL CHECK BITS	PARTIAL CHECK BITS	FINAL CHECK BITS

DIAGNOSTIC CORRECT/ DETECT	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0 ⊕ DL0	PH1 ⊕ DL0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ DL1	PA ⊕ DL1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ DL2	PB ⊕ DL2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ DL3	PC ⊕ DL3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ DL4	PD ⊕ DL4	PD ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ DL5	PE ⊕ DL5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ DL6	PF ⊕ DL6	PF ⊕ CB_6
$SC_7 \leftarrow$	–	PF ⊕ DL7	PG ⊕ CB_7
	FINAL SYNDROME	PARTIAL SYNDROME	FINAL SYNDROME

PASSTHRU	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	C0	C0	CB_0
$SC_1 \leftarrow$	C1	C1	CB_1
$SC_2 \leftarrow$	C2	C2	CB_2
$SC_3 \leftarrow$	C3	C3	CB_3
$SC_4 \leftarrow$	C4	C4	CB_4
$SC_5 \leftarrow$	C5	C5	CB_5
$SC_6 \leftarrow$	C6	C6	CB_6
$SC_7 \leftarrow$	–	C7	CB_7

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DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE ID_1, 0 position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

SYNDROME DECODE TO BIT CORRECTED (32-BIT CONFIGURATION) CODE ID $_{1-0}$ = 00

					HEX	0	1	2	3	4	5	6	7
					S_6	0	0	0	0	1	1	1	1
	SYNDROME BITS				S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0									
0	0	0	0	0		–	–	–	–	–	–	–	30
1	0	0	0	1		–	–	–	14	–	–	–	–
2	0	0	1	0		–	–	–	–	–	2	24	–
3	0	0	1	1		–	18	8	–	–	–	–	–
4	0	1	0	0		–	–	–	15	–	3	25	–
5	0	1	0	1		–	19	9	–	–	–	–	31
6	0	1	1	0		–	20	10	–	–	–	–	–
7	0	1	1	1		–	–	–	–	–	4	26	–
8	1	0	0	0		–	–	–	–	–	5	27	–
9	1	0	0	1		–	21	11	–	–	–	–	–
A	1	0	1	0		–	22	12	–	1	–	–	–
B	1	0	1	1		17	–	–	–	–	6	28	–
C	1	1	0	0		–	23	13	–	–	–	–	–
D	1	1	0	1		–	–	–	–	–	7	29	–
E	1	1	1	0		16	–	–	–	–	–	–	–
F	1	1	1	1		–	–	–	–	0	–	–	–

NOTE:
1. S_7 = 1 in CODE $ID_{1,0}$ = 00

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

PA = D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D20 ⊕ D22 ⊕ D24 ⊕ D26 ⊕ D28

PB = D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D19 ⊕ D20 ⊕ D23 ⊕ D25 ⊕ D26 ⊕ D29 ⊕ D31

PC = D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D16 ⊕ D17 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D27 ⊕ D28 ⊕ D29

PD = D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D30 ⊕ D31

PE = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PF = D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PG = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23

PH0 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

PH1 = D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30

PH2 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D10 ⊕ D12 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D20 ⊕ D22 ⊕ D23 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

SYNDROME DECODE TO BIT CORRECTED (64-BIT CONFIGURATION)

					HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	–	C6	–	–	62	C7	–	–	46	–	–	–	–
1	0	0	0	1		C0	–	–	14	–	–	–	–	–	–	–	–	–	–	–	30
2	0	0	1	0		C1	–	–	–	–	34	56	–	–	50	40	–	–	–	–	–
3	0	0	1	1		–	18	8	–	–	–	–	–	–	–	–	–	–	2	24	–
4	0	1	0	0		C2	–	–	15	–	35	57	–	–	51	41	–	–	–	–	31
5	0	1	0	1		–	19	9	–	–	–	–	63	–	–	–	47	–	3	25	–
6	0	1	1	0		–	20	10	–	–	–	–	–	–	–	–	–	–	4	26	–
7	0	1	1	1		–	–	–	–	–	36	58	–	–	52	42	–	–	–	–	–
8	1	0	0	0		C3	–	–	–	–	37	59	–	–	53	43	–	–	–	–	–
9	1	0	0	1		–	21	11	–	–	–	–	–	–	–	–	–	–	5	27	–
A	1	0	1	0		–	22	12	–	33	–	–	–	49	–	–	–	–	6	28	–
B	1	0	1	1		17	–	–	–	–	38	60	–	–	54	44	–	1	–	–	–
C	1	1	0	0		–	23	13	–	–	–	–	–	–	–	–	–	–	7	29	–
D	1	1	0	1		–	–	–	–	–	39	61	–	–	55	45	–	–	–	–	–
E	1	1	1	0		16	–	–	–	–	–	–	–	–	–	–	–	0	–	–	–
F	1	1	1	1		–	–	–	–	32	–	–	–	48	–	–	–	–	–	–	–

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10% (Military)
V_{LO} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5.0	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10.0	µA
			V_O = V_{CC} (Max.)	–	0.1	10.0	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30.0	–	–	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

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DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0		–	3.0	5	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)(5)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	6	10	mA/ MHz
			COM'L.	–	6	7	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	60	110	mA
			COM'L.	–	60	80	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	70	125	
			COM'L.	–	70	95	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency in Megahertz.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

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IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460C over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT ERROR	TO OUTPUT MULT ERROR	UNITS
	$DATA_{0-31}$		19	24	16	20	ns
	CB_{0-7} (CODE ID 00, 11)		14	21	12	16	ns
	CB_{0-7} (CODE ID 10)		14	16	19	21	ns
	LE_{OUT}/GENERATE	↗	–	12	↘ 18	↘ 18	ns
		↘	18	–	↗ 18	↗ 18	ns
	CORRECT Not Internal Control Mode		–	16	–	–	ns
	DIAG MODE Not Internal Control Mode		16	26	16	20	ns
	$CODE\ ID_{1,0}$		18	23	17	21	ns
	LE_{IN} From latched to transparent	↗	22	28	24	22	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	15	24	15	19	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	16	22	15	18	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		15	25	13	16	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)	SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$	↘	LE_{IN}	3	4	ns
CB_{0-7}	↘	LE_{IN}	2	4	ns
$DATA_{0-31}$	↘	LE_{OUT}/GENERATE	6	0	ns
CB_{0-7} (CODE ID 00, 11)	↘	LE_{OUT}/GENERATE	14	0	ns
CB_{0-7} (CODE ID 10)	↘	LE_{OUT}/GENERATE	8	0	ns
CORRECT	↗ ↘	LE_{OUT}/GENERATE	8	–	ns
DIAG MODE	↘	LE_{OUT}/GENERATE	17	0	ns
$CODE\ ID_{1,0}$	↘	LE_{OUT}/GENERATE	10	0	ns
LE_{IN}	↗ ↘	LE_{OUT}/GENERATE	19	–	ns
$DATA_{0-31}$		LE_{DIAG}	3	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ BYTE$_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	6		ns

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IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT $\overline{ERROR}$	TO OUTPUT $\overline{MULT\ ERROR}$	UNITS
	$DATA_{0-31}$		25	30	25	27	ns
	CB_{0-7} (CODE ID 00, 11)		14	30	17	20	ns
	CB_{0-7} (CODE ID 10)		16	18	19	21	ns
	$LE_{OUT}/\overline{GENERATE}$	↘	–	12	↘ 23	↘ 23	ns
		↗	21	–	↗ 23	↗ 23	ns
	CORRECT Not Internal Control Mode		–	23	–	–	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	$CODE\ ID_{1,0}$		18	26	21	26	ns
	LE_{IN} From latched to transparent	↗	27	38	30	3	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	15	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	16	32	19	24	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		16	32	20	25	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	4	4	ns
CB_{0-7}		↘	LE_{IN}	4	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	11	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	20	–	ns
$DATA_{0-31}$			LE_{DIAG}	4	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}\ BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	9		ns

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IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT $\overline{ERROR}$	TO OUTPUT $\overline{MULT\ ERROR}$	UNITS
	$DATA_{0-31}$		28	33	28	30	ns
	CB_{0-7} (CODE ID 00, 11)		17	33	20	23	ns
	CB_{0-7} (CODE ID 10)		19	23	22	24	ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–	15	↘ 26	↘ 26	ns
		↘	24	–	↗ 26	↗ 26	ns
	CORRECT Not Internal Control Mode		–	26	–	–	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	$CODE\ ID_{1,0}$		21	29	24	29	ns
	LE_{IN} From latched to transparent	↗	30	41	33	36	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	18	32	22	25	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	19	35	22	27	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		19	35	23	28	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	4	4	ns
CB_{0-7}		↘	LE_{IN}	4	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	14	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	23	–	ns
$DATA_{0-31}$			LE_{DIAG}	4	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ BYTE$_{0-3}$	↘	↗	$DATA_{0-31}$	10	25	10	21	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	27	10	22	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

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IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT $\overline{ERROR}$	TO OUTPUT $\overline{MULT\ ERROR}$	UNITS
	$DATA_{0-31}$		27	36	30	33	ns
	CB_{0-7} (CODE ID 00, 11)		16	34	19	23	ns
	CB_{0-7} (CODE ID 10)		16	20	19	21	ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–	12	↘ 25	↘ 25	ns
		↘	21	–	↗ 25	↗ 25	ns
	CORRECT Not Internal Control Mode		–	23	–	–	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	$CODE\ ID_{1,0}$		18	26	21	26	ns
	LE_{IN} From latched to transparent	↗	27	38	30	33	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	15	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	16	32	29	24	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		16	32	20	25	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	5	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	11	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	25	–	ns
$DATA_{0-31}$			LE_{DIAG}	5	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}\ BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	9		ns

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IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT $\overline{ERROR}$	TO OUTPUT $\overline{MULT\ ERROR}$	UNITS
	$DATA_{0-31}$		30	39	33	36	ns
	CB_{0-7} (CODE ID 00, 11)		19	37	22	26	ns
	CB_{0-7} (CODE ID 10)		19	23	22	24	ns
	LE_{OUT}/GENERATE	↗	–	15	↘ 28	↘ 28	ns
		↘	24	–	↗ 28	↗ 28	ns
	CORRECT Not Internal Control Mode		–	26	–	–	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	$CODE\ ID_{1,0}$		21	29	24	29	ns
	LE_{IN} From latched to transparent	↗	30	41	33	36	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	18	32	22	25	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	19	35	22	27	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		19	35	23	28	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	5	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	LE_{OUT}/GENERATE	27	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	LE_{OUT}/GENERATE	18	0	ns
CB_{0-7} (CODE ID 10)		↘	LE_{OUT}/GENERATE	18	0	ns
CORRECT	↗	↘	LE_{OUT}/GENERATE	14	–	ns
DIAG MODE		↘	LE_{OUT}/GENERATE	20	0	ns
$CODE\ ID_{1,0}$		↘	LE_{OUT}/GENERATE	20	0	ns
LE_{IN}	↗	↘	LE_{OUT}/GENERATE	28	–	ns
$DATA_{0-31}$			LE_{DIAG}	5	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ BYTE $_{0-3}$	↘	↗	$DATA_{0-31}$	10	25	10	21	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	27	10	22	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

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IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT				UNITS
			SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$	
	$DATA_{0-31}$		37	49	40	45	ns
	CB_{0-7} (CODE ID 00, 11)		22	46	26	31	ns
	CB_{0-7} (CODE ID 10)		22	30	26	29	ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–	17	↘ 30	↘ 30	ns
		↘	29	–	↗ 30	↗ 30	ns
	CORRECT Not Internal Control Mode		–	31	–	–	ns
	DIAG MODE Not Internal Control Mode		23	35	27	33	ns
	$CODE\ ID_{1,0}$		25	35	29	35	ns
	LE_{IN} From latched to transparent	↗	37	51	41	45	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	21	38	26	30	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	22	42	26	33	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		22	42	27	34	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	6	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	30	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	16	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	31	–	ns
$DATA_{0-31}$			LE_{DIAG}	6	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ BYTE$_{0-3}$	↘	↗	$DATA_{0-31}$	10	27	10	23	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	28	10	24	ns

MINIMUM PULSE WIDTHS [1]

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

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IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT				UNITS
			SC_{0-7}	$DATA_{0-31}$	ERROR	MULT ERROR	
	$DATA_{0-31}$		40	52	44	48	ns
	CB_{0-7} (CODE ID 00, 11)		25	49	29	34	ns
	CB_{0-7} (CODE ID 10)		25	33	29	32	ns
	LE_{OUT}/GENERATE	↗	–	20	↘ 33	↘ 33	ns
		↘	32	–	↗ 33	↗ 33	ns
	CORRECT Not Internal Control Mode		–	34	–	–	ns
	DIAG MODE Not Internal Control Mode		26	38	30	36	ns
	$CODE\ ID_{1,0}$		28	38	32	38	ns
	LE_{IN} From latched to transparent	↗	40	54	44	48	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	24	42	29	33	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	25	47	29	36	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		25	47	30	37	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	6	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	LE_{OUT}/GENERATE	36	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	LE_{OUT}/GENERATE	24	0	ns
CB_{0-7} (CODE ID 10)		↘	LE_{OUT}/GENERATE	24	0	ns
CORRECT	↗	↘	LE_{OUT}/GENERATE	20	–	ns
DIAG MODE		↘	LE_{OUT}/GENERATE	28	0	ns
$CODE\ ID_{1,0}$		↘	LE_{OUT}/GENERATE	28	0	ns
LE_{IN}	↗	↘	LE_{OUT}/GENERATE	37	–	ns
$DATA_{0-31}$			LE_{DIAG}	6	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ $BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	29	10	25	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	30	10	26	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	15		ns

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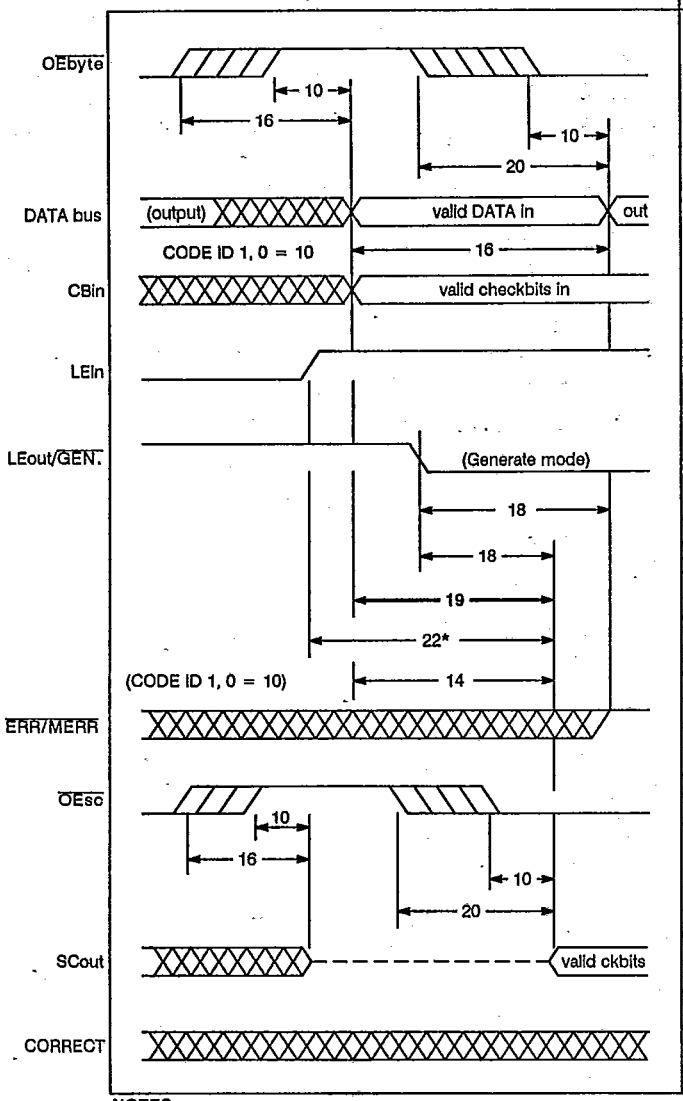
IDT49C460C TIMING: DATA SHEET PARAMETERS

GENERATE Mode (from DETECT or CORRECT Mode)



PROPAGATION DELAY FROM	TO	MIN./MAX.
$\overline{OEbyte}$ = High	to DATA out Disabled	Min.
$\overline{OEbyte}$ = High	to DATA out Disabled	Max.
$\overline{OEbyte}$ = Low	to DATA out Enabled	Min.
$\overline{OEbyte}$ = Low	to DATA out Enabled	Max.
CB in	to DATA out	Max.
(CODE ID 1, 0 = 10)		
LEout/$\overline{GENERATE}$ = Low	to $\overline{ERROR}$/$\overline{MERROR}$ = High	Max.
LEout/$\overline{GENERATE}$ = Low	to SC out	Max.
DATA in	**to SC out**	**Max.**
*LE in = High	to SC out*	Max.
CB in	to SC out	Max.
(forced high)		
$\overline{OEsc}$ = High	to SC out Disabled	Min.
$\overline{OEsc}$ = High	to SC out Disabled	Max.
$\overline{OEsc}$ = Low	to SC out Enabled	Min.
$\overline{OEsc}$ = Low	to SC out Enabled	Max.
(check bits exit)		
(don't care)		

NOTES:
1. BOLD indicates critical parameters.
2. Valid "DATA" and valid "CBin" are shown to occur simultaneously, since both busses are latched and opened by the "LEin" input.

*Assumes DATA bus becomes input 4ns before LEin goes high.

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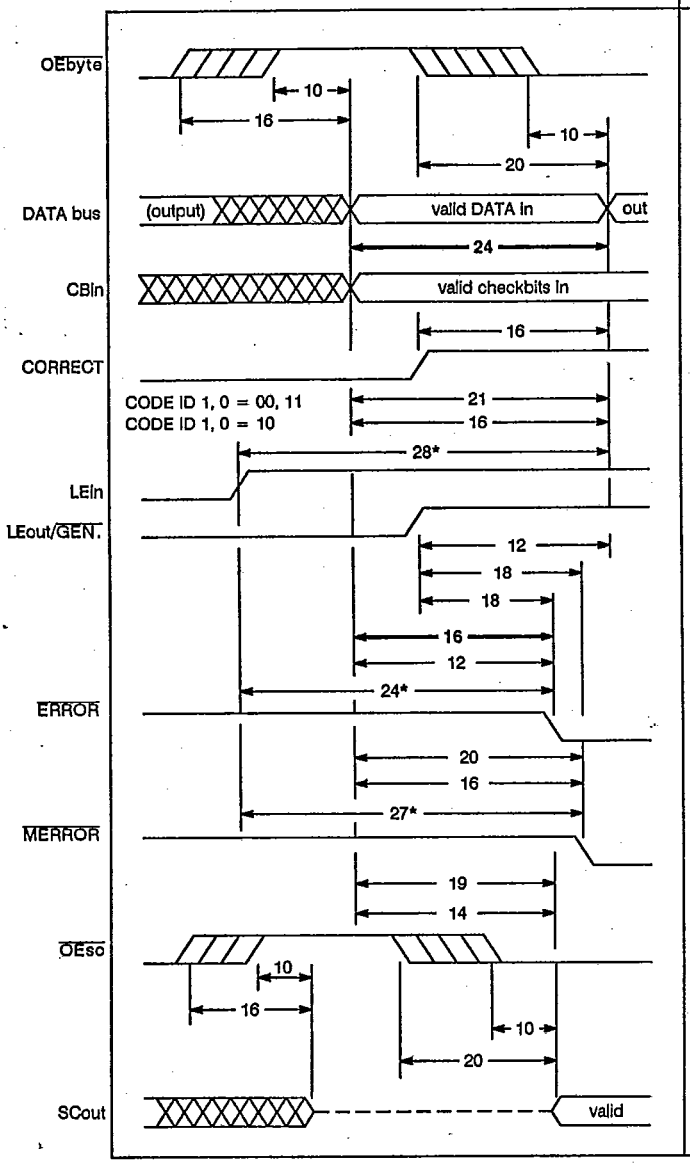
IDT49C460C TIMING: DATA SHEET PARAMETERS

DETECT or CORRECT Mode (from GENERATE Mode)



PROPAGATION DELAY FROM	TO	MIN./MAX.
$\overline{OEbyte}$ = High	to DATA out Disabled	Min.
$\overline{OEbyte}$ = High	to DATA out Disabled	Max.
$\overline{OEbyte}$ = Low	to DATA out Enabled	Min.
$\overline{OEbyte}$ = Low	to DATA out Enabled	Max.
(corrected DATA if Correct mode) (DATA in if Detect mode)		
DATA in	**to DATA out**	**Max.**
CB in	to DATA out	Max.
CORRECT = High	to DATA out	Max.
CB in	to DATA out	Max.
CB in	to DATA out	Max.
*LE in = High	to DATA out*	Max.
LEout/$\overline{GENERATE}$ = High	to DATA out	Max.
LEout/$\overline{GENERATE}$ = High	to $\overline{MERROR}$ = Low	Max.
LEout/$\overline{GENERATE}$ = High	to $\overline{ERROR}$ = Low	Max.
DATA in	**to $\overline{ERROR}$ = Low**	**Max.**
CB in	to $\overline{ERROR}$ = Low	Max.
*LE in = High	to $\overline{ERROR}$ = Low*	Max.
(Low = error)		
DATA in	to $\overline{MERROR}$ = Low	Max.
CB in	to $\overline{MERROR}$ = Low	Max.
*LE in = High	to $\overline{MERROR}$ = Low*	Max.
(Low = error)		
DATA in	to SC out	Max.
CB in	to SC out	Max.
$\overline{OEso}$ = High	to SC out Disabled	Min.
$\overline{OEso}$ = High	to SC out Disabled	Max.
$\overline{OEso}$ = Low	to SC out Enabled	Min.
$\overline{OEso}$ = Low	to SC out Enabled	Max.
(syndrome bits come out)		

NOTES:
1. BOLD indicates critical parameters.
*Assumes "CB in" and/or "DATA in" are valid at least 4ns before "LE in" goes high.

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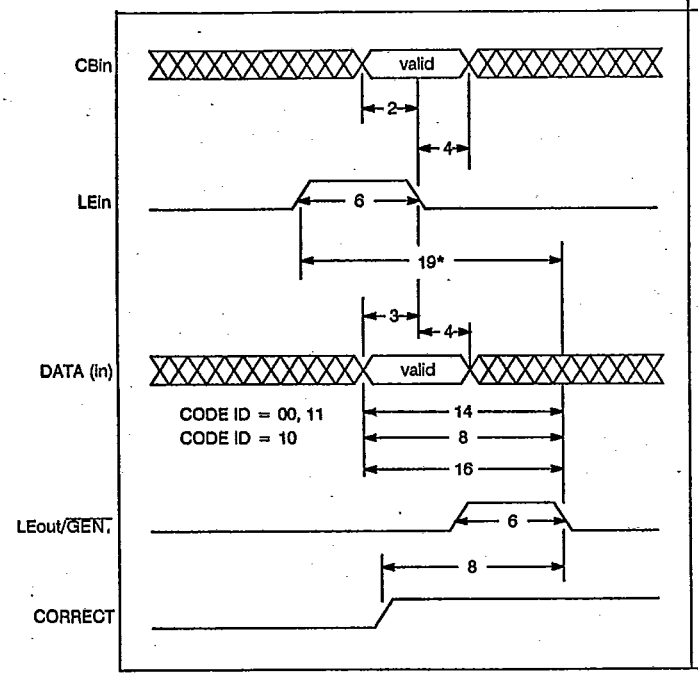
IDT49C460C TIMING: DATA SHEET PARAMETERS

SET-UP and HOLD Times and Minimum PULSE WIDTHS



SET-UP/HOLD TIME OF WITH RESPECT TO	MIN./MAX.
CB in Set-up to LE in = Low	Min.
CB in Hold to LE in = Low	Min.
LE in width	Min.
LE in = High to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
DATA Set-up to LE in = Low	Min.
DATA Hold to LE in = Low	Min.
CB in Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
CB in Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
DATA Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
LEout/$\overline{\text{GENERATE}}$ Width	Min.
CORRECT Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.

NOTES:

1. BOLD indicates critical parameters.

*Enable to enable timing requirement to ensure that the last DATA word applied to "DATA in" is made available as "DATA out"; assumes that "DATA in" is valid at least 4ns before "LE in" goes high.

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INPUT/OUTPUT INTERFACE CIRCUIT

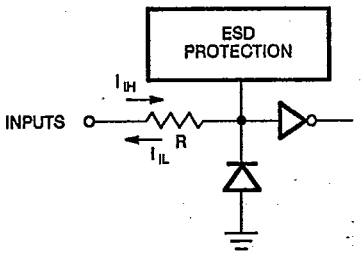

Figure 11. Input Structure (All Inputs)

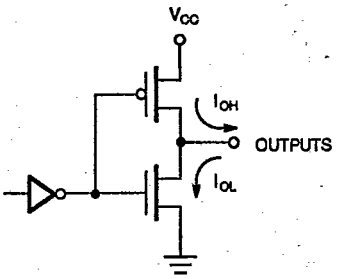

Figure 12. Output Structure

TEST LOAD CIRCUIT

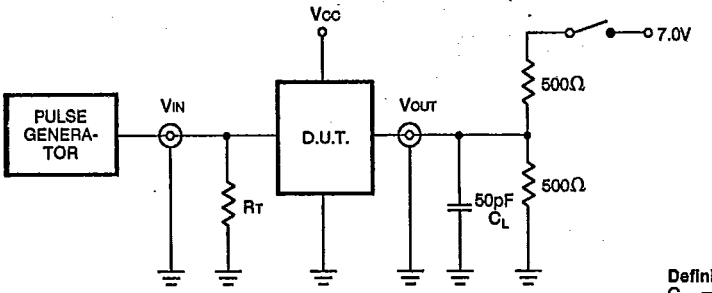

Figure 13.

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other outputs	Open

Definitions:
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of pulse generator.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 13

ORDERING INFORMATION

IDT — 49C460 (Device Type) — X (Speed) — X (Package) — X (Process/Temperature Range)

BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
L	Leadless Chip Carrier (50 mil centers)
G	Pin Grid Array
J	Plastic Leaded Chip Carrier
PG	Plastic Pin Grid Array
QE	Ceramic Quad Flat Pack
Blank	Standard Speed
A	High-Speed
B	Very High-Speed
C	Ultra-High-Speed
49C460	32-Bit E.D.C.