LC²MOS 16-Bit A/D Converter

AD7701

FEATURES
Monolithic 16-Bit ADC
0.0015% Linearity Error
On-Chip Self-Calibration Circuitry
Programmable Low Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS
Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

GENERAL DESCRIPTION

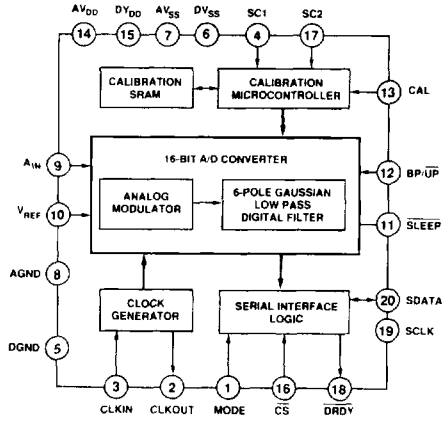
The AD7701 is a 16-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 16-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by a crystal-controlled on-chip clock oscillator.

The inherent linearity of the ADC is excellent, and end-point accuracy is ensured by self-calibration of zero and full-scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a flexible serial port, which has an asynchronous mode compatible with UARTs and two synchronous modes suitable for interfacing to shift registers or the serial ports of industry-standard microcontrollers.

CMOS construction insures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7701 offers 16-bit resolution coupled with outstanding 0.0015% accuracy.
2. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronous/asynchronous interface allows the AD7701 to interface directly to UARTs or to the serial ports of industry-standard microcontrollers.
5. Low operating power consumption and an ultralow power standby mode make the AD7701 ideal for loop-powered remote sensing applications, or battery-powered portable instruments.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = −5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; Bipolar Mode; MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN}, unless otherwise stated.)

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Integral Nonlinearity				
T_{min} to T_{max}		±0.0007	% FSR typ	
	±0.003	±0.0015	% FSR max	
Differential Nonlinearity				
T_{min} to T_{max}	±0.125	±0.125	LSB typ	Guaranteed No Missing Codes
	±0.5	±0.5	LSB max	
Positive Full-Scale Error[3]	±0.13	±0.13	LSB typ	
	±0.5	±0.5	LSB max	
Full-Scale Drift[4]	±1.2 (±2.3 S Version)	±1.2 (±2.3 T Version)	LSB typ	
Unipolar Offset Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Unipolar Offset Drift[4]	±1.6 (+3/−25 S Version)	±1.6 (+3/−25 T Version)	LSB typ	
Bipolar Zero Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Bipolar Zero Drift[4]	±0.8 (+1.5/−12.5 S Version)	±0.8 (+1.5/−12.5 T Version)	LSB typ	
Bipolar Negative Full-Scale Error[3]	±0.5	±0.5	LSB typ	
	±2	±2	LSB max	
Bipolar Negative Full-Scale Drift[4]	±0.6 (±1.2 S Version)	±0.6 (±1.2 T Version)	LSB typ	
Noise (Referred to Output)	0.1	0.1	LSB rms typ	
DYNAMIC PERFORMANCE				
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION				Applies to Unipolar and Bipolar Ranges. After Calibration, If $A_{IN} > V_{REF}$, the Device Will Output All 1s If $A_{IN} < 0$ (Unipolar) or $-V_{REF}$ (Bipolar), the Device Will Output All 0s.
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	
Negative Full-Scale Overrange	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Maximum Offset Calibration Range[5, 6]				
Unipolar Input Range	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Bipolar Input Range	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	V max	
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	V min	
	2 V_{REF} +0.2	2 V_{REF} +0.2	V max	
ANALOG INPUT				
Unipolar Input Range	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	Volts	
Input Capacitance	10	10	pF typ	
Input Bias Current[1]	1	1	nA typ	
LOGIC INPUTS				
All Inputs Except CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	
CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	V min	
I_{IN}, Input Current	10	10	μA max	
LOGIC OUTPUTS				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD}−1	DV_{DD}−1	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	±10	μA max	
Floating State Output Capacitance	9	9	pF typ	

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
POWER REQUIREMENTS[8]				
Power Supply Voltages				
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	Vmin/Vmax	
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	Vmin/Vmax	
Analog Negative Supply (AV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Digital Negative Supply (DV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Calibration Memory Retention				
Power Supply Voltage	2.0	2.0	V min	
DC Power Supply Currents[8]				
Analog Positive Supply (AI_{DD})	2.7	2.7	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	2	2	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	2.7	2.7	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]				
Positive Supplies	70	70	dB typ	
Negative Supplies	75	75	dB typ	
Power Dissipation				
Normal Operation	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]	20 (40 S Version)	20 (40 T Version)	μW max	$\overline{SLEEP}$ = Logic 0, Typically 10 μW

NOTES
[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency.
[2]Temperature ranges are as follows: A, B Versions; −40°C to +85°C; S, T Versions; −55°C to +125°C.
[3]Apply after calibration at the temperature of interest. Full-scale error applies for both unipolar and bipolar input ranges.
[4]Total drift over the specified temperature range since calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.
[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.
[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.
[7]For unipolar mode, input span is the difference between full-scale and zero scale. For bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF} + 0.1)$.
[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.
[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.
[10]CLKIN is stopped. All digital inputs are grounded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . . −0.3 V to +0.3 V
DV_{SS} to AGND . . . . . +0.3 V to −6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{SS} to AGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . . −0.3 V to DV_{DD} +0.3 V
Analog Input
Voltage to AGND . . . . . AV_{SS} −0.3 V to AV_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
Industrial Cerdip (A, B Versions) . . . . . −40°C to +85°C
Extended Cerdip (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

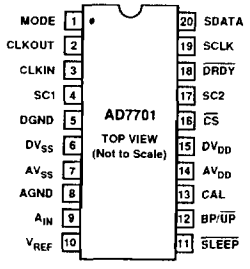
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to −5 V, the AD7701 will operate in the asynchronous communications (AC) mode. The SCLK pin is configured as an input, and data is transmitted in two bytes, each with one start bit and two stop bits. If MODE is tied to DGND, the synchronous external clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7701 operates in the synchronous self-clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty-cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is not connected.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, −5 V nominal.
7	AV_{SS}	Analog Negative Supply, −5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full-scale in the unipolar mode and of both positive and negative full-scale in the bipolar mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken low, the AD7701 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar Mode Pin. When this pin is low, the AD7701 is configured for a unipolar input range going from AGND to V_{REF}. When Pin 12 is high, the AD7701 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration Mode Pin. When CAL is taken high for more than 4 cycles, the AD7701 is reset and performs a calibration cycle when CAL is brought low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7701s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7701 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes high after transmission of a word is completed. It also goes high for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the synchronous self-clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7701's output data is available at this pin as a 16-bit serial word. The transmission format is determined by the state of the MODE pin.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (%FSR)	Package Options[2]
AD7701AN	−40°C to +85°C	0.003	N-20
AD7701BN	−40°C to +85°C	0.0015	N-20
AD7701AR	−40°C to +85°C	0.003	R-20
AD7701BR	−40°C to +85°C	0.0015	R-20
AD7701AQ	−40°C to +85°C	0.003	Q-20
AD7701BQ	−40°C to +85°C	0.0015	Q-20
AD7701SQ[3]	−55°C to +125°C	0.003	Q-20
AD7701TQ[3]	−55°C to +125°C	0.0015	Q-20

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

TIMING CHARACTERISTICS[1, 2]

(AV_{DD} = DV_{DD} = +5 V ± 10%; AV_{SS} = DV_{SS} = −5 V ± 10%; AGND = DGND = 0 V; f_{CLKIN} = 4.096 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD})

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	40	40	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4.096 MHz
	40	40	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC Mode				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns min	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9[8]	$1/f_{CLKIN}$ +200	$1/f_{CLKIN}$ +200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ +100 ns typ)
t_{10}[8, 9]	$(4/f_{CLKIN})$ +200	$(4/f_{CLKIN})$ +200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC Mode				
f_{SCLK}	5	5	MHz	Serial Clock Input Frequency
t_{11}	50	50	ns min	SCLK Input High Pulse Width
t_{12}	180	180	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns min	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns min	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns min	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns
AC Mode				
t_{17}	40	40	ns max	$\overline{CS}$ Setup Time. Typically 20 ns
t_{18}	180	180	ns max	Data Delay Time. Typically 90 ns
t_{19}	200	200	ns max	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 5.

[3]CLKIN Duty Cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7701 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7701 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7701s together using the $\overline{SLEEP}$ pin, this specification is met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_8, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such as independent of external bus loading capacitance.

[9]If $\overline{CS}$ is returned high before all 16 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, the SCLK input should not be taken high sooner then 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

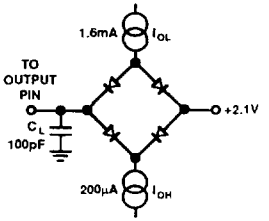
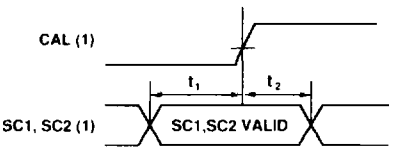
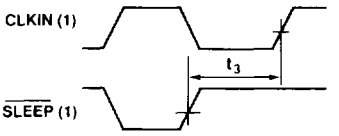


Figure 1. Load Circuit for Access Time and Bus Relinquish Time



2a. Calibration Control Timing



2b. SLEEP Mode Timing

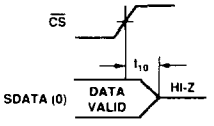


Figure 3. SSC Mode Data Hold Time

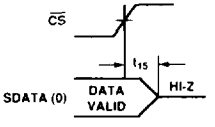


Figure 4a. SEC Mode Data Hold Time

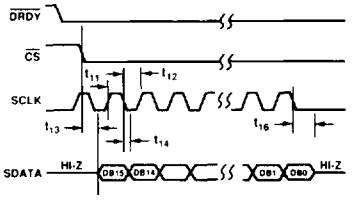


Figure 4b. SEC Mode Timing Diagram

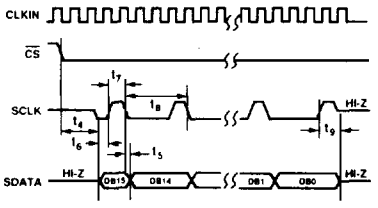


Figure 5. SSC Mode Timing Diagram

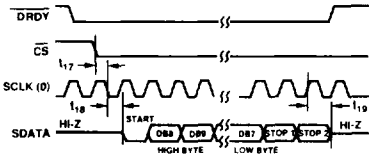


Figure 6. AC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are Zero-Scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} −3/2 LSBs). It applies to both positive and negative analog input ranges and it is expressed in microvolts.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode. It is expressed in microvolts.

BIPOLAR ZERO ERROR

This is the deviation of the mid-scale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND − 0.5 LSB) when operating in the bipolar mode. It is expressed in microvolts.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode. It is expressed in microvolts.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter. It is expressed in millivolts.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode. The overhead is expressed in millivolts.