FEATURES

- 3.3V power supply
- 50ps output-to-output skew
- Low power
- Synchronous enable/disable
- Multiplexed clock input
- 75KΩ internal input pull-down resistors
- Available in 16-pin SOIC package

DESCRIPTION

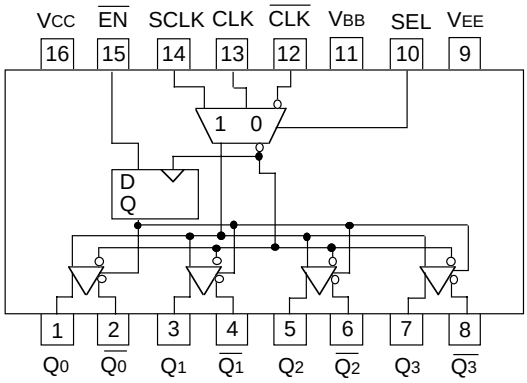
The SY100EL15L is a low skew 1:4 clock distribution IC designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to V_{EE} and $\overline{CLK}$ input will bias around $V_{CC}/2$.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Synchronous Clock Input
$\overline{EN}$	Synchronous Enable
SEL	Clock Select Input
V_{BB}	Reference Output
Q_{0-3}	Differential Clock Outputs

TRUTH TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{OUT}	Output Current –Continuous –Surge	 50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C

NOTES:

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 3 volt Power Supply Range 100EL15L Series –3.0V to –3.8V.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = 3.3V ±10%; V_{CC} = GND[1]

		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage[2]	–1085	–880	–1025	–880	–1025	–955	–880	–1025	–880	mV
V_{OL}	Output LOW Voltage[2]	–1830	–1555	–1810	–1620	–1810	–1705	–1620	–1810	–1620	mV
V_{OHA}	Output HIGH Voltage[3]	–1095	—	–1035	—	–1035	—	—	–1035	—	mV
V_{OLA}	Output LOW Voltage[3]	—	–1555	—	–1610	—	—	–1610	—	–1610	mV
V_{IH}	Input HIGH Voltage	–1165	–880	–1165	–880	–1165	—	–880	–1165	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1475	–1810	–1475	–1810	—	–1475	–1810	–1475	mV
I_{IH}	Input High Current	—	150	—	150	—	—	150	—	150	µA
I_{IL}	Input LOW Current[4] $\overline{CLK}$	0.5 –300	— —	0.5 –300	— —	0.5 –300	 —	— —	0.5 –300	— —	µA
I_{EE}	Power Supply Current	—	35	—	35	—	25	35	—	38	mA
V_{BB}	Output Reference Voltage	–1.38	–1.26	–1.38	–1.26	–1.38	—	–1.26	–1.38	–1.26	V

NOTES:

1. This table replaces the three traditionally seen in ECL 100K data books. Outputs are terminated through a 50Ω resistor to –2.0V.
2. V_{IN} = V_{IH}(Max) or V_{IL}(Min).
3. V_{IN} = V_{IH}(Min) or V_{IL}(Max).
4. V_{IN} = V_{IL}(Max).

AC ELECTRICAL CHARACTERISTICS

V_{EE} = 3.3V ±10%; V_{CC} = GND[1]

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 460 410 410	 660 710 710	 470 420 420	 670 720 720	 470 420 420	 — — —	 670 720 720	 500 450 470	 700 750 750	ps
t_{skew}	Part-to-Part Skew[1] Within-Device Skew	— —	200 50	— —	200 50	— —	— —	200 50	— —	200 50	ps
t_S	Setup Time $\overline{EN}$	150	—	150	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	400	—	400	—	400	—	—	400	—	ps
V_{PP}	Minimum Input Swing CLK	 250	 —	 250	 —	 250	 —	 —	 250	 —	 mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 –2.0 –1.8	 –0.4 –0.4	 –2.1 –1.9	 –0.4 –0.4	 –2.1 –1.9	 — —	 –0.4 –0.4	 –2.1 –1.9	 –0.4 –0.4	mV
t_r t_f	Output Rise/Fall TimesQ (20% – 80%)	375	625	325	575	325	—	575	325	575	ps

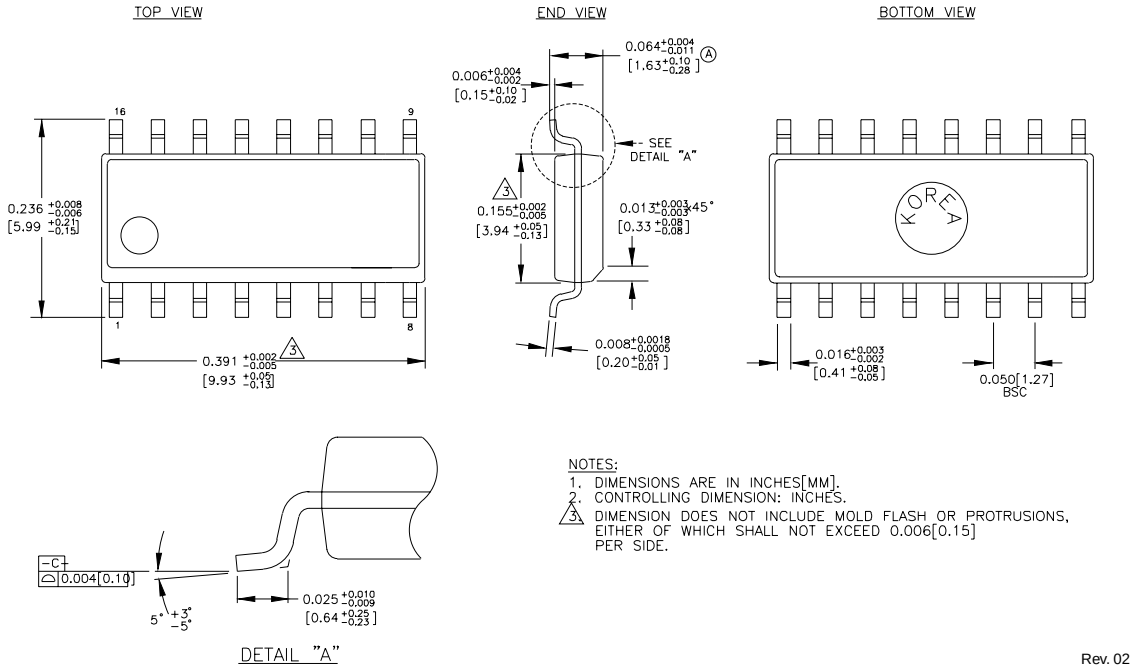
NOTES:

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP}(Min.) and <1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(Min) will be fixed at 3.3V – |V_{CMR}(Min)|.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL15LZC	Z16-2	Commercial
SY100EL15LZCTR	Z16-2	Commercial

16 LEAD SOIC .150" WIDE (Z16-2)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Rev. 02