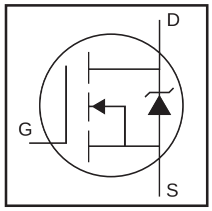
飞思卡尔(深圳)功率半导体有限公司

# IRF/B/S/SL4310

## Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## Benefits
- Worldwide Best $R_{DS(on)}$ in TO-220
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

HEXFET® Power MOSFET




| | | |
|---|---|---|
| $V_{DSS}$ | | 100V |
| $R_{DS(on)}$ | typ. | 5.6mΩ |
| | max. | 7.0mΩ |
| $I_D$ | | 140A |


TO-220AB IRFB4310 | D²Pak IRFS4310 | TO-262 IRFSL4310

### Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 140① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 97 ① | |
| $I_{DM}$ | Pulsed Drain Current ② | 550 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 330 | W |
| | Linear Derating Factor | 2.2 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| dV/dt | Peak Diode Recovery ④ | 14 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds<br>(1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lb·in (1.1N·m) | |

### Avalanche Characteristics

| | | | |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ③ | 980 | mJ |
| $I_{AR}$ | Avalanche Current ① | See Fig. 14, 15, 22a, 22b, | A |
| $E_{AR}$ | Repetitive Avalanche Energy ⑤ | | mJ |

### Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑨ | — | 0.45 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface , TO-220 | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient, TO-220 ⑨ | — | 62 | |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) , D²Pak ⑧⑨ | — | 40 | |

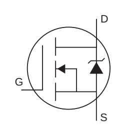
## Static @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.064 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 5.6 | 7.0 | mΩ | $V_{GS}$ = 10V, $I_D$ = 75A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | —— | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 20 | μA | $V_{DS}$ = 100V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 100V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 200 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -200 | | $V_{GS}$ = -20V |
| $R_G$ | Gate Input Resistance | —— | 1.4 | —— | Ω | f = 1MHz, open drain |

## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 160 | —— | —— | S | $V_{DS}$ = 50V, $I_D$ = 75A |
| $Q_g$ | Total Gate Charge | —— | 170 | 250 | nC | $I_D$ = 75A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 46 | —— | | $V_{DS}$ = 80V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 62 | —— | | $V_{GS}$ = 10V ⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 26 | —— | ns | $V_{DD}$ = 65V |
| $t_r$ | Rise Time | —— | 110 | —— | | $I_D$ = 75A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 68 | —— | | $R_G$ = 2.6Ω |
| $t_f$ | Fall Time | —— | 78 | —— | | $V_{GS}$ = 10V ⑤ |
| $C_{iss}$ | Input Capacitance | —— | 7670 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 540 | —— | | $V_{DS}$ = 50V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 280 | —— | | $f$ = 1.0MHz |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related)⑦ | —— | 650 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 80V ⑧, See Fig.11 |
| $C_{oss}$ eff. (TR) | Effective Output Capacitance (Time Related)⑥ | —— | 720.1 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 80V ⑥, See Fig. 5 |

## Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 140① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ②⑦ | —— | —— | 550 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C, $I_S$ = 75A, $V_{GS}$ = 0V ⑤ |
| $t_{rr}$ | Reverse Recovery Time | —— | 45 | 68 | ns | $T_J$ = 25°C   $V_R$ = 85V, |
| | | —— | 55 | 83 | | $T_J$ = 125°C   $I_F$ = 75A |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 82 | 120 | nC | $T_J$ = 25°C   di/dt = 100A/μs ⑤ |
| | | —— | 120 | 180 | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | —— | 3.3 | —— | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.35mH $R_G$ = 25Ω, $I_{AS}$ = 75A, $V_{GS}$ =10V. Part not recommended for use above this value.

④ $I_{SD} \leq$ 75A, di/dt ≤ 550A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recom mended footprint and soldering techniques refer to application note #AN-994.

⑨ $R_\theta$ is measured at $T_J$ approximately 90°C

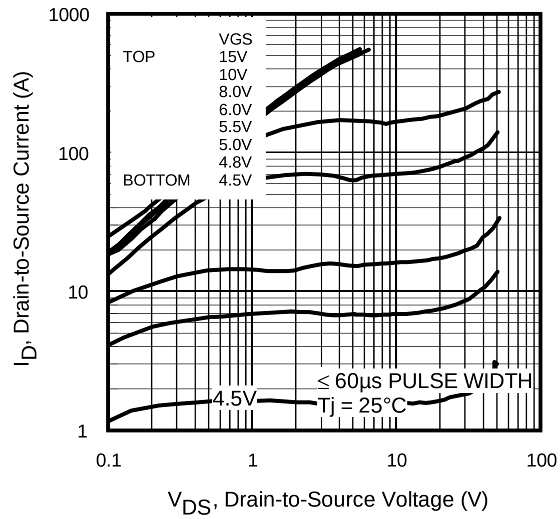



**Fig 1.** Typical Output Characteristics

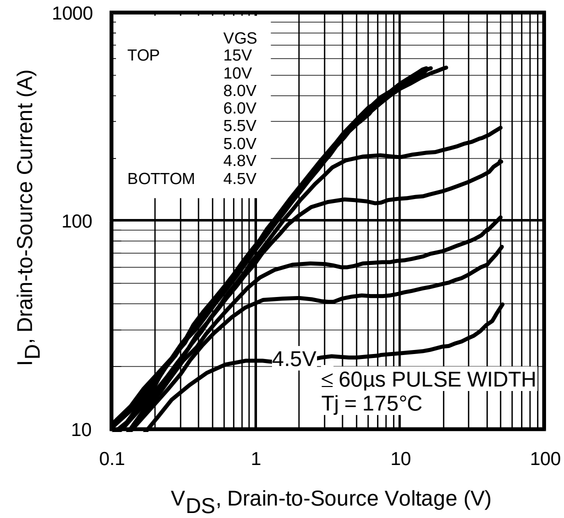



**Fig 2.** Typical Output Characteristics

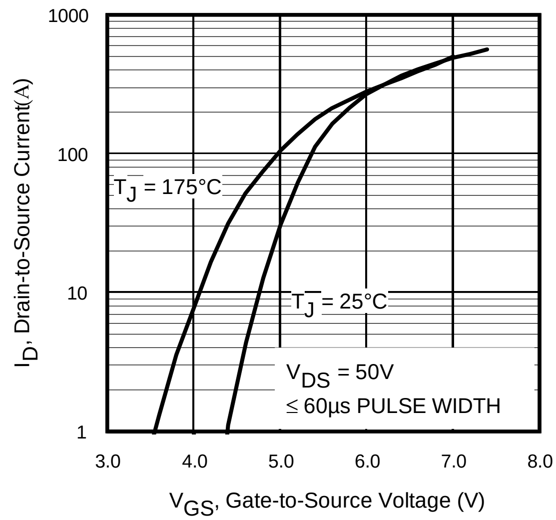



**Fig 3.** Typical Transfer Characteristics

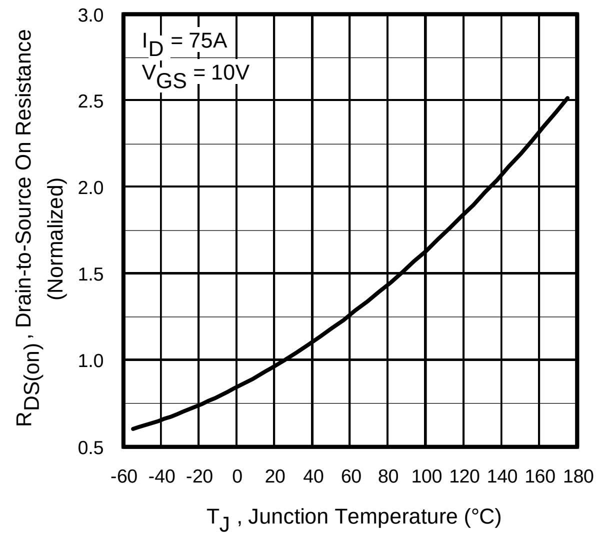



**Fig 4.** Normalized On-Resistance vs. Temperature

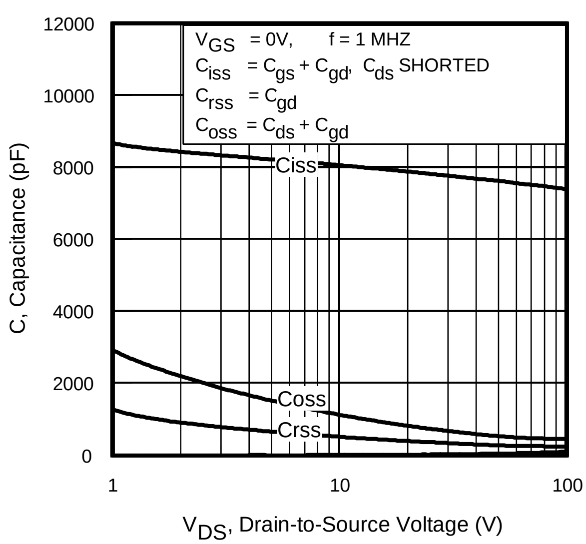



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

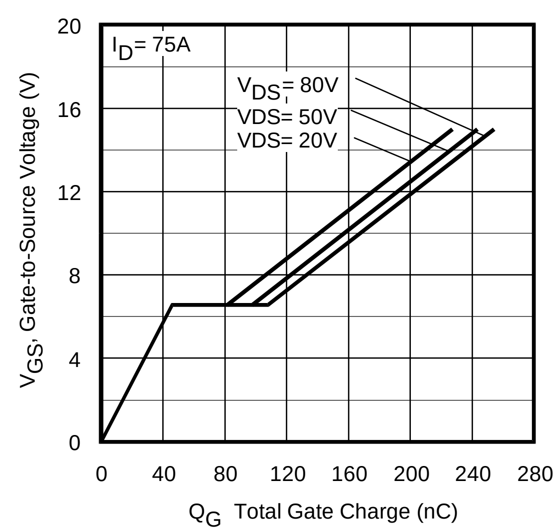



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

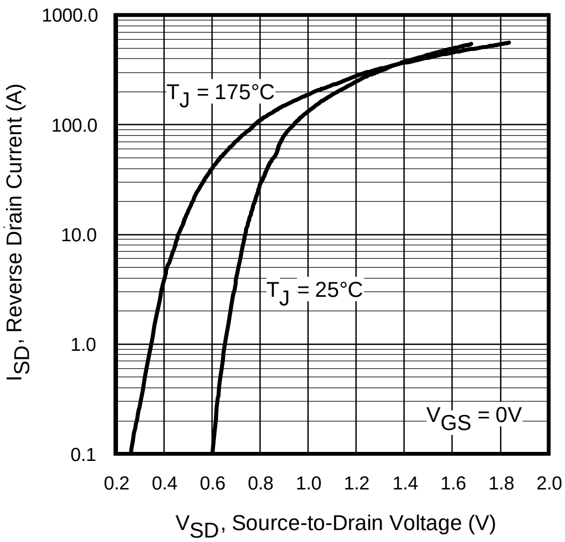



**Fig 7.** Typical Source-Drain Diode Forward Voltage

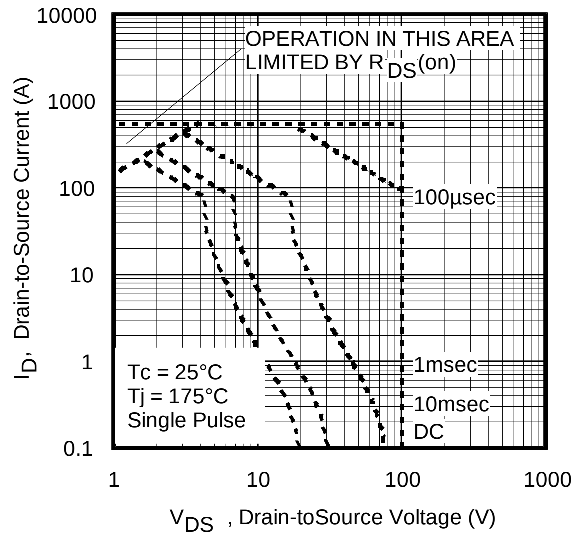



**Fig 8.** Maximum Safe Operating Area

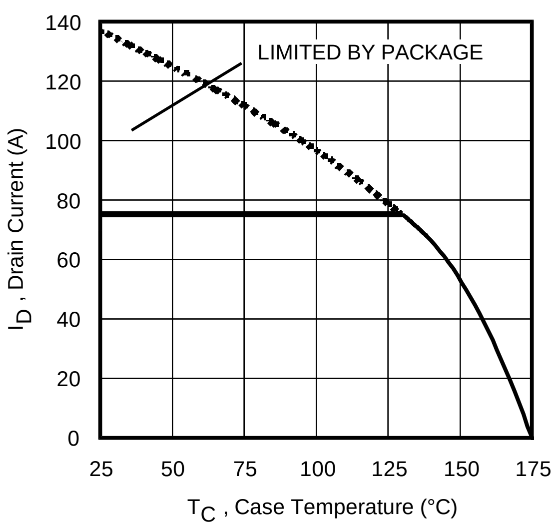



**Fig 9.** Maximum Drain Current vs. Case Temperature

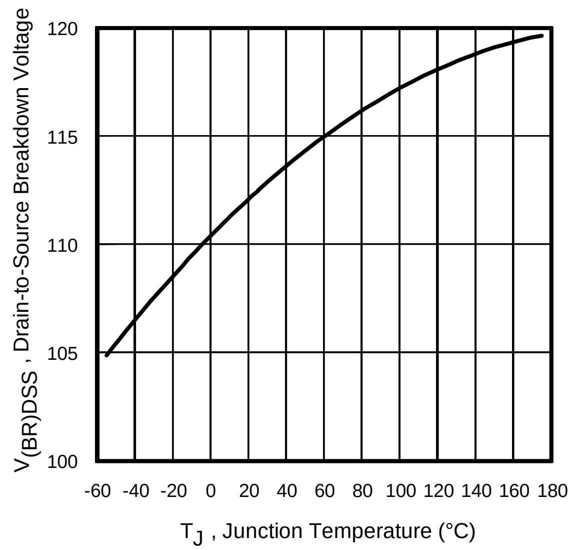



**Fig 10.** Drain-to-Source Breakdown Voltage

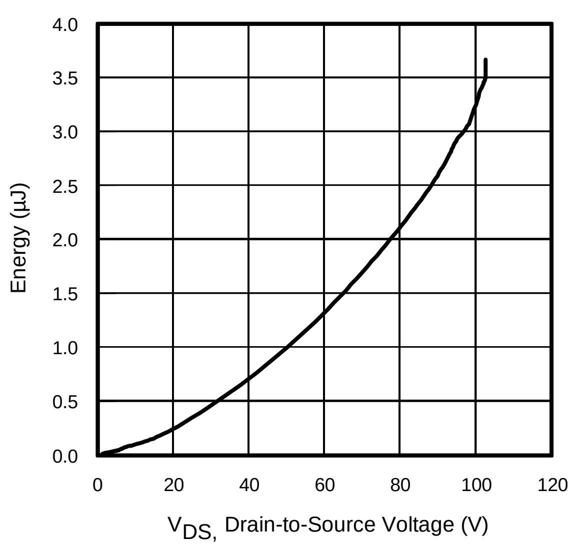



**Fig 11.** Typical $C_{OSS}$ Stored Energy

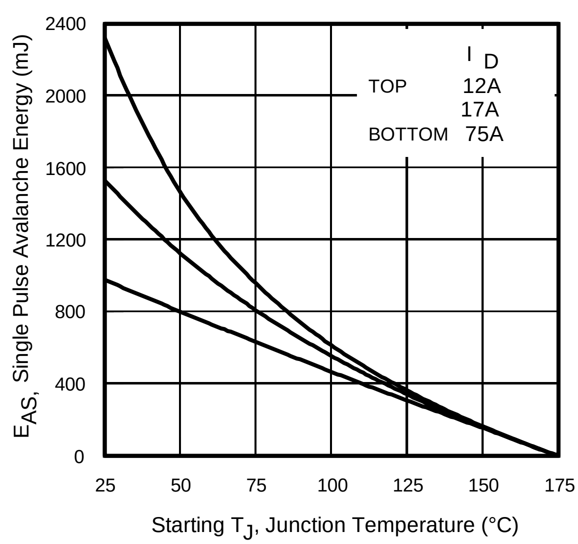



**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent

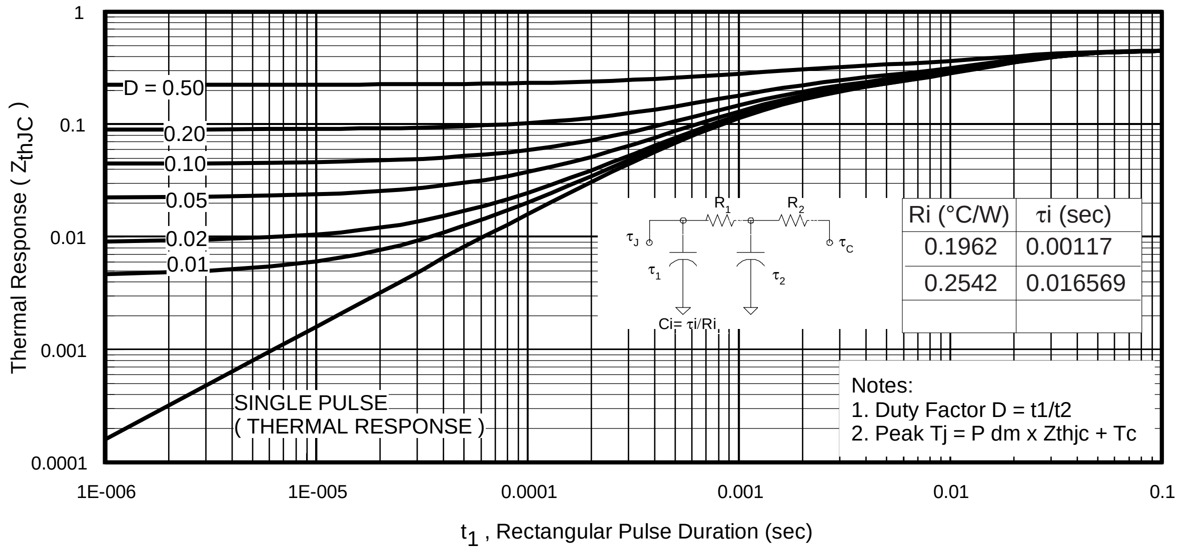



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

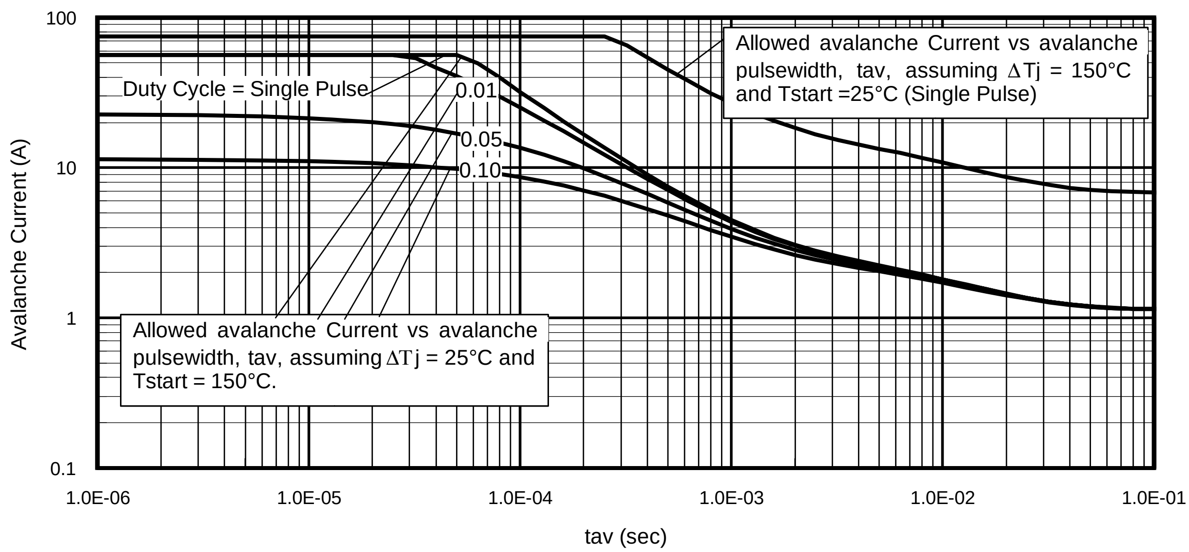



**Fig 14.** Typical Avalanche Current vs.Pulsewidth

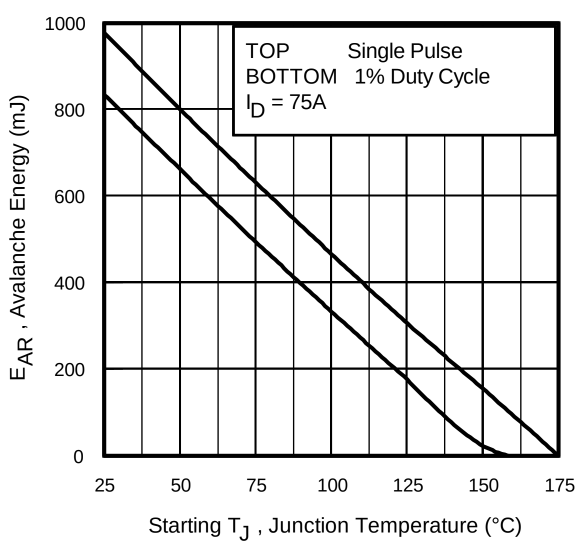



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither $T_{jmax}$ nor Iav (max) is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 14, 15).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

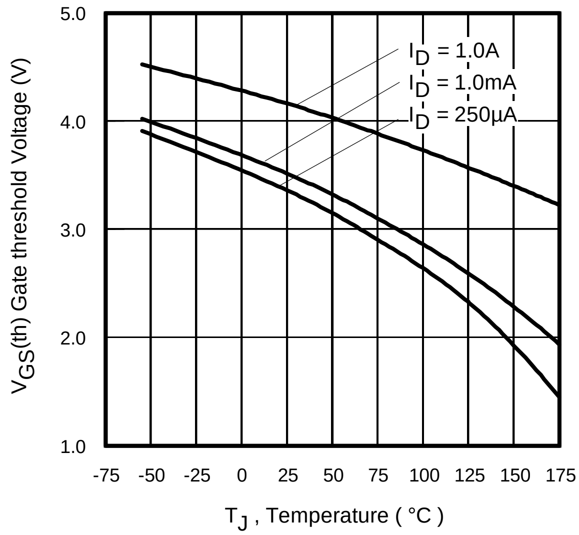



**Fig 16.** Threshold Voltage Vs. Temperature

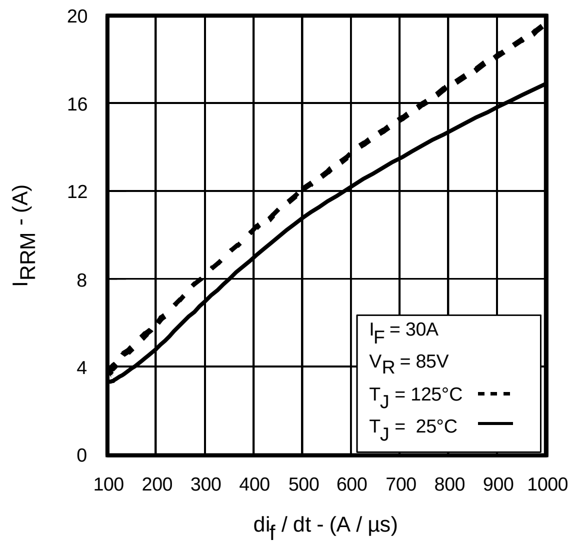



**Fig. 17 -** Typical Recovery Current vs. $di_f/dt$

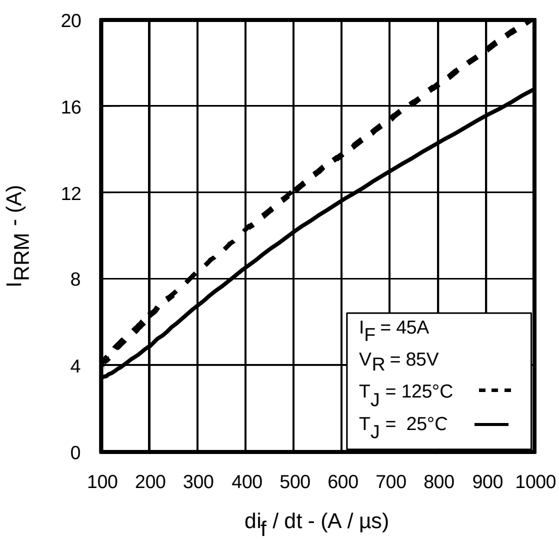



**Fig. 18 -** Typical Recovery Current vs. $di_f/dt$

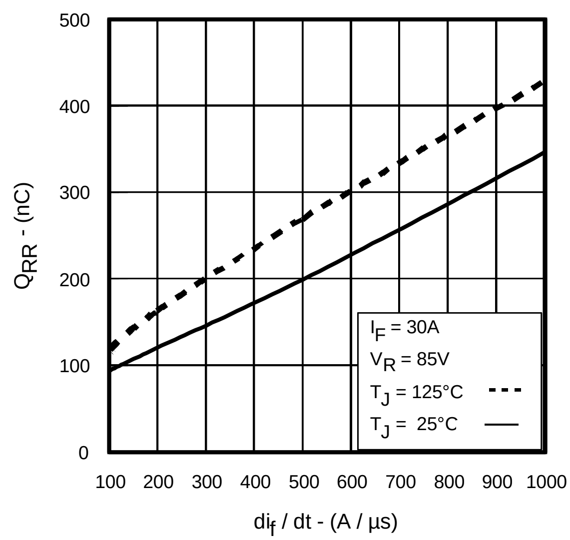



**Fig. 19 -** Typical Stored Charge vs. $di_f/dt$

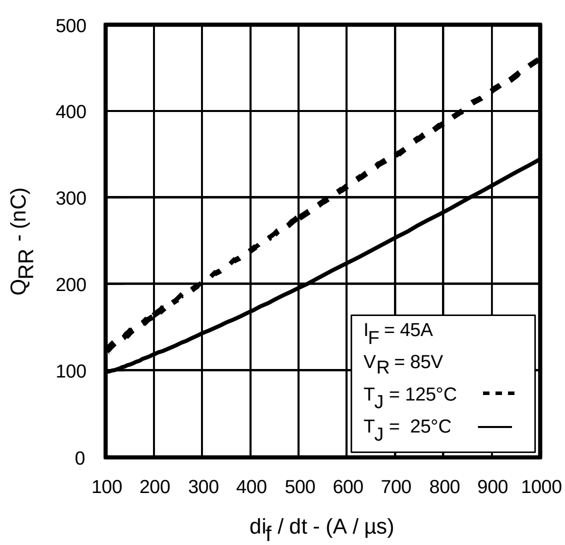



**Fig. 20 -** Typical Stored Charge vs. $di_f/dt$

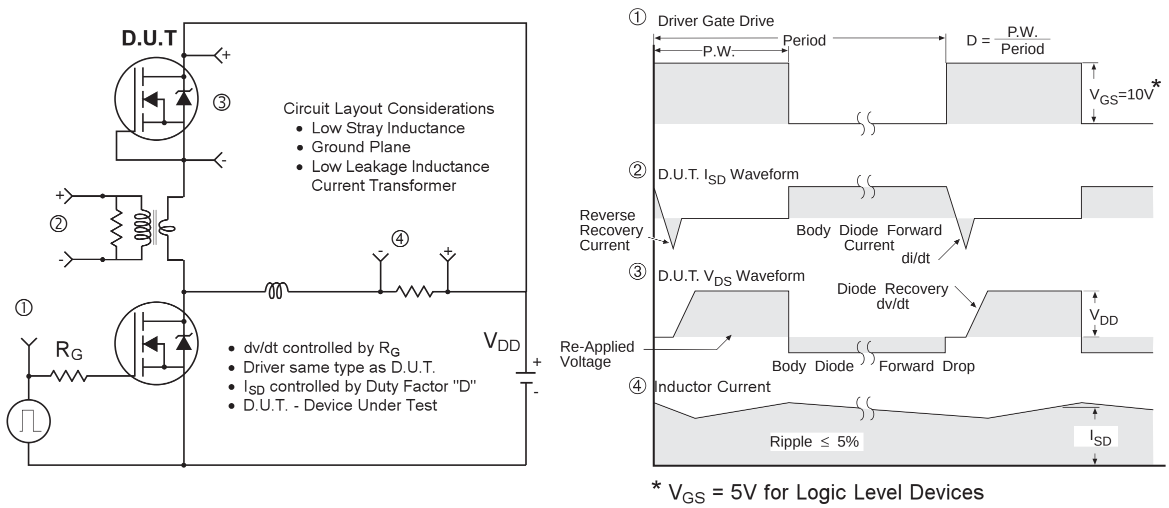



**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

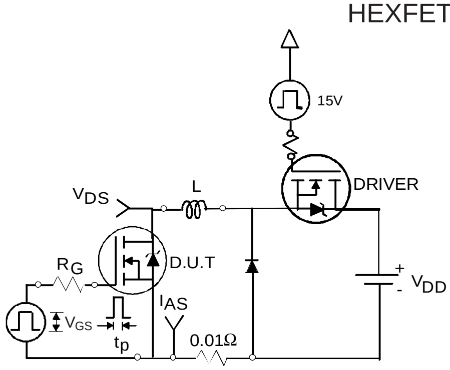



**Fig 22a.** Unclamped Inductive Test Circuit

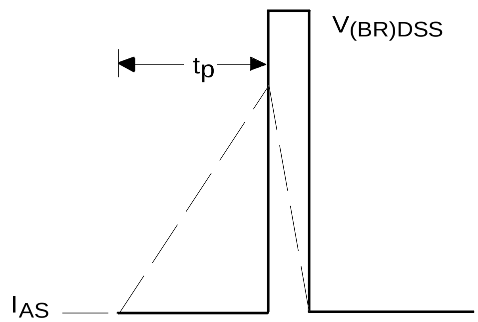



**Fig 22b.** Unclamped Inductive Waveforms

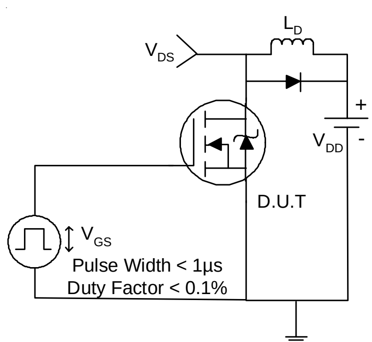



**Fig 23a.** Switching Time Test Circuit

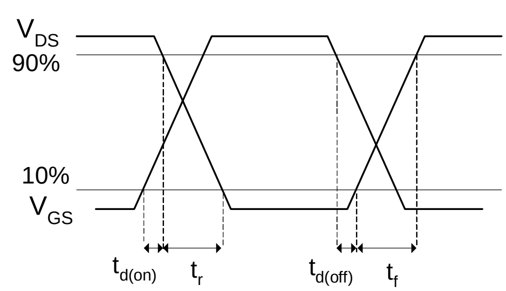



**Fig 23b.** Switching Time Waveforms

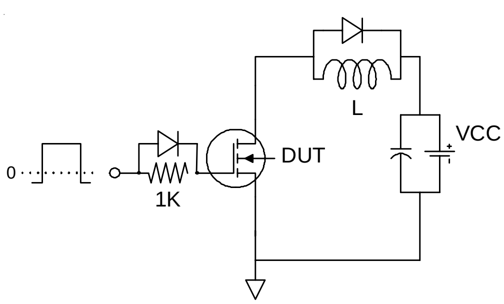



**Fig 24a.** Gate Charge Test Circuit

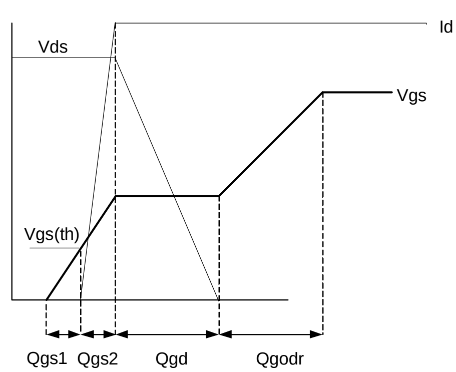
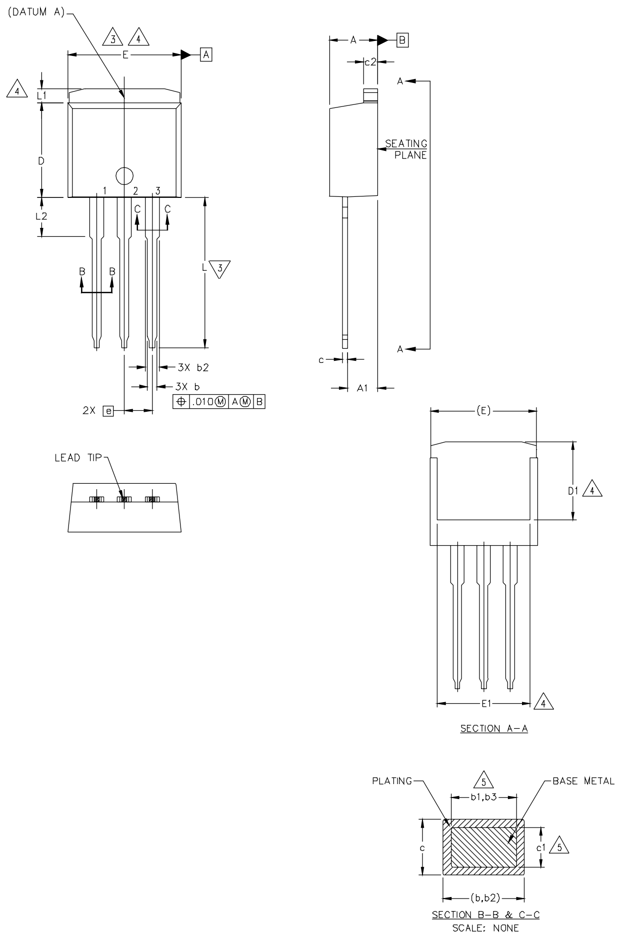



**Fig 24b.** Gate Charge Waveform

# TO-262 Package Outline

Dimensions are shown in millimeters (inches)




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7.– OUTLINE CONFORM TO JEDEC TO–262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 3.02 | .080 | .119 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | – | .270 | – | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | – | .245 | | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.10 | .530 | .555 | |
| L1 | – | 1.65 | – | .065 | 4 |
| L2 | 3.56 | 3.71 | .140 | .146 | |

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

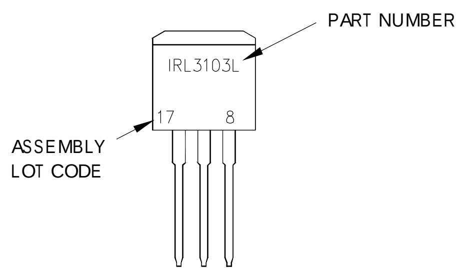
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

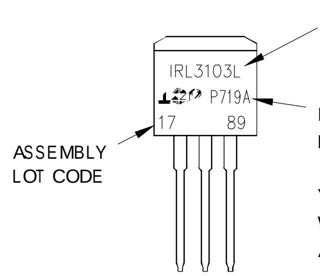
# TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line positio
indicates "Lead – Free"

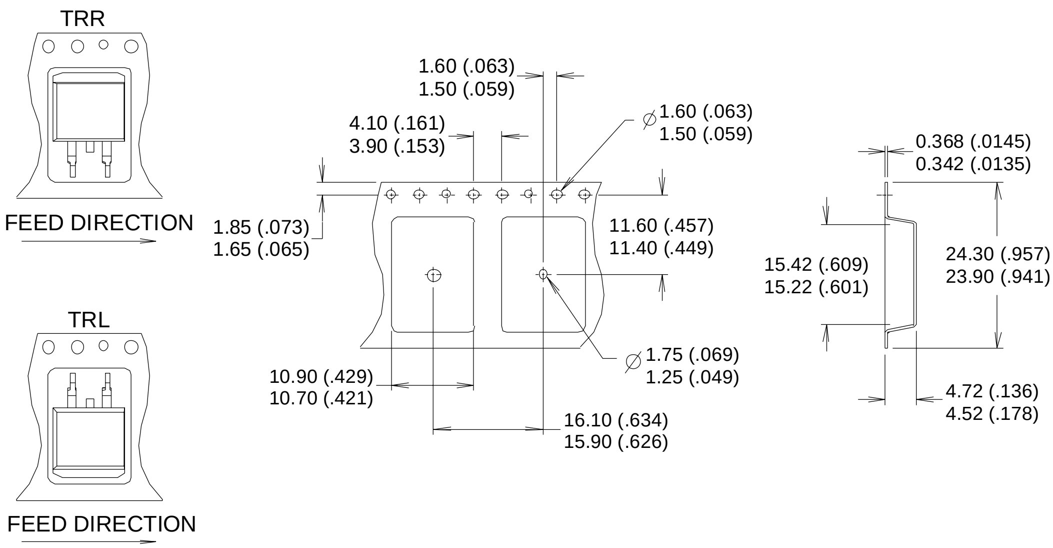


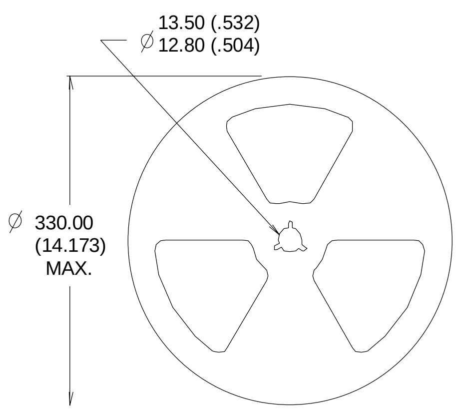

OR

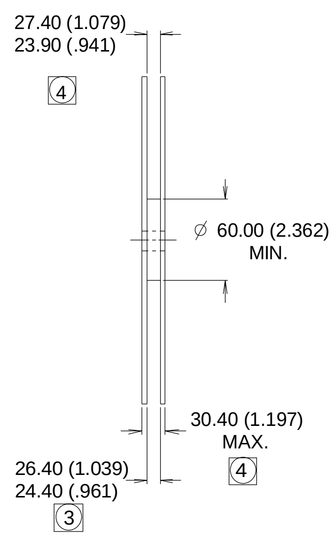



DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE

## D²Pak (TO-263AB) Tape & Reel Information




NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.