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NEW

CCD linear image sensor

S11151-2048

High sensitivity in the ultraviolet region, front-illuminated CCD

Despite a front-illuminated CCD, the S11151-2048 offers high sensitivity in the ultraviolet region (200 nm) nearly equal to back-thinned CCD.

Features

- **High sensitivity in the ultraviolet region (spectral response range: 200 to 1000 nm)**
- **Image lag: 0.1% typ.**
- **Low dark current**
- **Low cost**

Applications

- **Spectrometers**

Structure

Parameter	Specification
Pixel size (H × V)	14 × 200 µm
Number of total pixels	2056
Number of effective pixels	2048
Image size (H × V)	28.672 × 0.200 mm
Horizontal clock phase	2-phase
Output circuit	Two-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outline)
Window material	Quartz glass*1

*1: Resin sealing

Absolute maximum ratings (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2 *3		Topr	-50	-	+55	°C
Storage temperature*3		Tstg	-50	-	+70	°C
Output transistor drain voltage		VOD	-0.5	-	+25	V
Reset drain voltage		VRD	-0.5	-	+18	V
Test point	Vertical input source voltage	VISV	-0.5	-	+18	V
	Horizontal input source voltage	VISH	-0.5	-	+18	V
	Vertical input gate voltage	VIGV	-10	-	+15	V
	Horizontal input gate voltage	VIGH	-10	-	+15	V
Summing gate voltage		VSG	-10	-	+15	V
Output gate voltage		VOG	-10	-	+15	V
Reset gate voltage		VRG	-10	-	+15	V
Transfer gate voltage		VTG	-10	-	+15	V
Horizontal shift register clock voltage		VP1H, VP2H	-10	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
*2: Package temperature
*3: No condensation

Operating conditions (Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	13	14	V
Reset drain voltage			V_{RD}	10.5	11	11.5	V
Test point	Vertical input source voltage		V_{ISV}	-	V_{RD}	-	V
	Horizontal input source voltage		V_{ISH}	-	V_{RD}	-	V
	Vertical input gate voltage		V_{IGV}	-5	-4	-	V
	Horizontal input gate voltage		V_{IGH}	-5	-4	-	V
Summing gate voltage		High	V_{SGH}	4	5	6	V
		Low	V_{SGL}	-5	-4	-3	
Output gate voltage			V_{OG}	2	3	4	V
Substrate voltage			V_{SS}	-	0	-	V
Reset gate voltage		High	V_{RGH}	4	5	6	V
		Low	V_{RGL}	-5	-4	-3	
Transfer gate voltage		High	V_{TGH}	7	8	9	V
		Low	V_{TGL}	-5	-4	-3	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	4	5	6	V
		Low	V_{P1HL}, V_{P2HL}	-5	-4	-3	
External load resistance			R_L	2.0	2.2	2.4	kΩ

Electrical characteristics (Ta=25 °C, unless otherwise noted, operating conditions: Typ.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency*4	fc	-	1	5	MHz
Line rate	LR	-	0.48	2.37	kHz
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	220	-	pF
Summing gate capacitance	C_{SG}	-	10	-	pF
Reset gate capacitance	C_{RG}	-	10	-	pF
Transfer gate capacitance	C_{TG}	-	110	-	pF
Charge transfer efficiency*5	CTE	0.99995	0.99999	-	-
DC output level*4	Vout	-	8.5	-	V
Output impedance*4	Zo	-	220	-	Ω
Power consumption*4 *6	P	-	65	-	mW

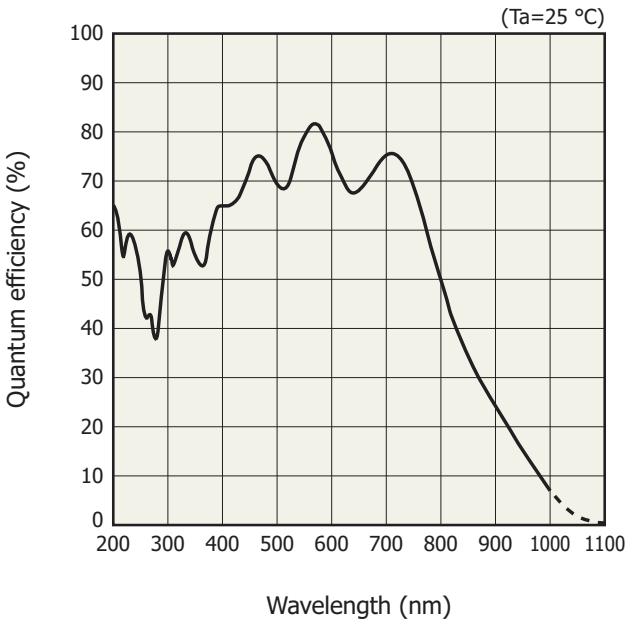
*4: The value depends on the load resistance.
*5: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity
*6: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted, operating conditions: Typ.)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity		Fw	150	200	-	ke^-
CCD node sensitivity		Sv	5	6	7	$\mu V/e^-$
Dark current*7	Average of all effective pixels	DSave	-	700	3500	e^-/pixel/s
			-	4	20	pA/cm²
	Maximum of all effective pixels	DSmax	-	3500	17500	e^-/pixel/s
			-	20	100	pA/cm²
Readout noise*8		Nr	-	25	50	e^- rms
Dynamic range*9		DR	3000	8000	-	-
Spectral response range		λ	-	200 to 1000	-	nm
Photoresponse nonuniformity*10 *11		PRNU	-	±3	±10	%
Image lag*10		L	-	0.1	1	%

*7: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*8: Readout frequency 1 MHz
*9: Dynamic range = Full well capacity / Readout noise
*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)
*11: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]

Spectral response (without window, typical example)*12



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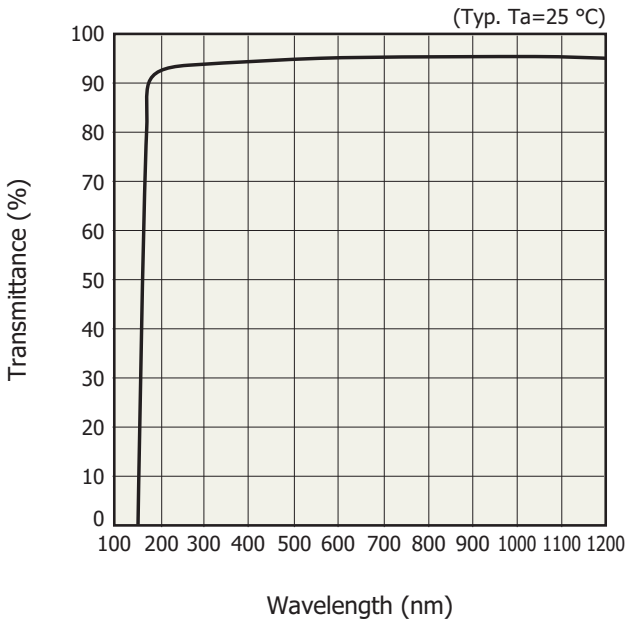
Spectral transmittance characteristics of window material



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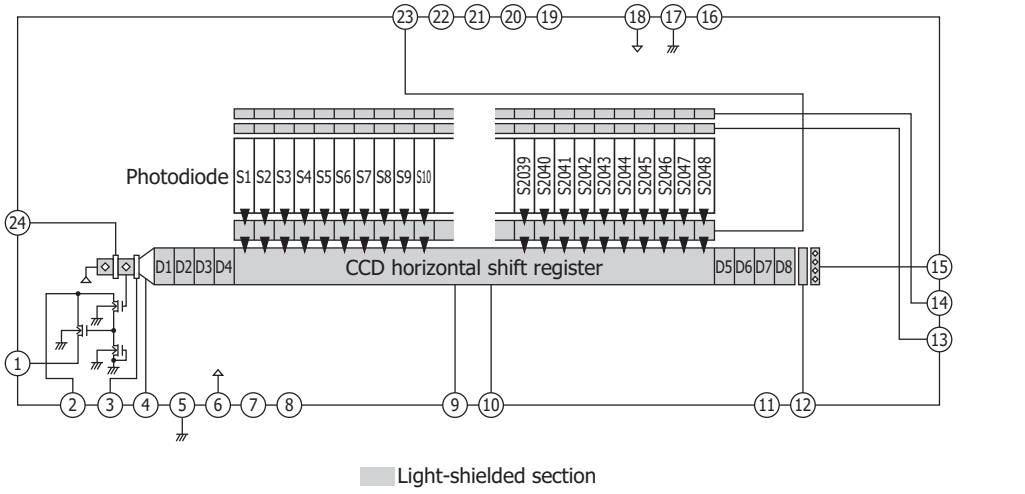
*12: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

Device structure (conceptual drawing of top view)



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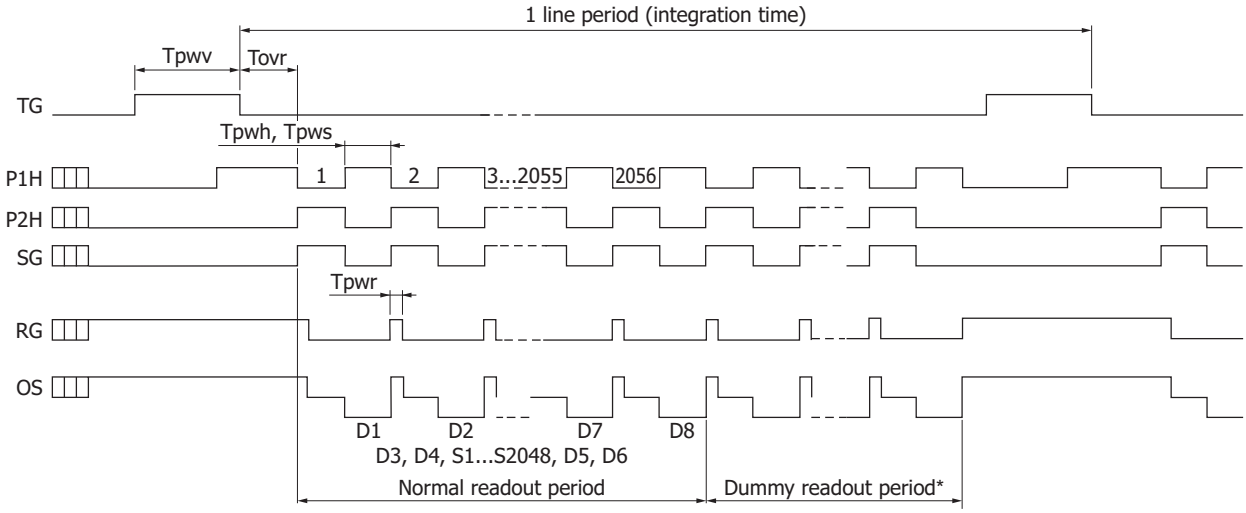
Timing chart



* When making the integration time longer than the normal readout period, to carry away the dark current generated in the CCD horizontal shift register, perform dummy readout after completion of the normal readout until right before rising transfer gate pulse.

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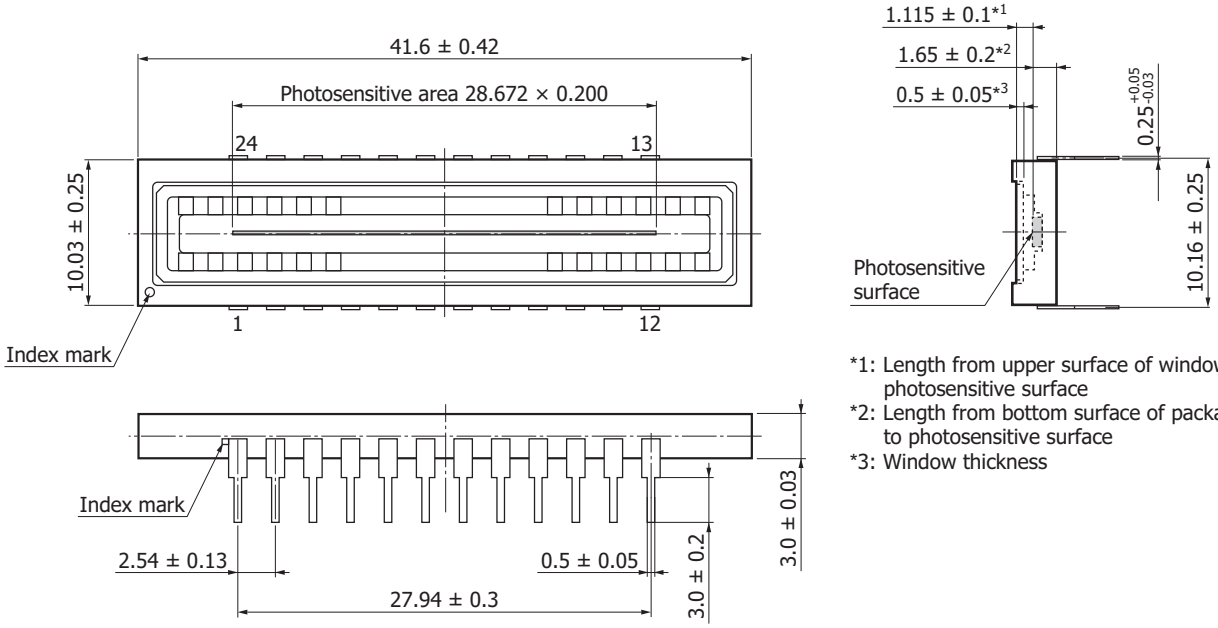
Parameter		Symbol	Min.	Typ.	Max.	Unit
TG	Pulse width	Tpwv	6	8	-	µs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*13	Pulse width	Tpwh	100	500	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	100	500	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	10	100	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time	Tovr	1	2	-	µs

*13: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm, tolerance unless otherwise noted: ±0.1)



*1: Length from upper surface of window to photosensitive surface
*2: Length from bottom surface of package to photosensitive surface
*3: Window thickness

Note: This product is not hermetically sealed and moisture may penetrate inside the package. Avoid using or storing this product in an environment where sudden temperature and humidity changes may occur and cause condensation in the package.

KMPDA0261EC

Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=2.2 kΩ
2	OD	Output transistor drain	+13 V
3	OG	Output gate	+3 V
4	SG	Summing gate	Same pulse as P2H
5	SS	Substrate	GND
6	RD	Reset drain	+11 V
7	-		
8	-		
9	P2H	CCD horizontal register clock-2	+5/-4 V
10	P1H	CCD horizontal register clock-1	+5/-4 V
11	-		
12	IGH	Test point (horizontal input gate)	-4 V
13	IGV	Test point (vertical input gate)	-4 V
14	ISV	Test point (vertical input source)	Connect it to RD.
15	ISH	Test point (horizontal input source)	Connect it to RD.
16	-		
17	SS	Substrate	GND
18	RD	Reset drain	+11 V
19	-		
20	-		
21	-		
22	-		
23	TG	Transfer gate	+8/-4 V
24	RG	Reset gate	+5/-4 V

Related information

■ Precautions
http://jp.hamamatsu.com/sp/ssd/tech_pre_en.html

・Precautions for use (Image sensors)

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